A 5GHz, 1mW CMOS Voltage–Controlled Differential Injection–Locked Frequency Divider

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OUTLINE

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- motivation
- injection–locked frequency dividers (ILFDs)
  - mathematical model
  - circuit implementation
  - design issues
    - ∗ optimal inductor design
- measurement results
- summary
- conclusion

Motivation

- wireless systems:
  - are narrowband
  - require frequency synthesizers
  - require low power operation

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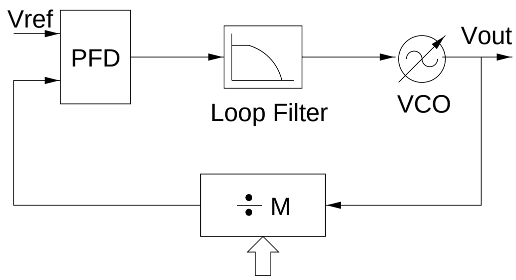
- PLL–based frequency synthesizer require frequency dividers which are conventionally:
  - wideband
  - power hungry



Idea

- design a low–power and narrowband frequency divider

use resonators to trade off bandwidth for power

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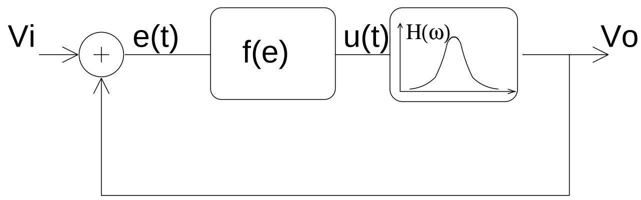
ILFD MODEL



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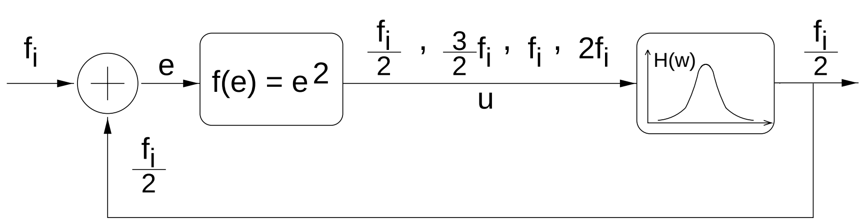
$$v_o(t) = V_o cos(\omega_o t)$$
$$v_i(t) = V_i cos(\omega_i t + \phi)$$
$$u(t) = f[e(t)] = f[v_o(t) + v_i(t)]$$
$$H(\omega) = \frac{H_0}{1 + j2Q\frac{\omega-\omega_r}{\omega_r}}$$

- oscillation condition should be satisfied in the presence of the incident signal.

SIMPLIFIED PICTURE



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e=$\cos(\mathrm{f_i t}) + \cos(\frac{\mathrm{f_i}}{2}\mathrm{t})$

u=$(\cos(\mathrm{f_i t}) + \cos(\frac{\mathrm{f_i}}{2}\mathrm{t}))^2$

u=$1 + \frac{1}{2}\cos(2\mathrm{f_i t}) + \frac{1}{2}\cos(\mathrm{f_i t}) + \cos(\frac{3\mathrm{f_i}}{2}\mathrm{t}) + \cos(\frac{\mathrm{f_i}}{2}\mathrm{t})$

Special case (divide–by–two)

$$f(e) = a_0 + a_1 e + a_2 e^2 + a_3 e^3$$

- phase condition:

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$$|\frac{\Delta\omega}{\omega_r}| < |\frac{H_0 a_2 V_i}{2Q}| \qquad , \qquad \frac{H_0}{Q} = \frac{LQ\omega_r}{Q} = L\omega_r$$

- gain condition:

$$V_o = \sqrt{\frac{4}{3}\frac{1}{a_3 H_0}[1 - H_0(a_1 + \frac{3}{2}a_3 V_i^2 + a_2 V_i cos(\phi))]}$$

Voltage–controlled differential ILFD

- 0.24μm CMOS
- Vdd=1.5V
- I_{bias}=300μA
- f_o=2.25GHz
- f_i=4.5GHz

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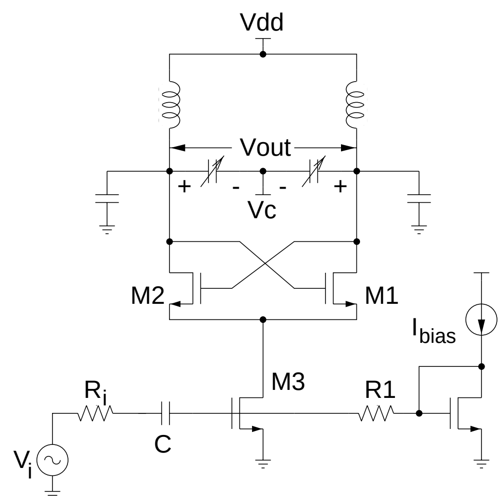

DESIGN OBJECTIVE

- maximum locking range ⇒ maximize L
- minimum power consumption ⇒ maximize LQ

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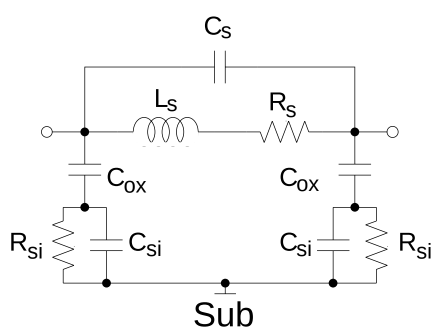
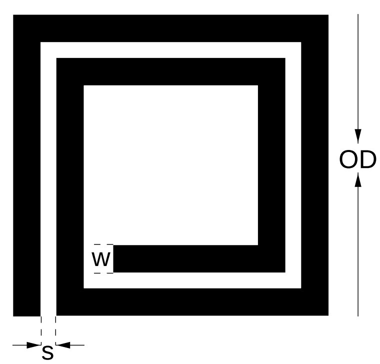
INDUCTOR DESIGN





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- design parameters:
  - w: metal width
  - s: metal spacing
  - OD: outer dimension
  - n: number of turns

INDUCTOR DESIGN

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- in planar spiral inductors maximizing L does not maximize LQ

$$\Downarrow$$

maximize L for a given LQ

MEASUREMENT (FREE–RUNNING OSCILLATION)

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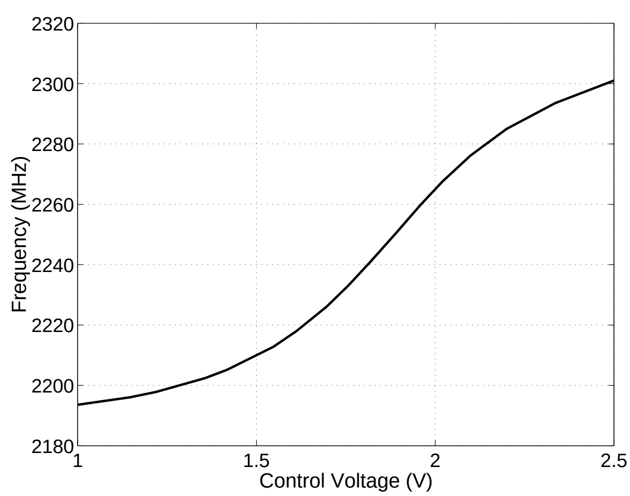
- 0.24μm CMOS
- Vdd=2.0V
- $\mathrm{I}_{\mathrm{bias}}$=600$\mu$A
- Δf=110MHz
- ΔV_c=1.5V



Measurements (frequency range)

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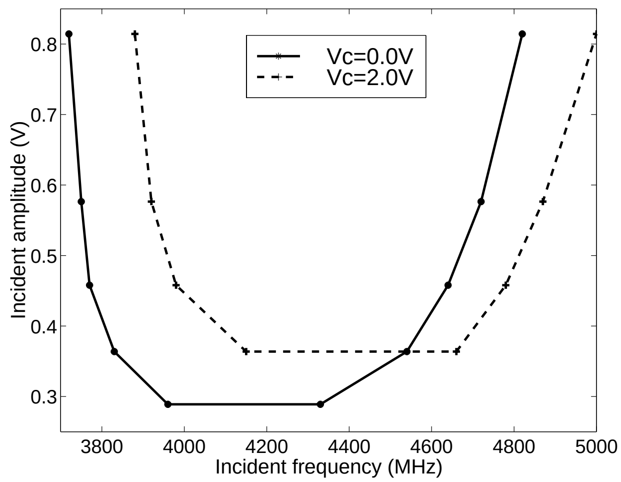
- 0.24μm CMOS
- Vdd=1.5V
- I_{bias}=300μA



Smart circuit

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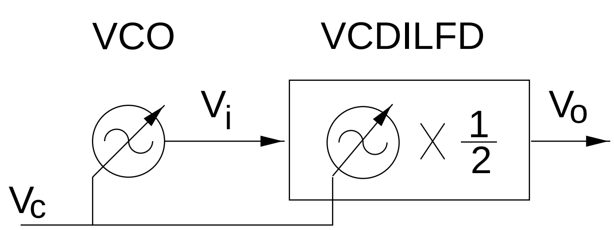

MEASUREMENTS (LOCKING RANGE)

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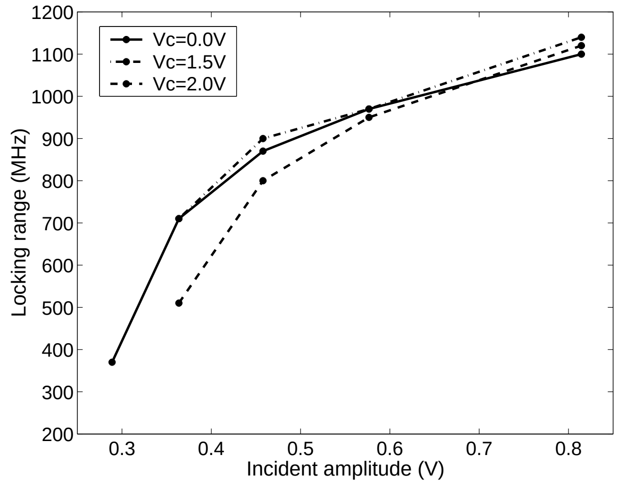
- 0.24μm CMOS
- Vdd=1.5V
- f_o=2.2GHz
- f_i=4.4GHz



MEASUREMENTS (POWER CONSUMPTION)

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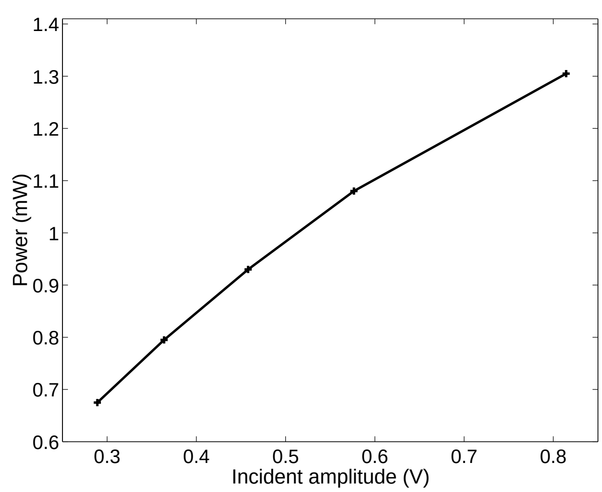
- 0.24μm CMOS
- Vdd=1.5V
- f_o=2.2GHz
- f_i=4.4GHz



PHASE NOISE MEASUREMENT TEST SETUP

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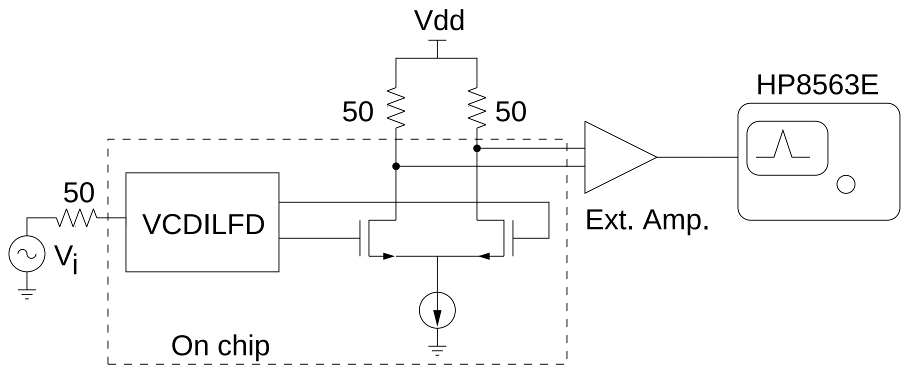

MEASUREMENTS (PHASE NOISE)

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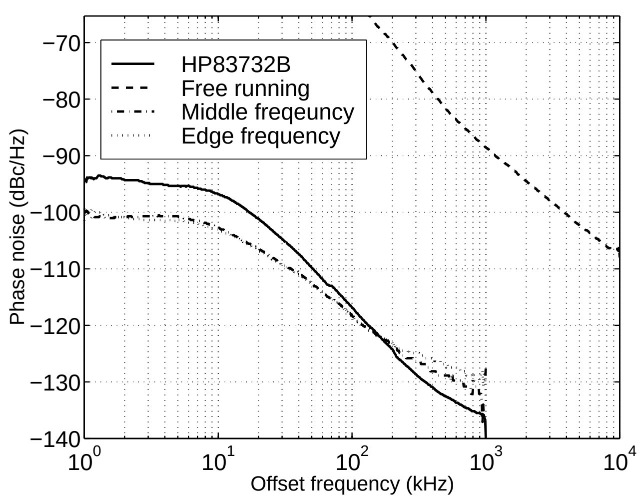
- 0.24μm CMOS
- Vdd=1.5V
- f_o=2.2GHz
- f_i=4.4GHz



CHIP MICROGRAPH

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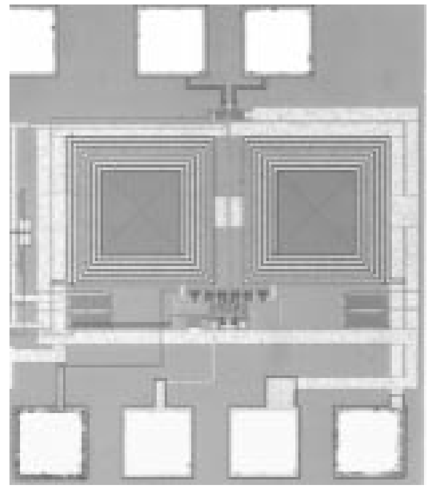
- 0.24μm CMOS
- area=0.186mm^2 ($345\mu\text{m} \times 540\mu\text{m}$)



SUMMARY

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maximum operation frequency	5GHz
free–running frequency tuning	110MHz
locking range	900MHz @ 1.0mW
	1.28GHz @ 1.3mW
technology	0.24μm CMOS
die area	0.186mm^2

CONCLUSION

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- injection–locked frequency dividers can be designed with:
  - very large locking range
  - very low power consumption
- spiral inductor design can be optimized to increase the ILFD locking range
- varactors can be used to extend the ILFD locking range
- voltage–controlled ILFDs are suitable for low–power and high–frequency wireless systems

ACKNOWLEDGMENT

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