Recent Developments in CMOS RF Integrated Circuits

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Introduction

- Digital CMOS is hardly the ideal medium for RF ICs. But is it hopelessly inferior?
- Interesting question: How well can one do in such a technology if one tries very hard?
  - Scaling delivers faster devices every year; eventually, they'll be fast enough.
  - Is the substrate really so big a problem that good inductors (and capacitors) simply cannot be realized?
  - Is device noise so large that CMOS LNAs will always be HNAs?
  - Does the inferior 1/f noise of CMOS transistors doom the close-in phase noise performance of oscillators?
- Can you *really* build credible RF ICs in standard digital CMOS?

Outline

- A few brief words on scaling trends
- The patterned ground shield spiral inductor
- Capacitors
  - Fractal capacitors
  - Accumulation mode varactors
- Passive mixers
- Broadband noise models for the deep submicron regime
- Power-constrained LNA design
- A new phase noise theory and its implications for 1/f noise upconversion
- Putting it all together: A 115mW single chip GPS receiver in 0.5μm CMOS

Scaling Trends in Brief

- CMOS f_T (and f_{max}) are in the range of 30GHz now, and double roughly every three years.
- Devices with ~75nm L_{eff} have been demonstrated, and exhibit ~150GHz f_T!
- CMOS suffers from large source/drain parasitics, compared with other technologies.
  - Gate-drain "overlap" capacitance is also large.
- Series gate resistance is also an increasingly serious problem as gate lengths continue to shrink, but can be accommodated by using narrower unit devices.
  - Salicided gates help, too.
- Interconnect layers increasing at ~0.75 to 1 level per generation (5 layers are now relatively common).

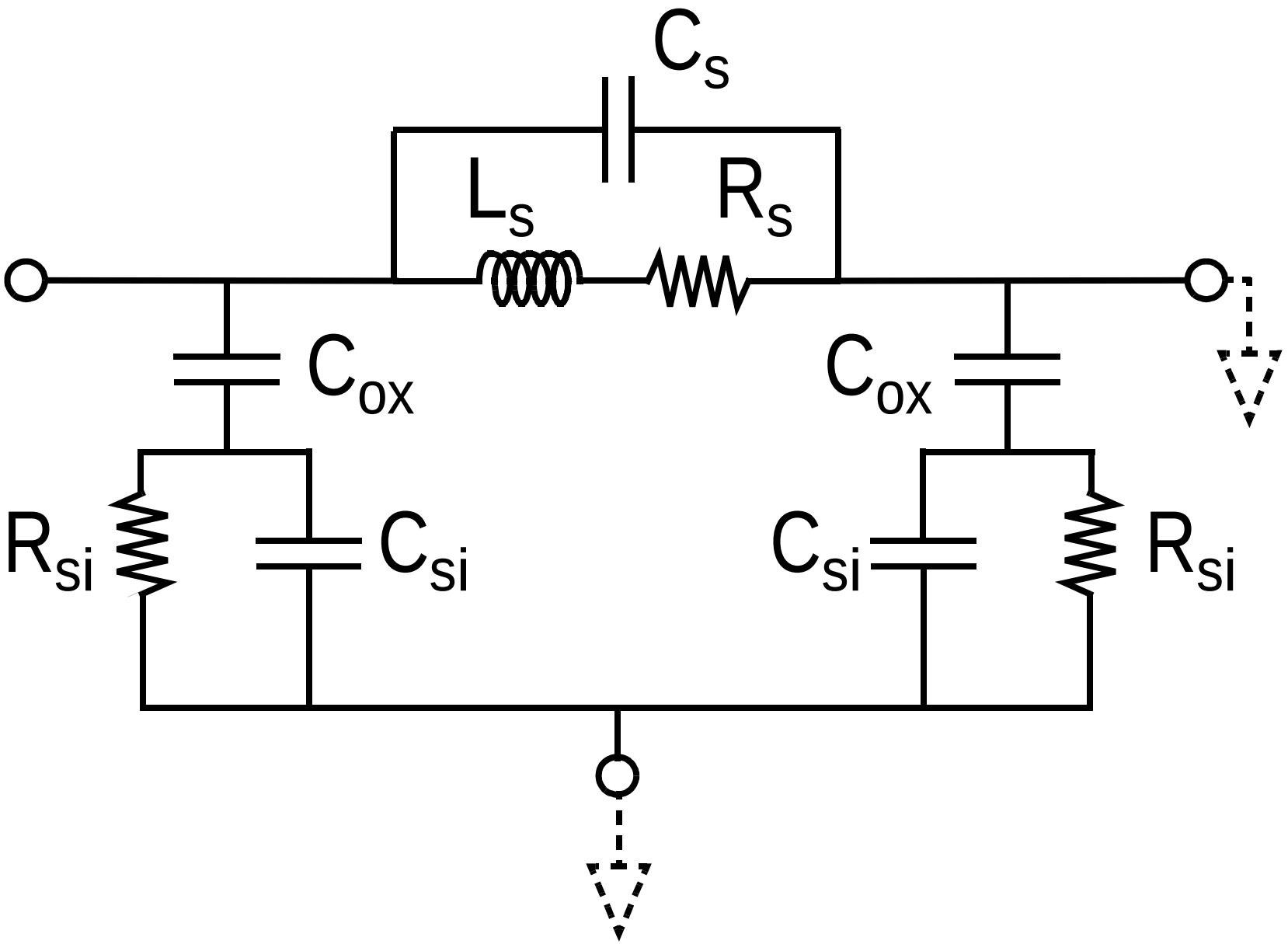
Passive Elements: Planar Spiral Inductors

- Planar spirals in Si technology are infamous for poor Q (typically well below 10).
- Conductor resistance, exacerbated by skin and proximity effects, typically accounts for about half the loss.
  - Applies to both bulk and epi technologies.
- The remaining loss is primarily due to currents flowing in the substrate.
  - Getting rid of the substrate would work wonders (e.g., post-fab etch, SOA, etc.), but requires deviation from ordinary process technology.
  - Next-best choice is to use a high-resistivity substrate, but can't do so without sacrificing other CMOS characteristics.
  - Next next-best choice is to construct a *pseudo-substrate* out of existing interconnect layers.

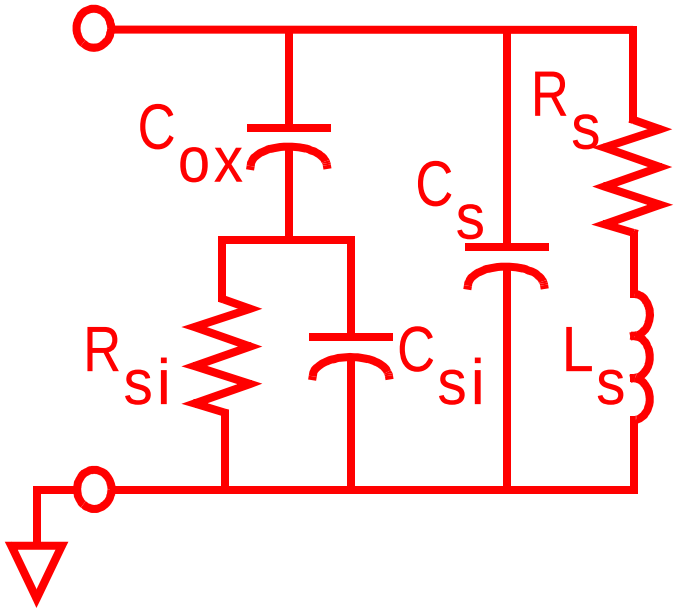
Passive Elements: Planar Spiral Inductors

- Most of the substrate loss is *not* due to the flow of magnetically induced eddy currents, contrary to widespread superstition.
- Main mechanism is simply current flow into the substrate through the parasitic capacitance between inductor and substrate.
- Grounded shield interposed between inductor and substrate diverts this current into ground.
  - Slots cut into ground shield prevent loss in shield due to eddy currents.
  - Drawback is a reduction in self-resonant frequency due to increase in parasitic capacitance (can mitigate this by using higher-level metal layers).

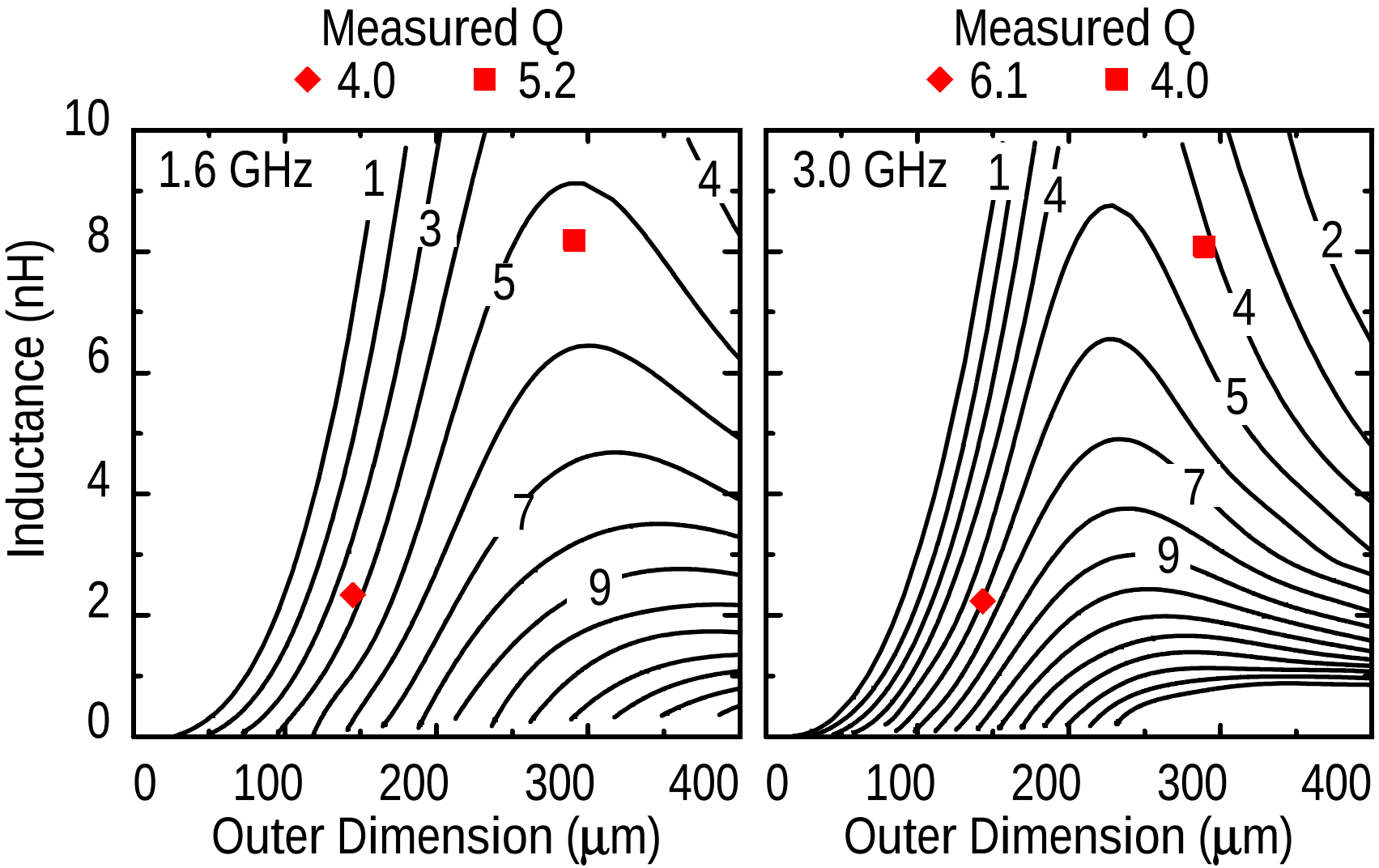
Model Description



Model Description

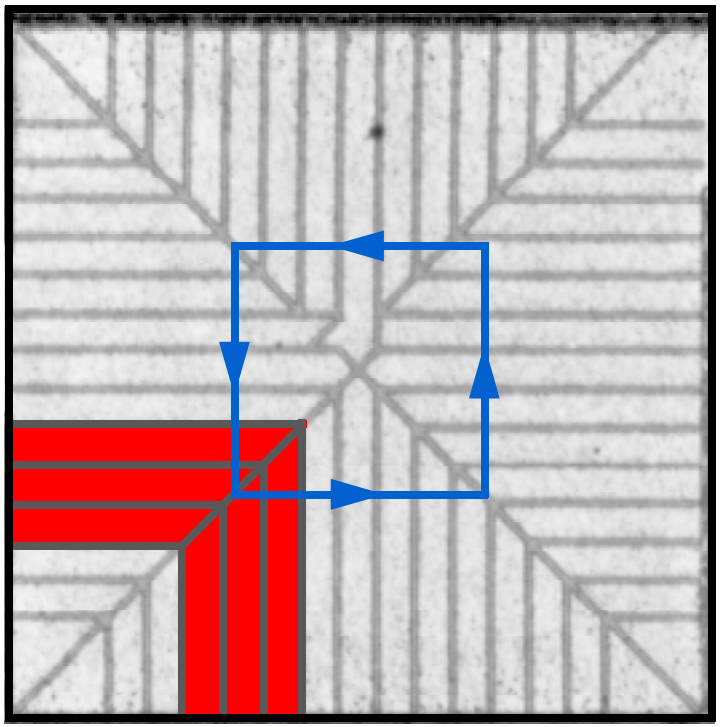
Physical Model of Inductor on Silicon		Effects
	L_s: Greenhouse Method	Mutual Couplings
	$R_s = \frac{\rho \cdot l}{w \cdot \delta \cdot (1 - e^{-t/\delta})}$	Eddy Current
	$C_s = n \cdot w^2 \cdot \frac{\varepsilon_{ox}}{t_{ox\ M1\text{-}M2}}$	Feed-Through Capacitance
	$C_{ox} = \frac{1}{2} \cdot l \cdot w \cdot \frac{\varepsilon_{ox}}{t_{ox}}$	Oxide Capacitance
	$C_{si} = \frac{1}{2} \cdot l \cdot w \cdot C_{Sub}$	Si Substrate Capacitance
	$R_{si} = \frac{2}{l \cdot w \cdot G_{Sub}}$	Si Substrate Ohmic Loss

Contour Plots of Q



Patterned Ground Shield Design

- Pattern
  - Orthogonal to spiral (induced loop current)
- Resistance
  - Low for termination of the electric field
  - Avoid attenuation of the magnetic field

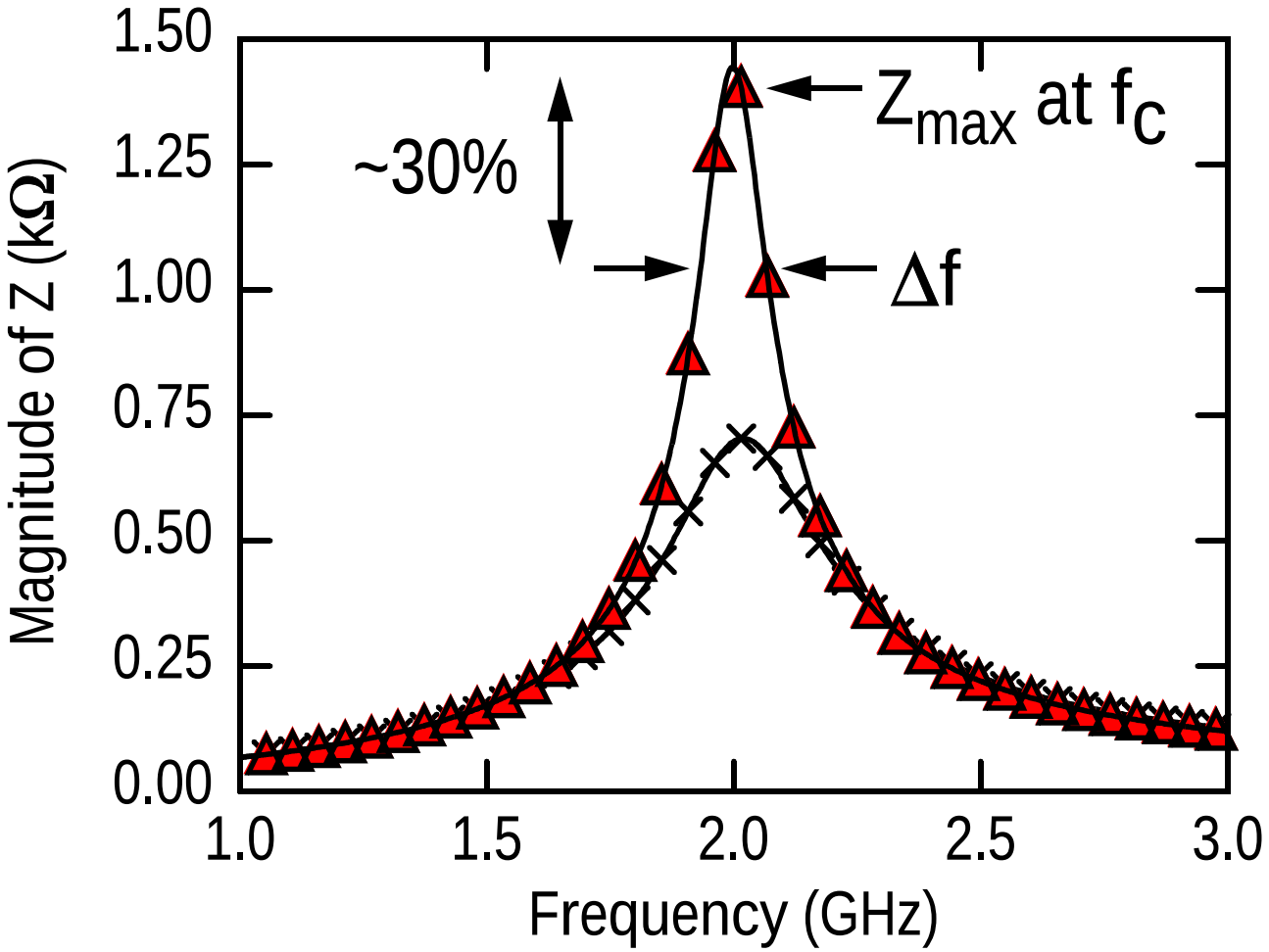


Ground Strips

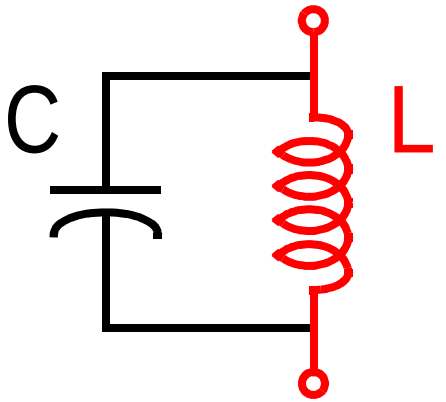
Slot between Strips

Induced Loop Current

Parallel LC Resonator at 2 GHz



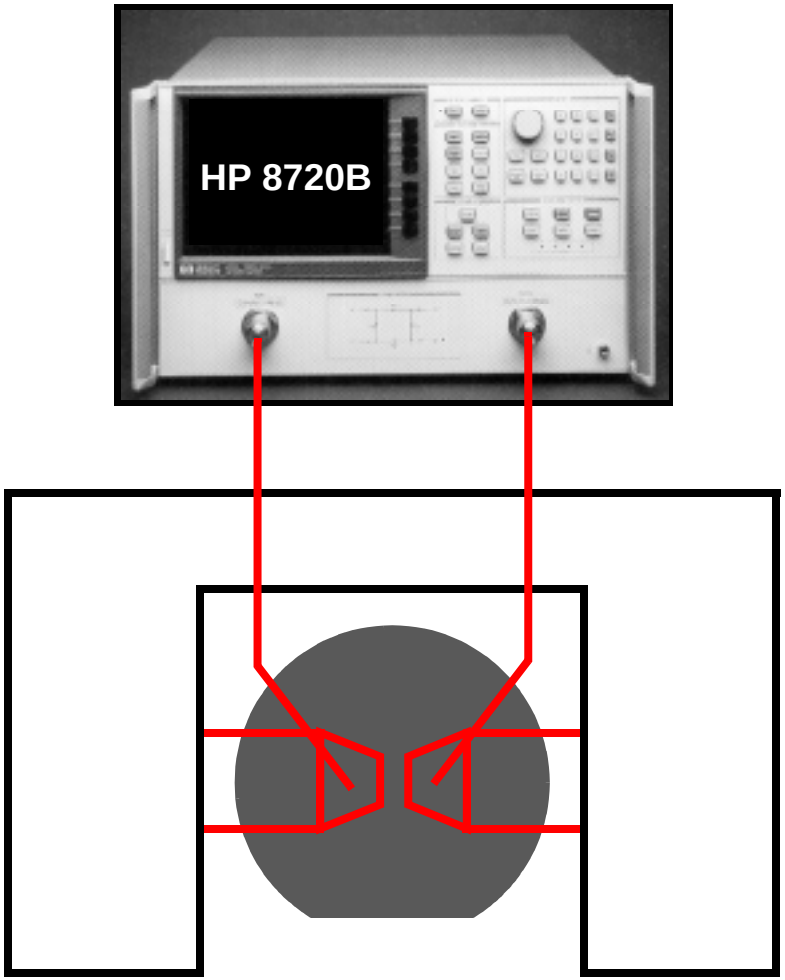
$$Q_{RESONATOR} = \frac{f_C}{\Delta f}$$



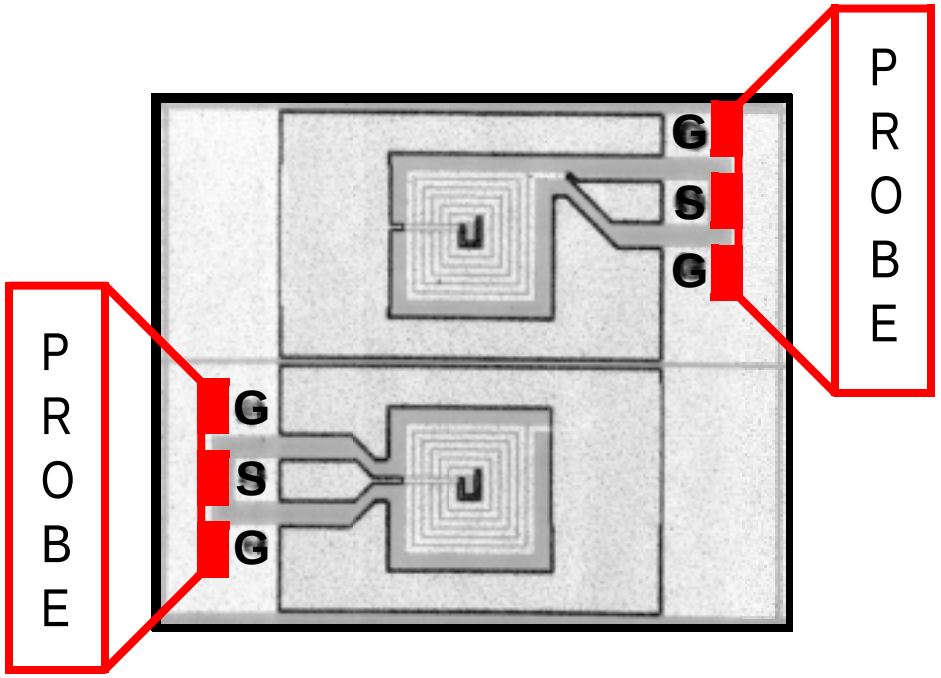
Patterned Polysilicon

None (11 Ω-cm)

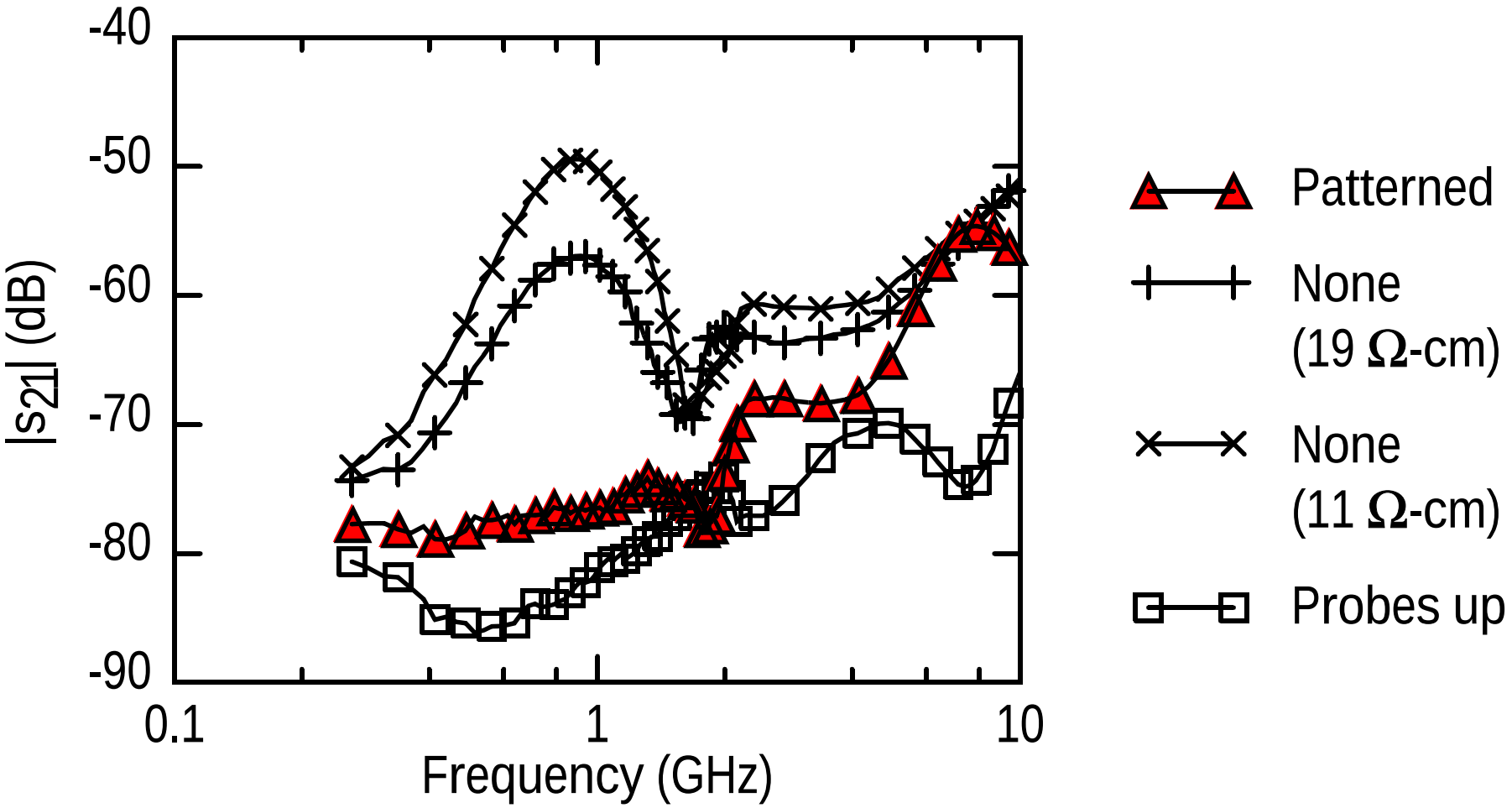
Noise Coupling Measurement



Probe Station



Effect of Polysilicon GS on Isolation

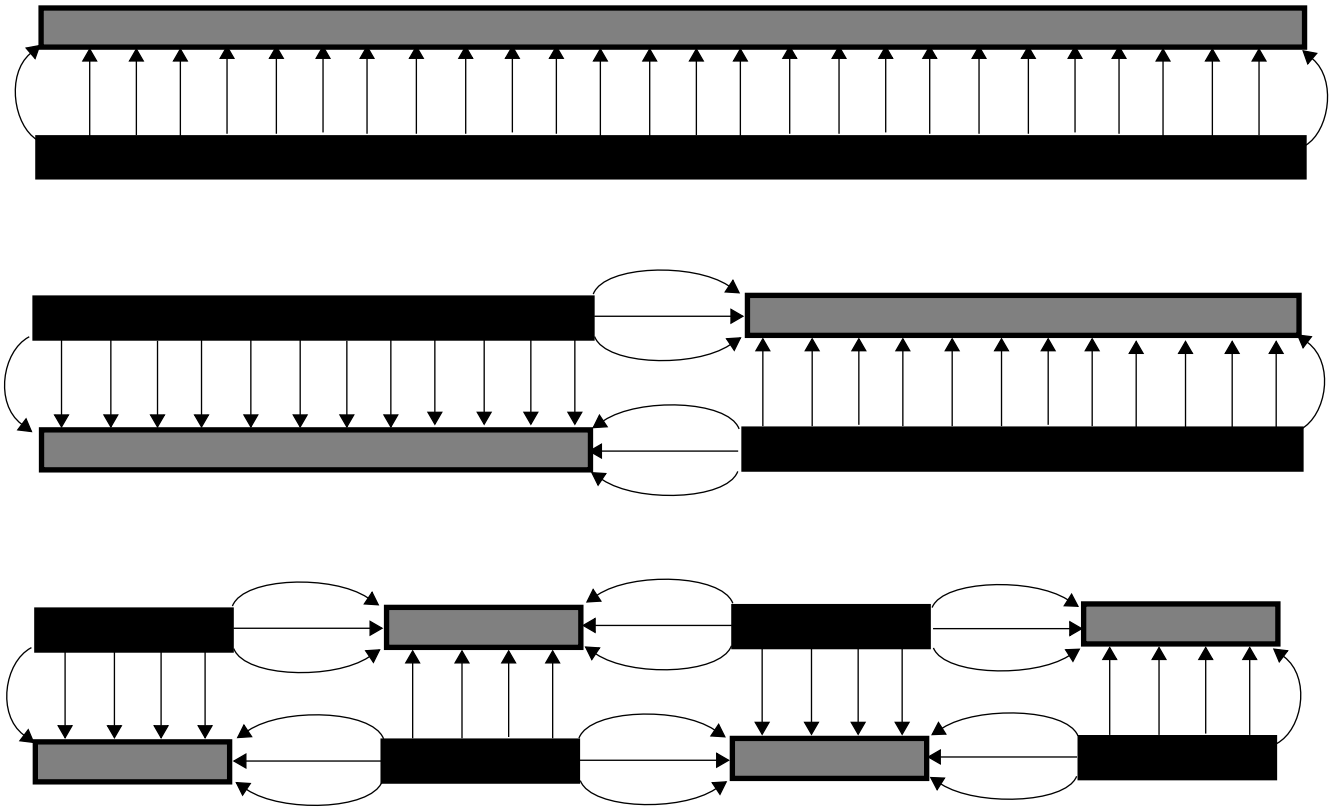


Passive Elements: Capacitors

- Ordinary parallel plate structures don't scale with technology because the vertical spacing is held roughly constant to keep interconnect capacitance small.
- Bottom-plate parasitics are large (e.g., 30% of main capacitance).
- Gate capacitors are area efficient, but impose bias constraints, and are not as linear as MIM structures.
- Traditional varactor options (e.g., p+ in n-well) have poor Q
  - Gate capacitors in accumulation-mode are an attractive alternative (Q values in excess of 100 at 1GHz are potentially realizable)

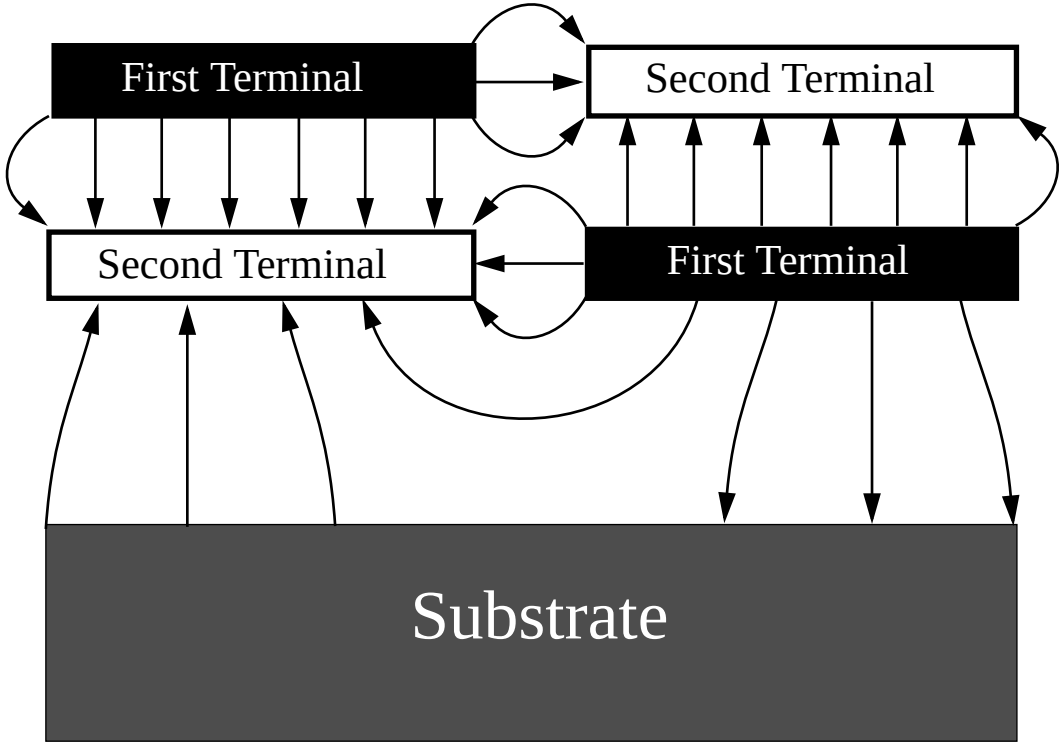
Vertical vs. Lateral Flux

- Lateral flux increases the total amount of capacitance.

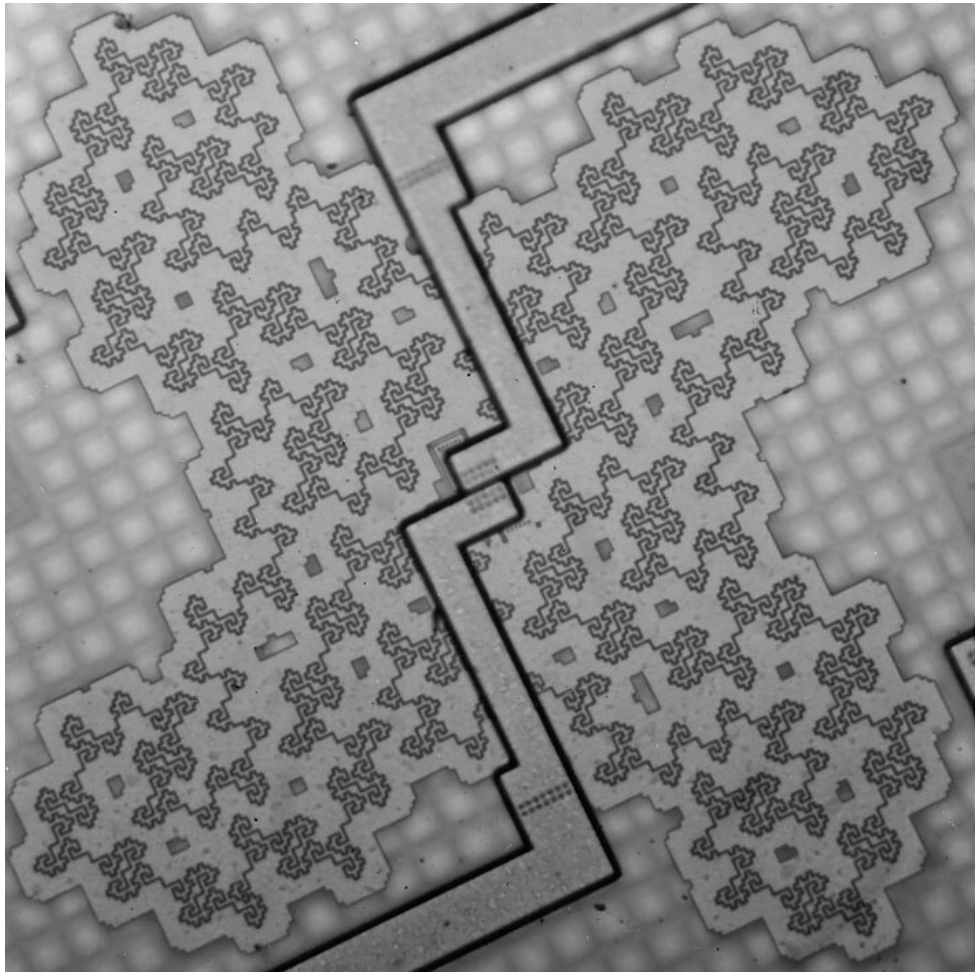


Reduction of the Bottom-Plate Capacitance

- Area is smaller.
- Some of the field lines terminate on the adjacent plate instead of the substrate.



Die Micrograph

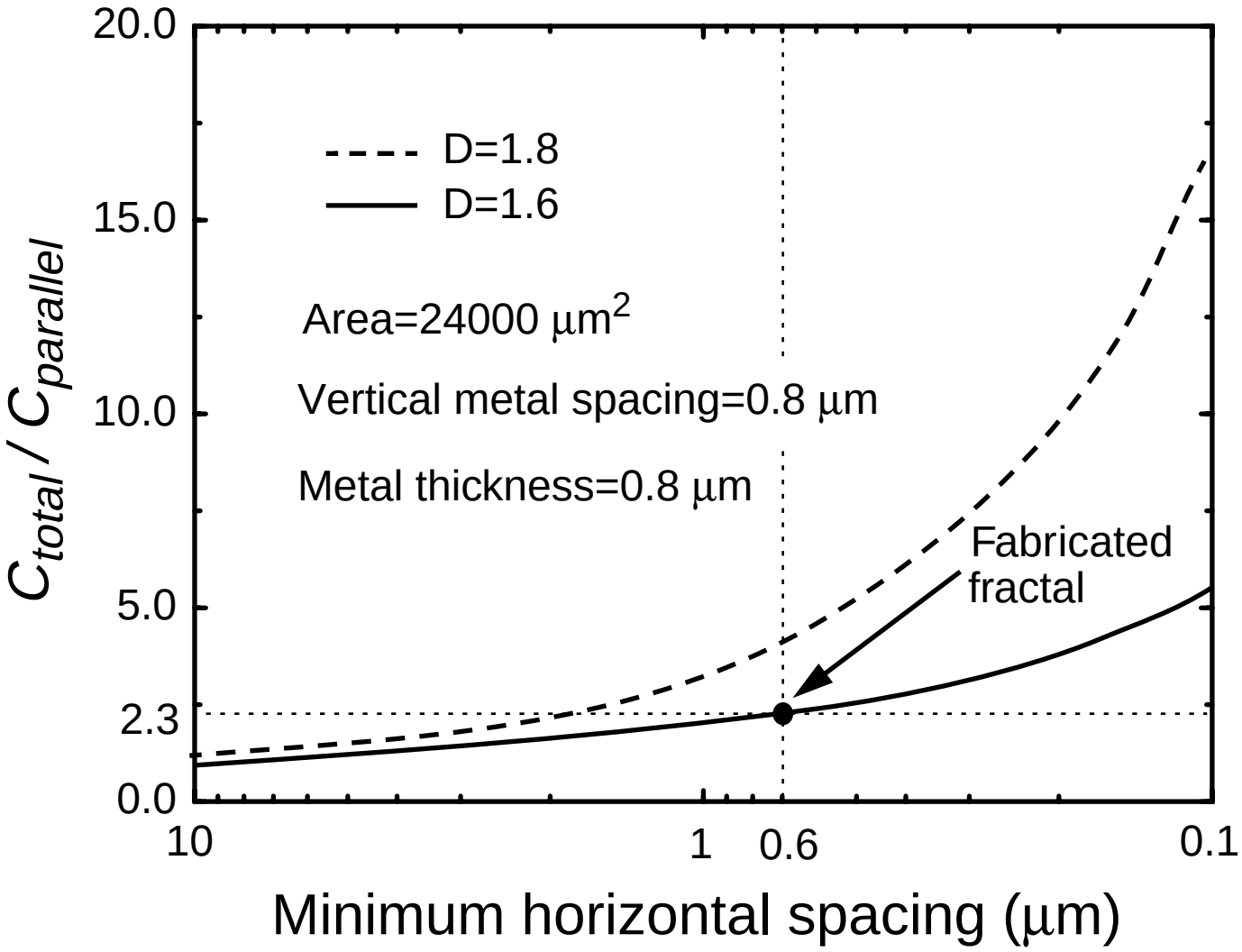


Horizontal spacing=0.6 μm

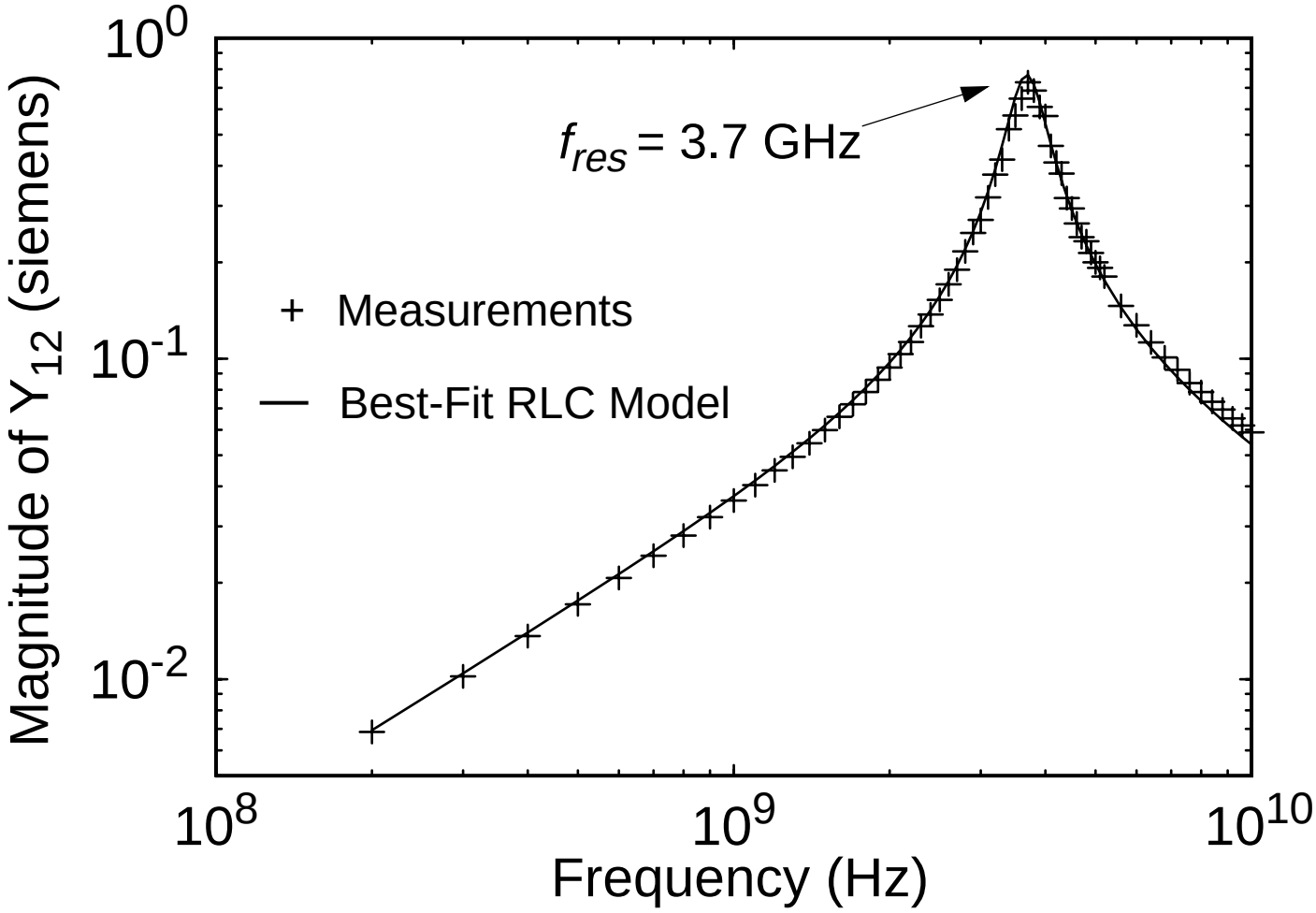
Vertical spacing=0.8μm

Area=24,000 μm^2

Boost Factor *vs.* Lateral Spacing

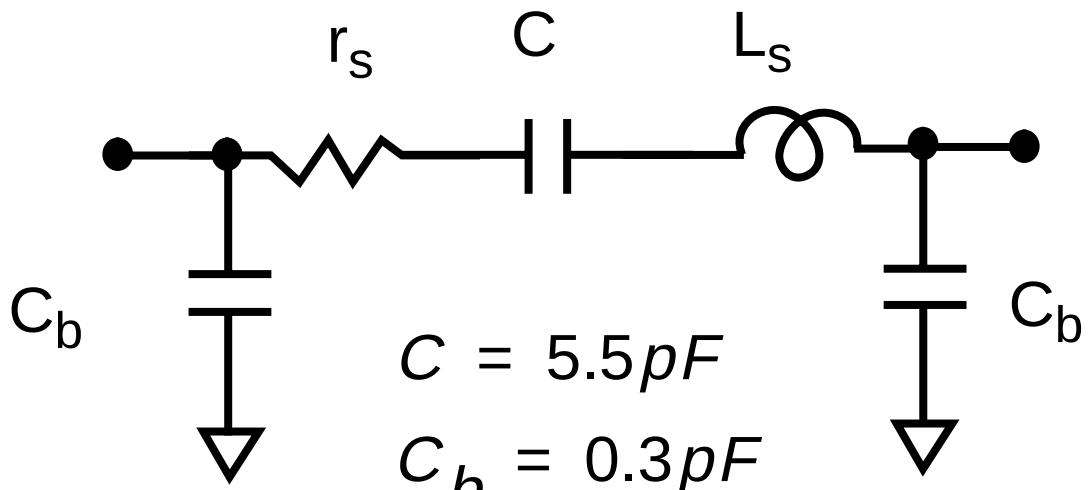


Measurements



High-frequency two-port measurements

Measurements



$C = 5.5pF$

$C_b = 0.3pF$

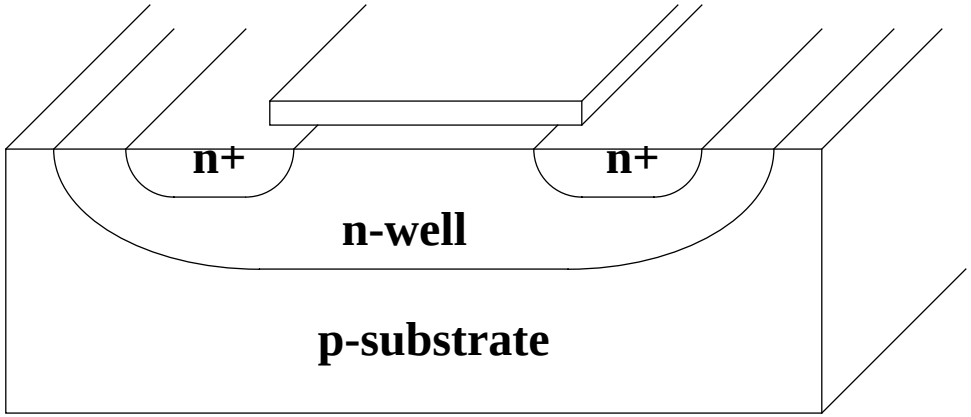
$L_s = 0.34nH$

$r_s = 1.3\Omega$

Best-Fit Parameters

Passive Elements: Capacitors

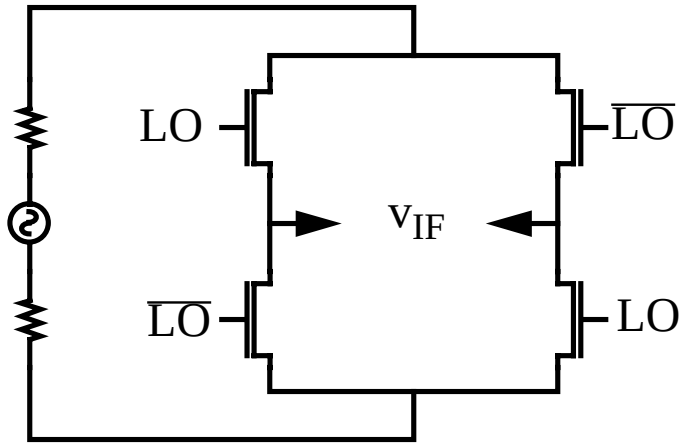
- **Accumulation-mode varactor (ref. Soorapanth et al., VLSI Circuits Symposium, June 1998):**



- **Compatible with standard CMOS processing**
- **Practical capacitance range exceeds 150%**

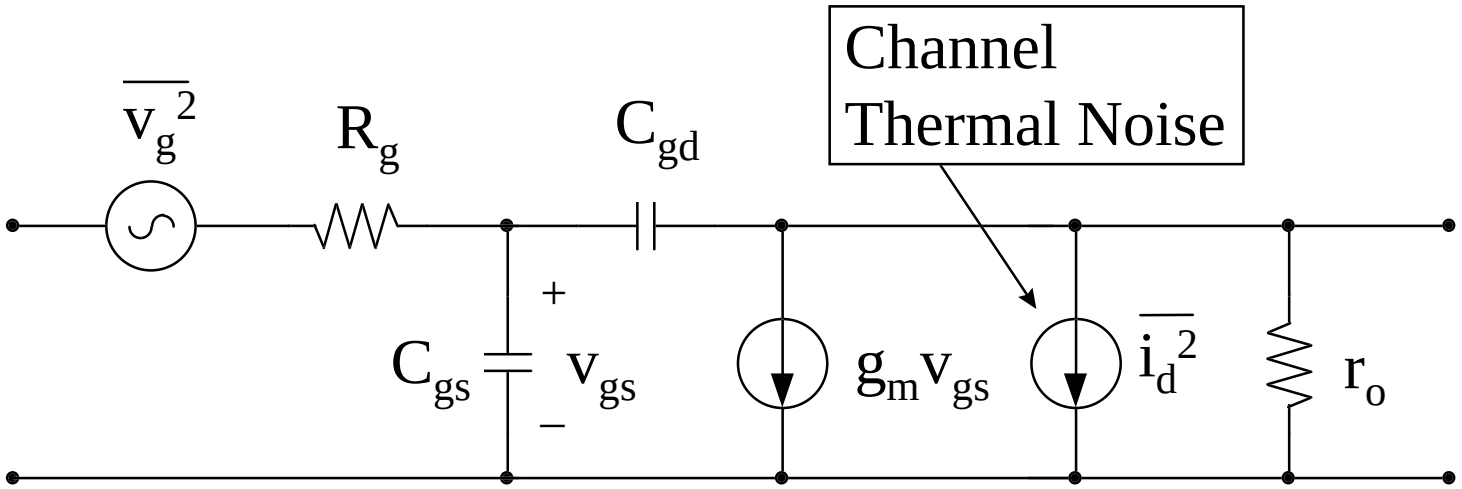
Passive Mixers

- Gilbert multiplier performs mixing in current domain because bipolar transistors are not good voltage switches.
  - Penalty: V-I conversion costs power and linearity
- CMOS voltage switches are excellent, so mixers made out of them work well:



- @1.6GHz: 3.6dB loss, +10dBm IIP3 achieved at 200μW

Simple CMOS Noise Model



- Channel thermal noise is dominant.

$$\overline{i_d^2} = 4kTB\gamma g_{d0}$$

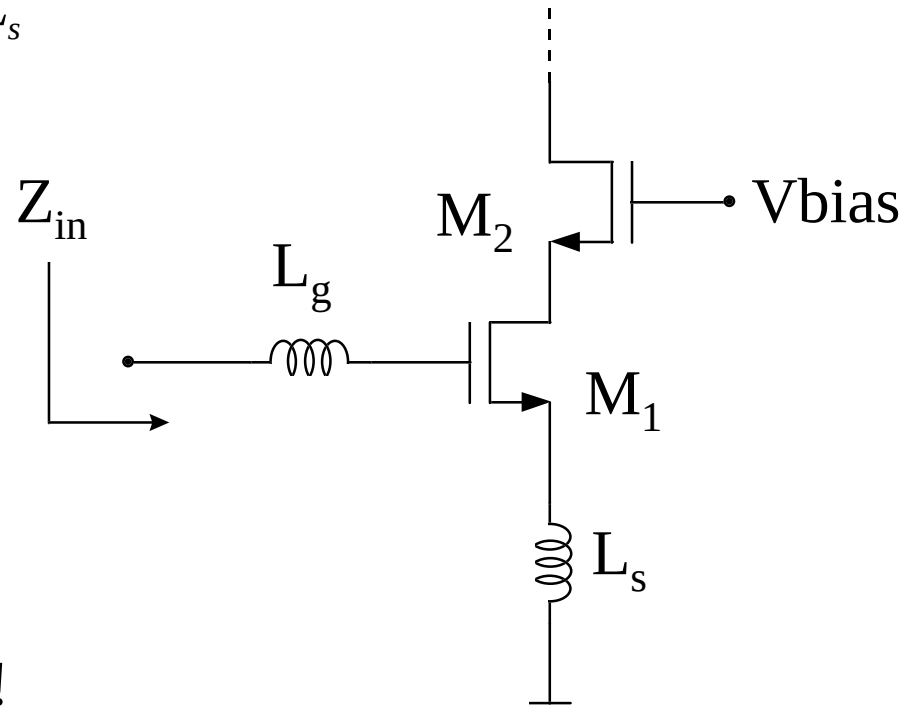
- Gate resistance minimized by good layout.

LNA Input Stage

$$Z_{in} = s\left(L_s + L_g\right) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \approx \omega_T L_s$$

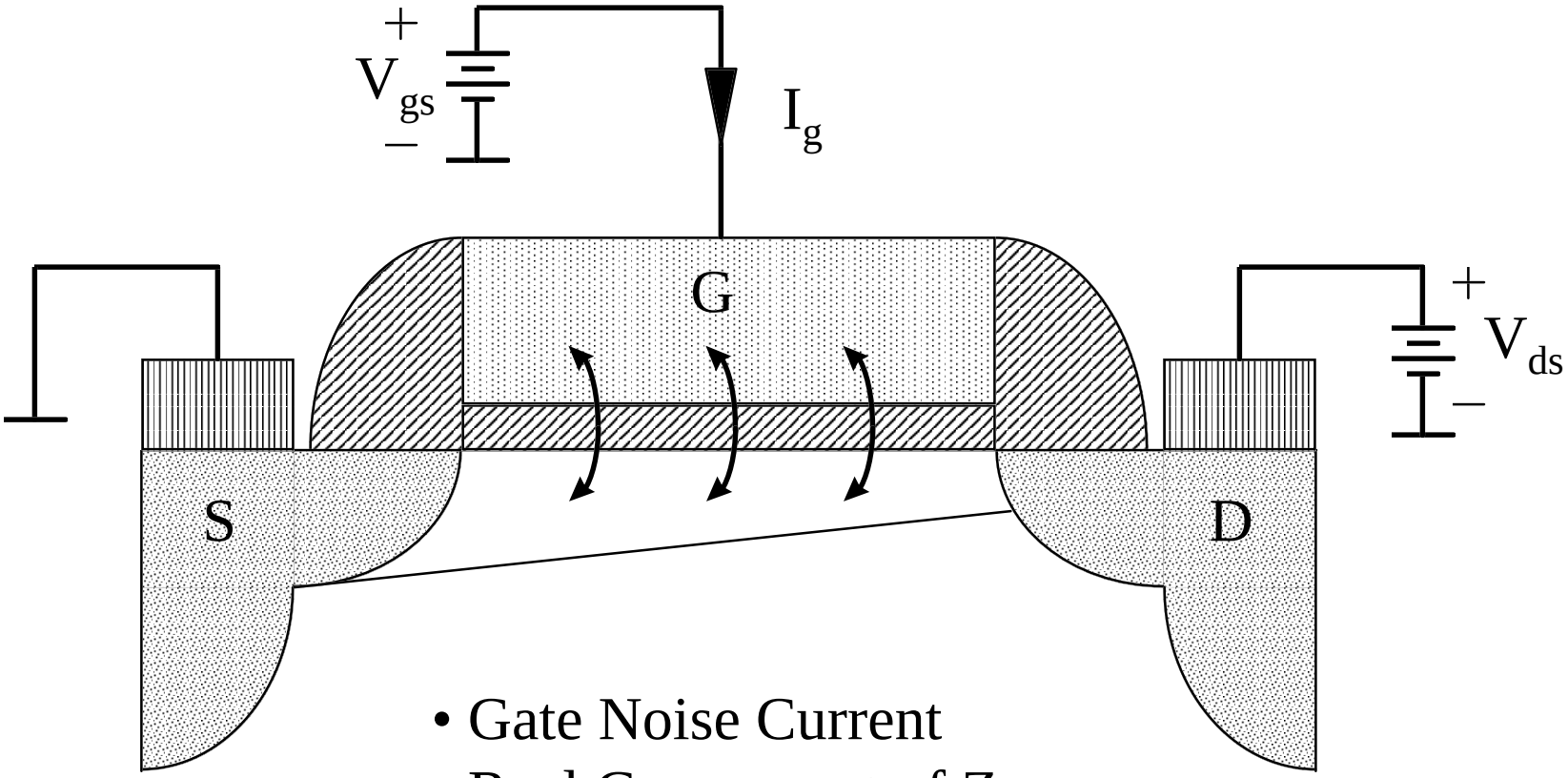
$$G_{m,eff} = g_{m1}Q_{in} = \frac{g_{m1}}{\omega C_{gs}\left(R_s + \omega_T L_s\right)}$$

$$= \frac{\omega_T}{\omega R_s\left(1 + \frac{\omega_T L_s}{R_s}\right)} = \frac{\omega_T}{2\omega R_s}$$



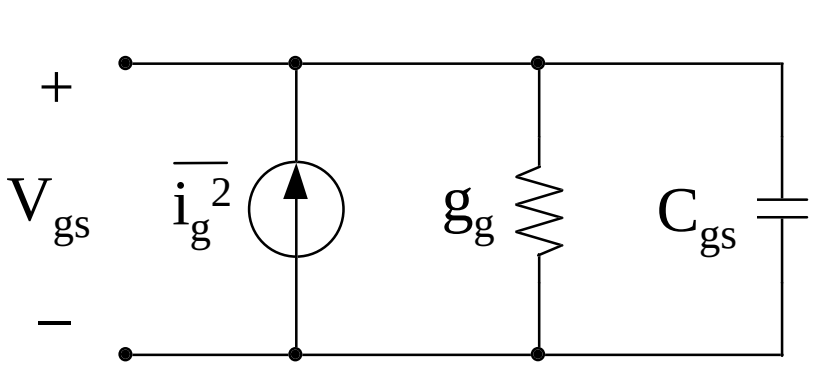
Note: $G_{m,eff}$ is <u>independent</u> of g_{m1}!

Induced Gate Effects

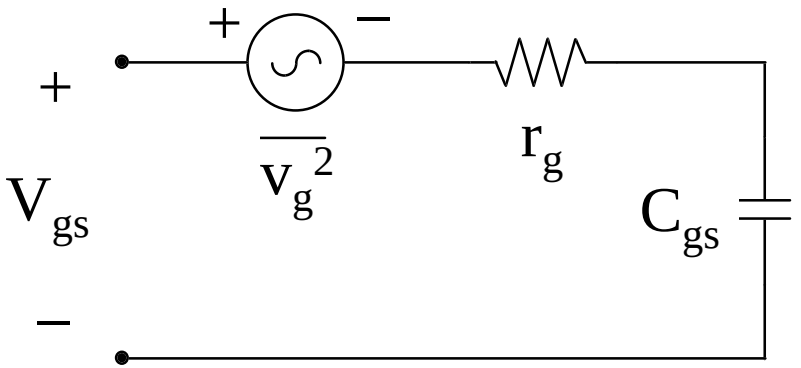


- Gate Noise Current
- Real Component of Z_g

Equivalent Gate Circuit



-OR-



$$\overline{i_g^2} = 4kTB\delta g_g \qquad g_g = \frac{1}{5}\frac{\omega^2 C_{gs}^2}{g_{d0}}$$

"Blue" Noise

$$\overline{v_g^2} = 4kTB\delta r_g \qquad r_g = \frac{1}{5g_{d0}}$$

"White" Noise

- δ (~ 4/3) modified by hot electron effects
- $\overline{i_g^2}$ partially correlated with $\overline{i_d^2}$ (c = 0.395j)
- $\overline{i_g^2}$ and g_g not modeled in HSPICE

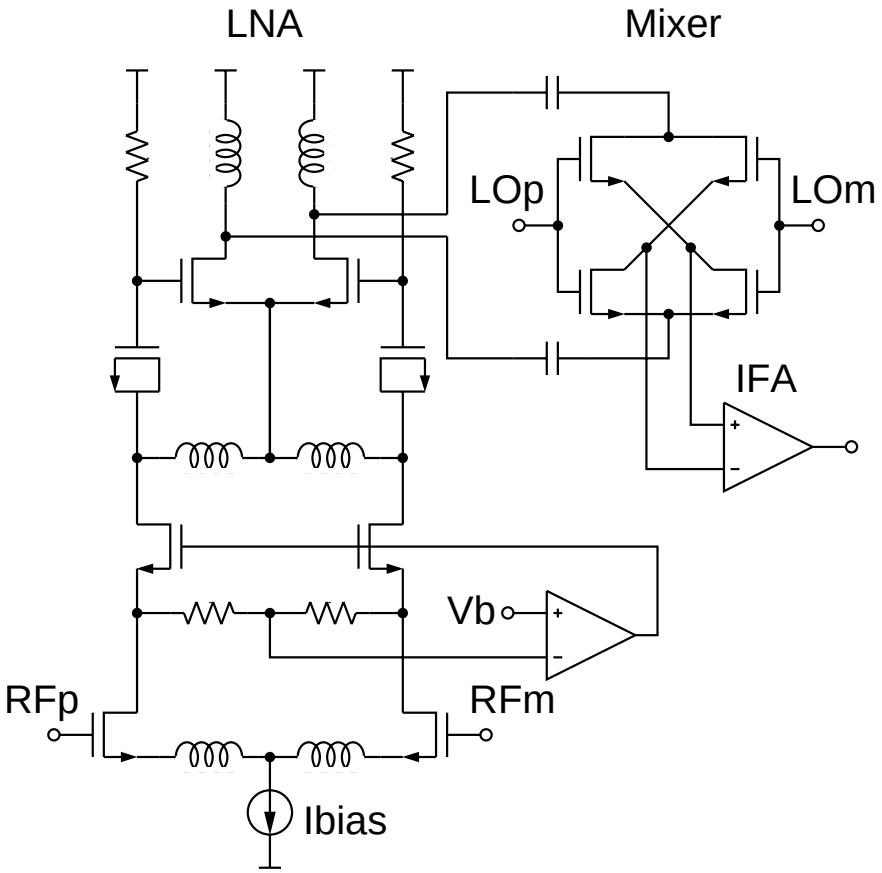
LNA Design Procedure

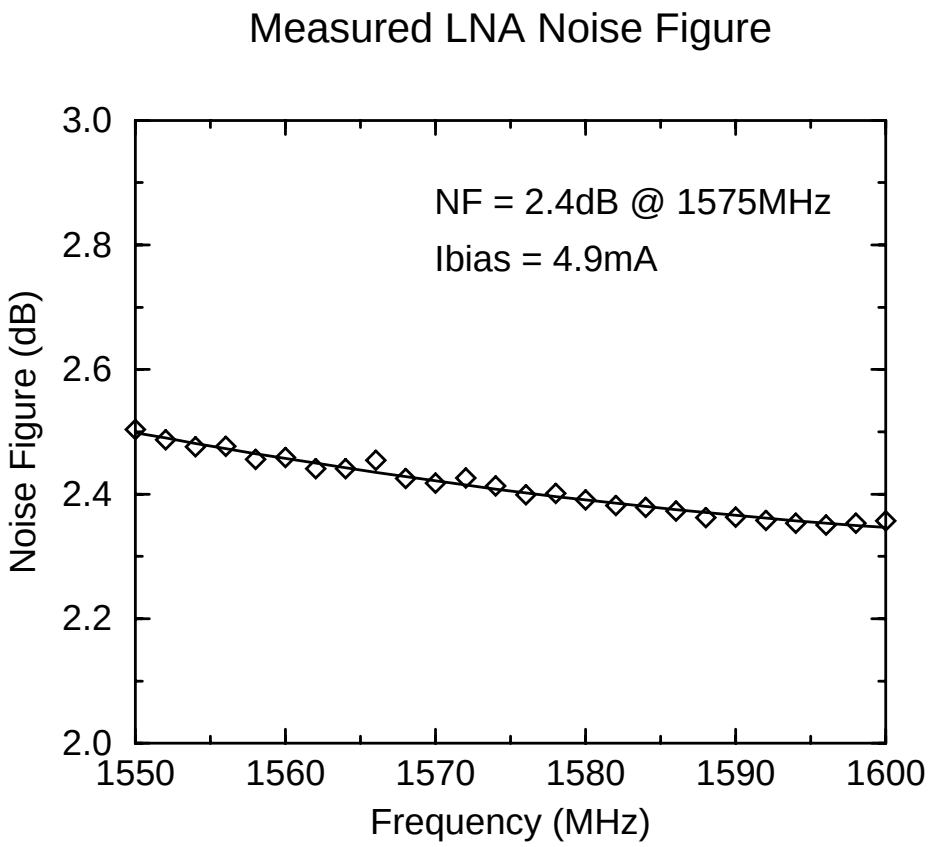
- **Select device width roughly equal to (500μm-GHz)/f_0** (for a 50Ω system)
- **Adjust bias to obtain desired power dissipation**
  - **Keep V_{DS}–V_{DSAT} as small as practical to minimize hot-electron effects (say, under half a volt or so)**
- **Select source degeneration inductance (assuming equal-sized cascoding and main devices) according to:**

$$L_S \approx \frac{R_S \cdot [1 + 2(C_{gd}/C_{gs})]}{\omega_T}$$

- **Add enough gate inductance to bring input to resonance**
- **Noise factor bound is $1 + 2.4(\gamma/\alpha)(\omega/\omega_T)$, so scaling continues to help directly**

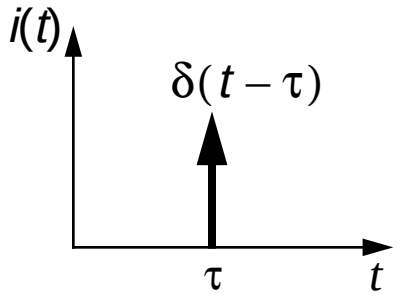
CIRCUITS: LNA / MIXER

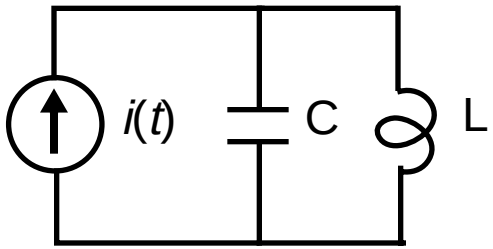


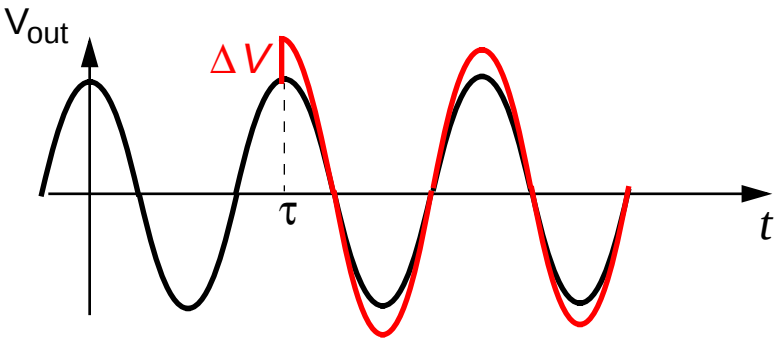


Shahani, Shaeffer and Lee, ”A 12mW Wide Dynamic Range CMOS GPS Receiver,” ISSCC 1997

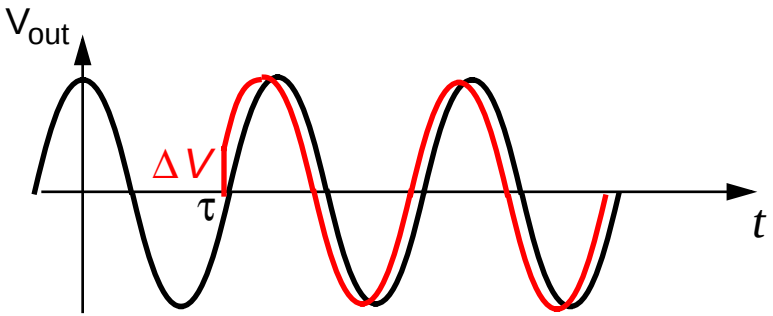
Oscillators Are Time-Variant Systems







Impulse injected at the peak of amplitude.



Impulse injected at zero crossing.

Even for an ideal LC oscillator, the phase response is *Time Variant.*

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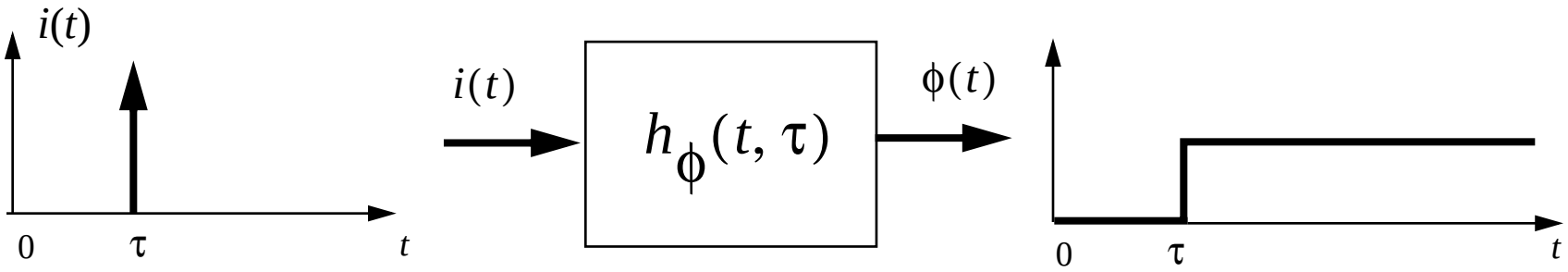
Phase Impulse Response

The phase impulse response of an arbitrary oscillator is a time varying step.



The unit impulse response is:

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_o \tau)}{q_{max}} u(t-\tau)$$

$\Gamma(x)$ is a dimensionless function periodic in 2π, describing how much phase change results from applying an impulse at time: $t = T\frac{x}{2\pi}$

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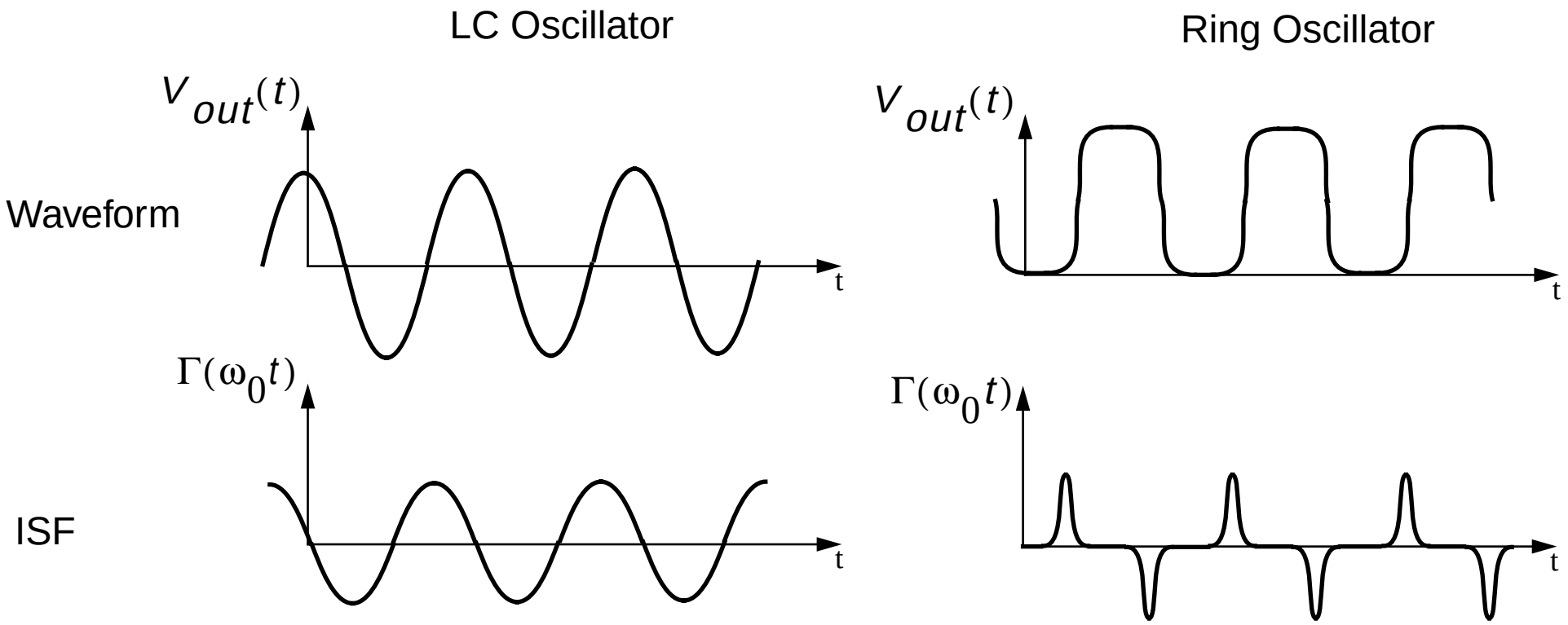
Impulse Sensitivity Function (ISF)



The ISF quantifies the sensitivity of every point in the waveform to perturbations.

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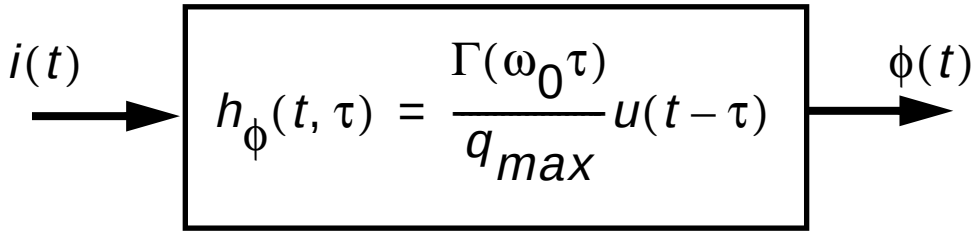
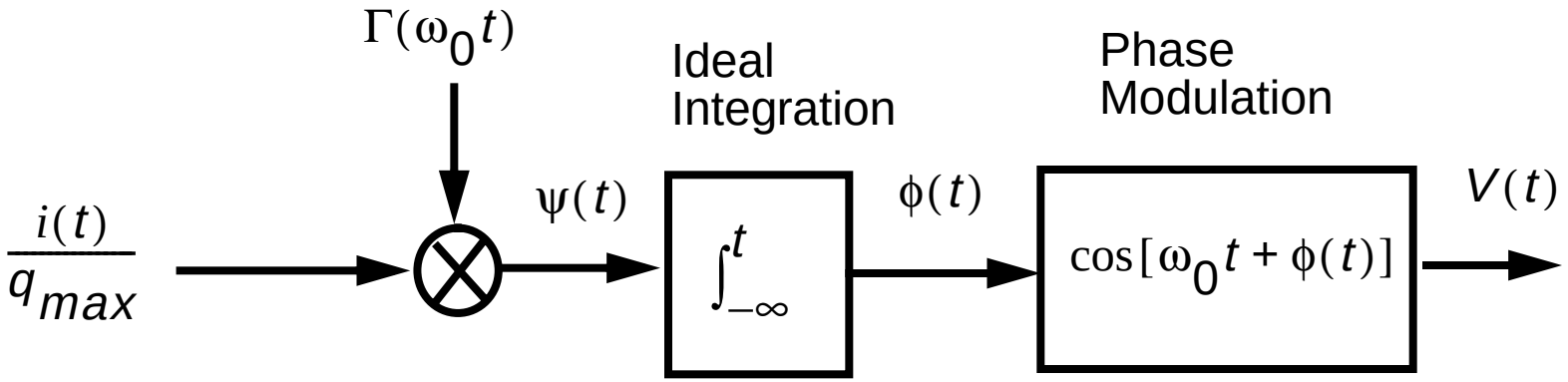
Phase Response to an Arbitrary Source



Superposition Integral:

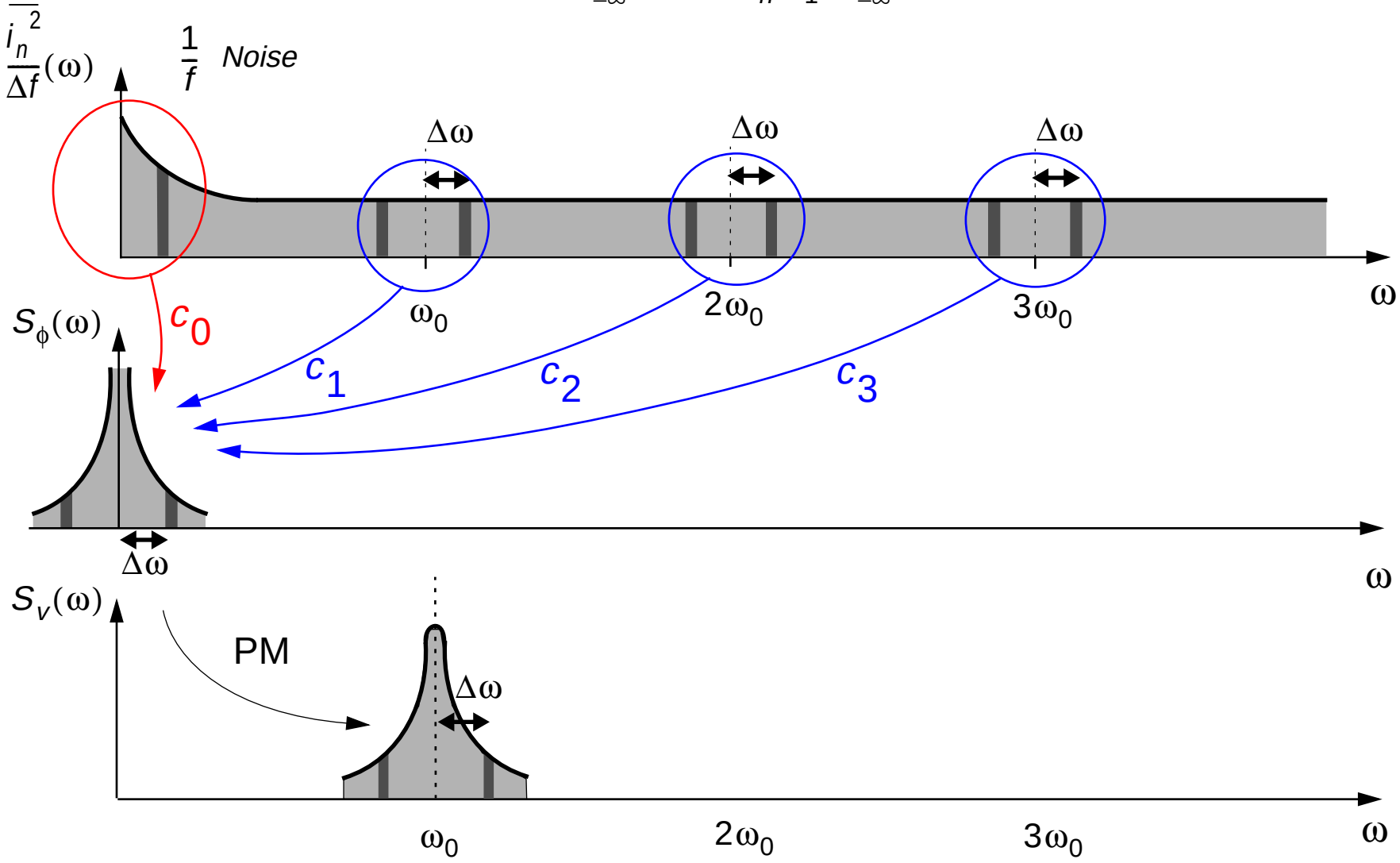
$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau) i(\tau) d\tau = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_0\tau) i(\tau) d\tau$$

Equivalent representation:



Noise Contributions from $n\omega_o$

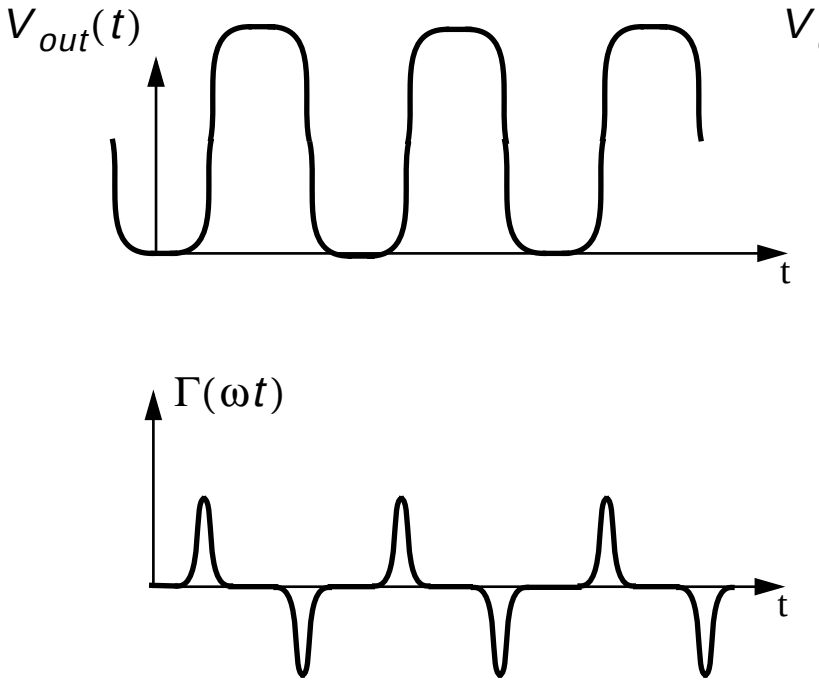
$$\phi(t) = \frac{1}{q_{max}}\left[c_0 \int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(n\omega\tau)d\tau\right]$$



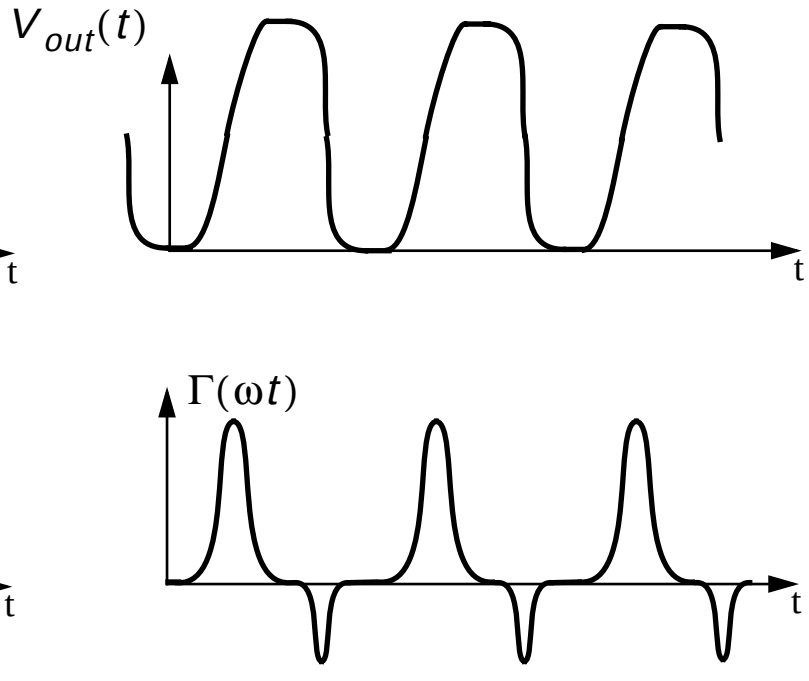
Effect of Symmetry

$$c_0 = \frac{1}{2\pi}\int_0^{2\pi} \Gamma(x)\,dx$$

Symmetric rise and fall time



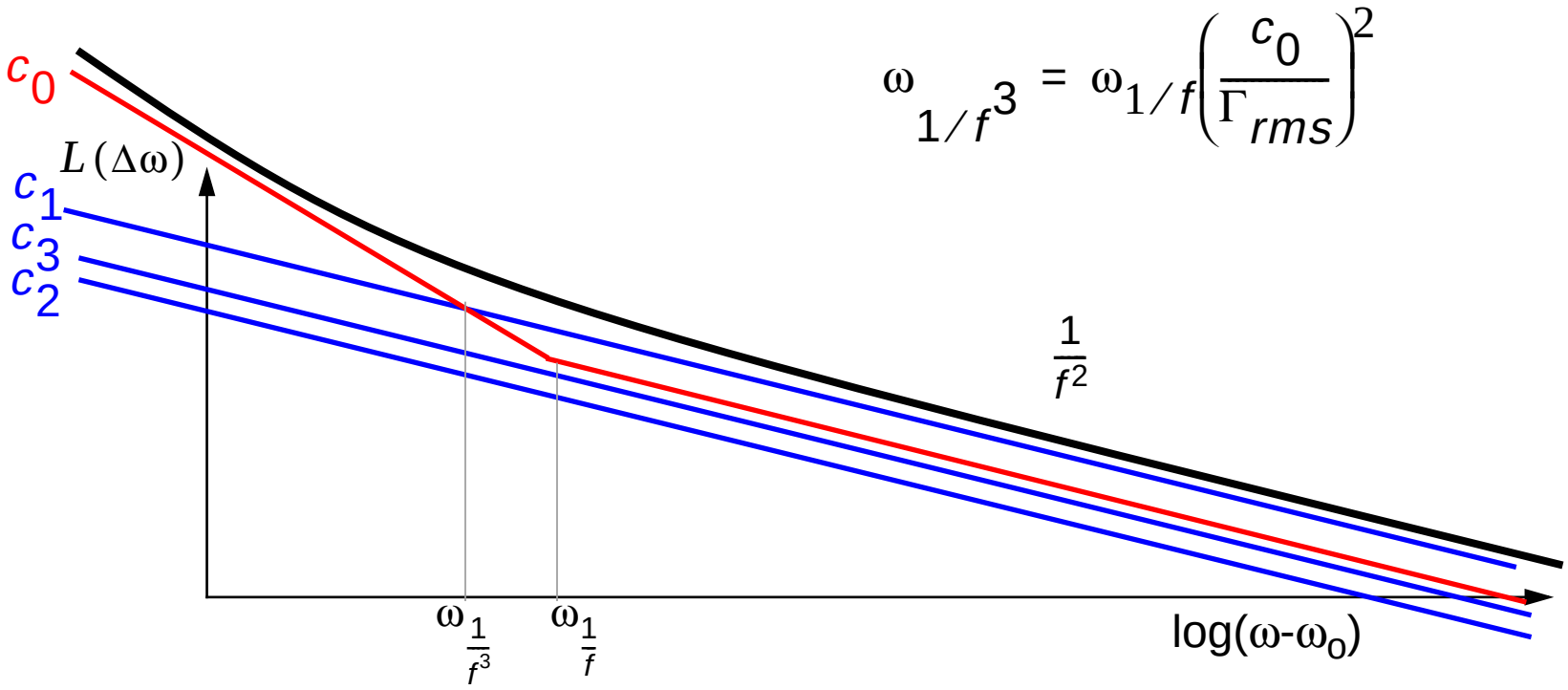
Asymmetric rise and fall time



The dc value of the ISF is governed by rise and fall time symmetry, and controls the contribution of low frequency noise to the phase noise.

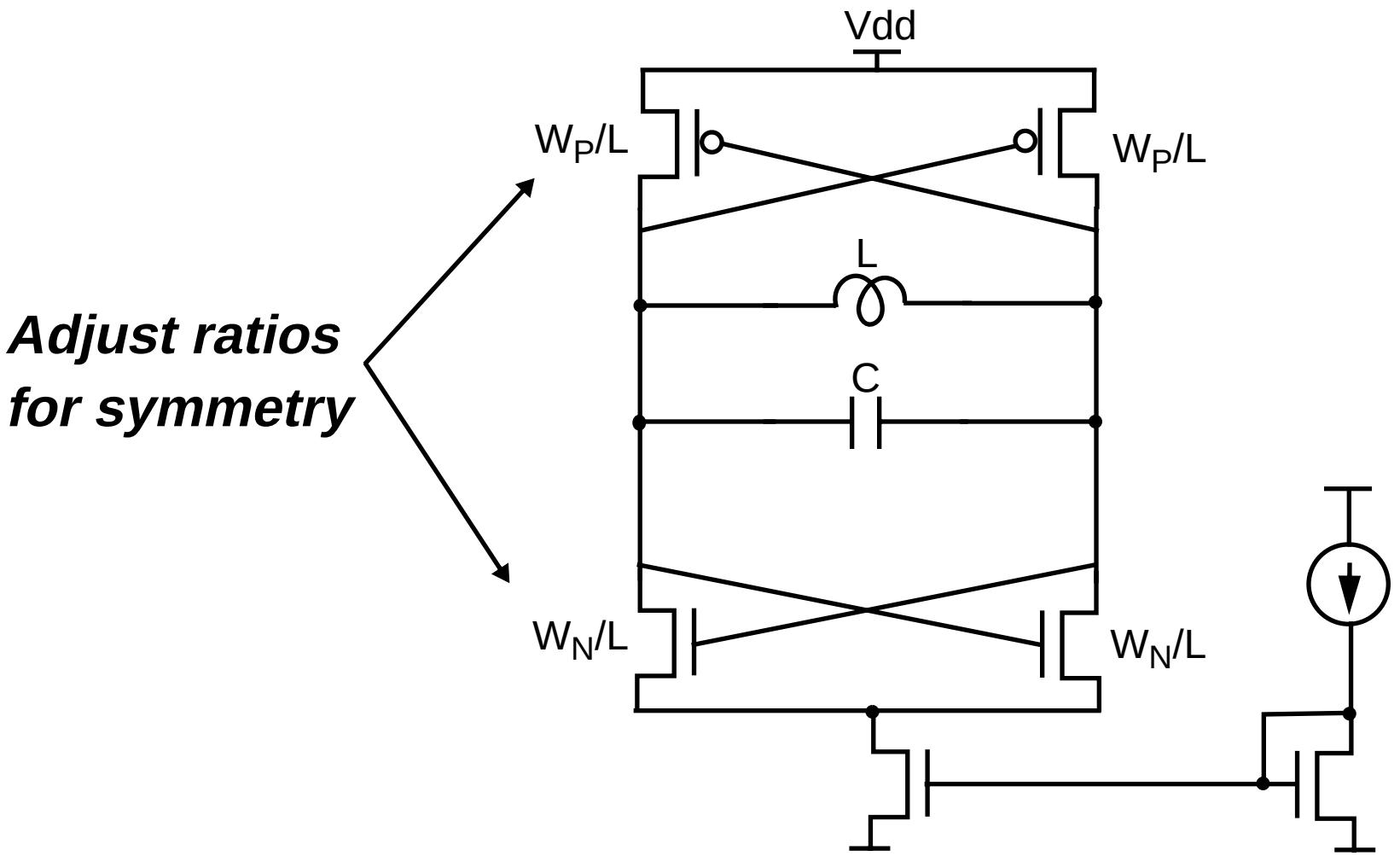
$1/f^3$ Corner of Phase Noise Spectrum

The $1/f^3$ corner of phase noise is NOT the same as 1/f corner of device noise



By designing for a symmetric waveform, the performance degradation due to low frequency noise can be minimized.

A Symmetric LC Oscillator



Possible to Adjust Symmetry Properties of the Waveform

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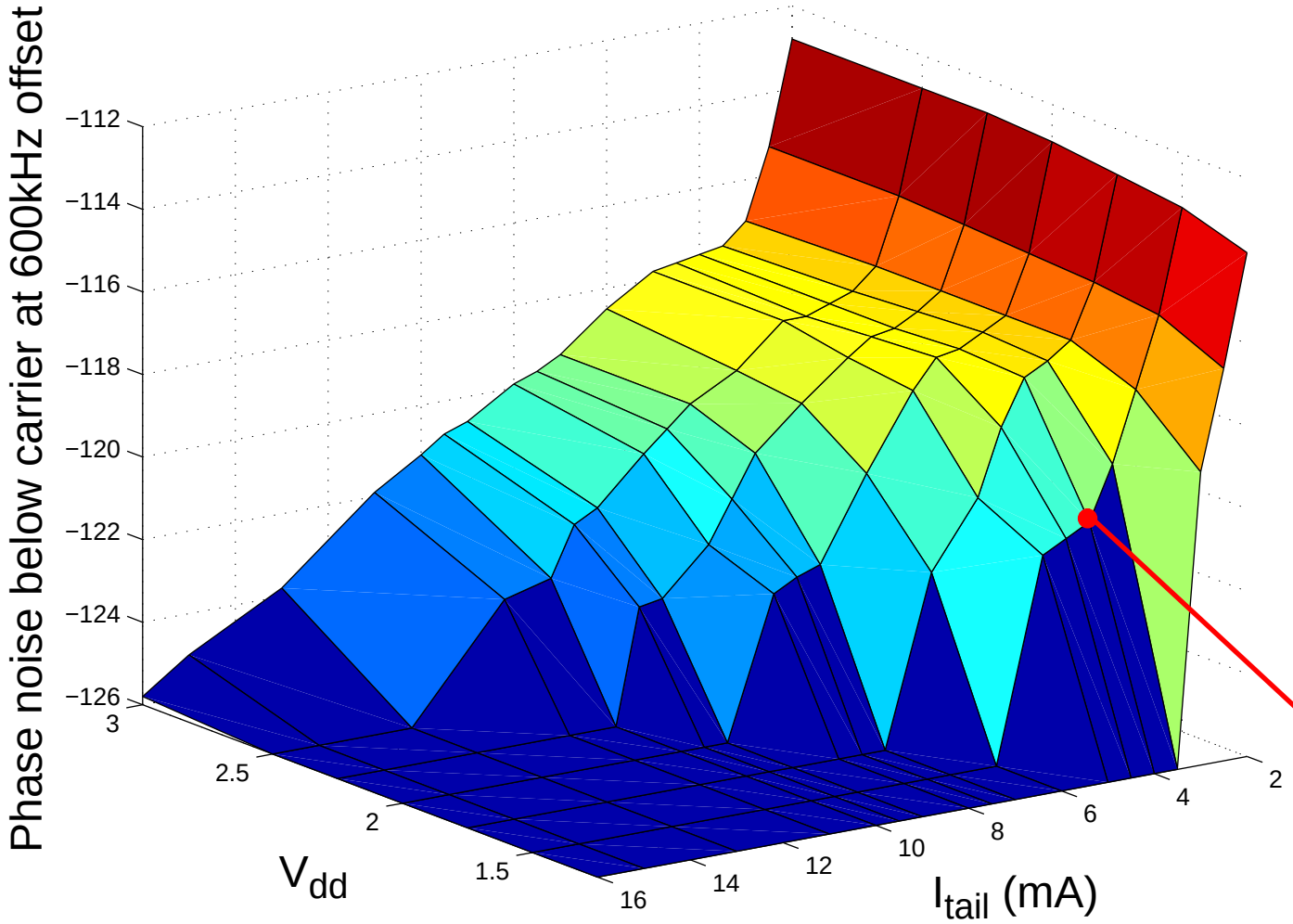
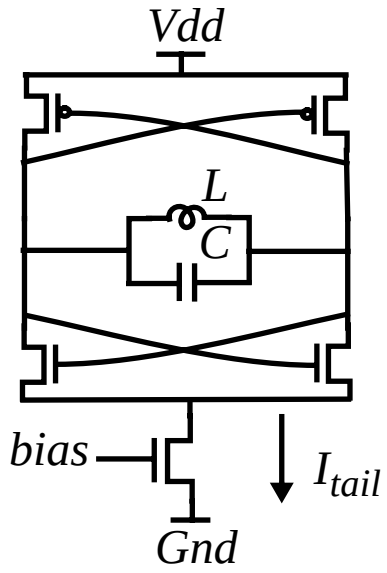
Complementary Cross-Coupled VCO

f_0=1.8GHz, 0.25µm Process



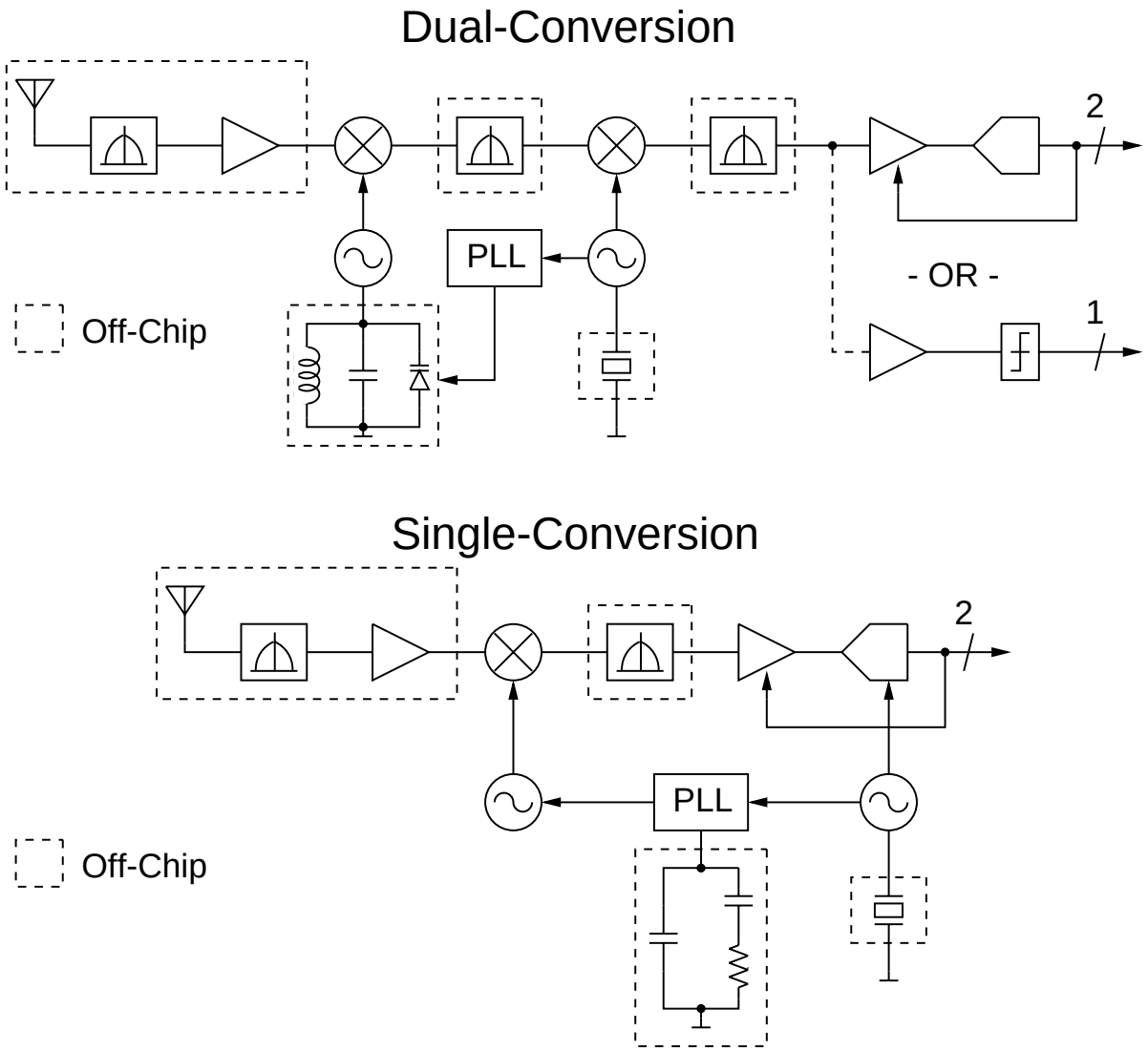


f_0=1.8GHz
P=6mW
-121dBc/Hz@600kHz

GPS Overview: Typical Receiver Architectures

Distinguishing Features:

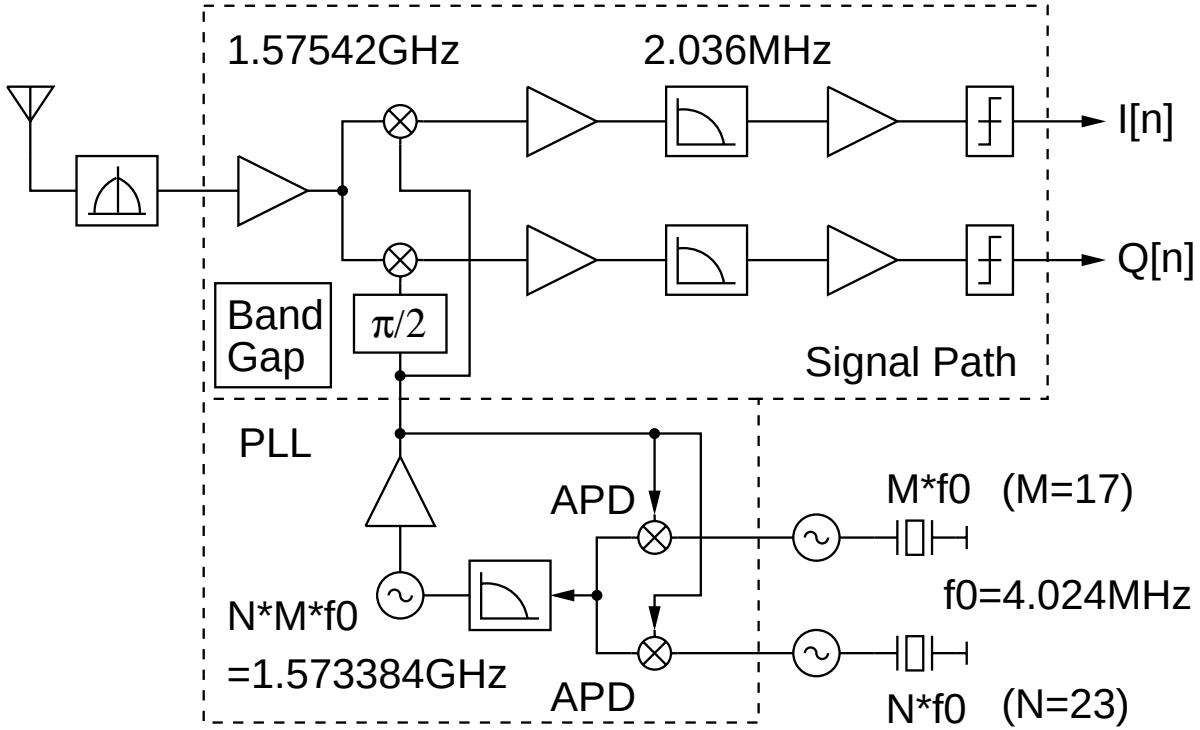
- Typical on-chip P_D is 100mW – 500mW
- Off-chip LNA or active antenna
- Off-chip IF filtering
- 1 or 2 bit quantization



ARCHITECTURE: LOW-IF RECEIVER

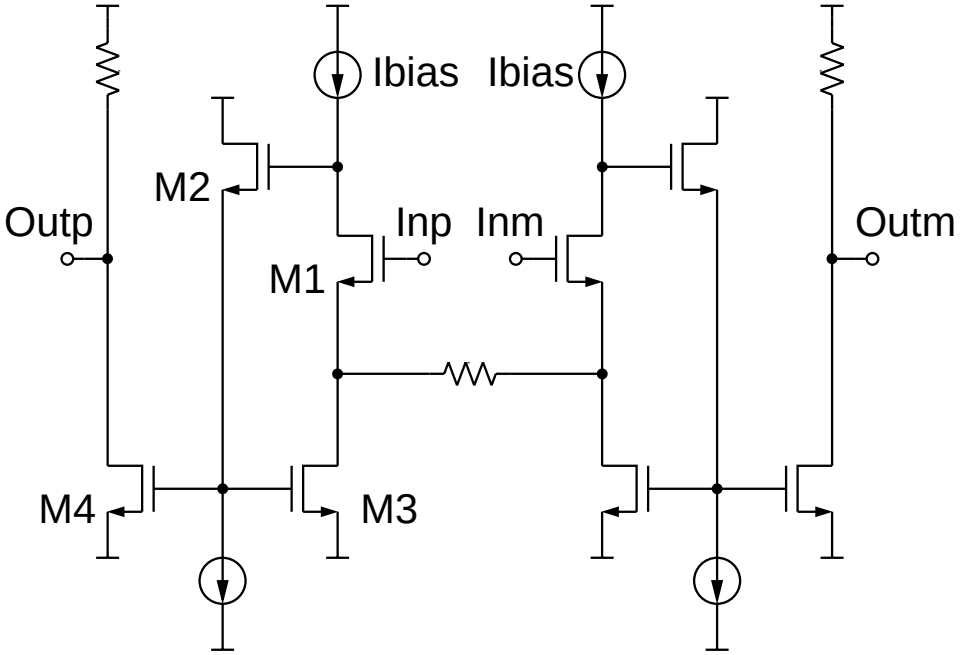
Primary Goal: Make choices to minimize P_D, maximize integration.

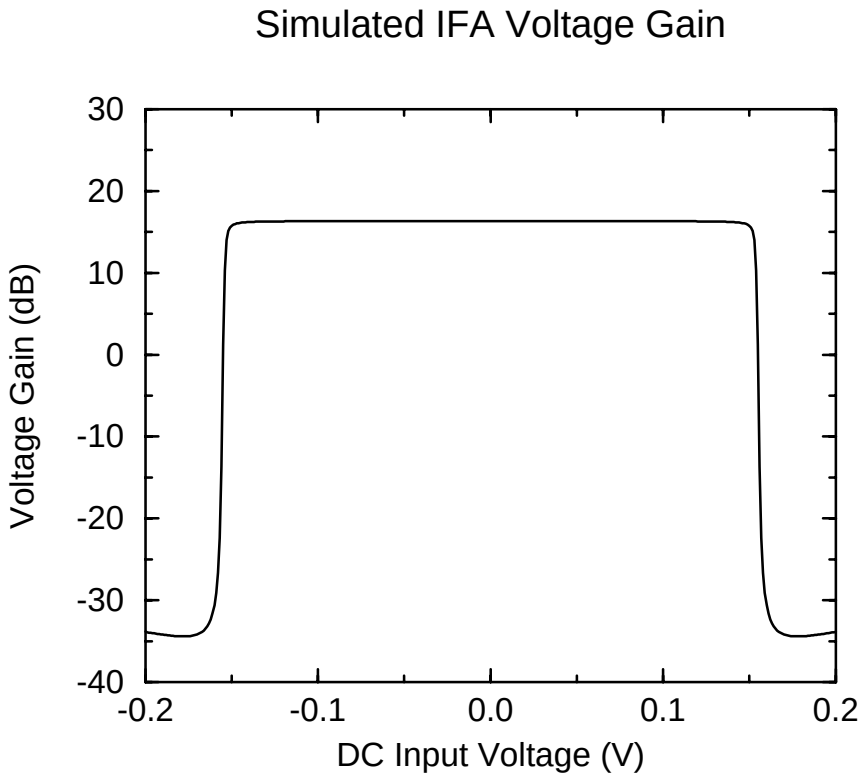
- Low-IF $\Rightarrow$ On-chip active channel filter.
- Image in GPS band $\Rightarrow$ Relaxed I/Q matching.
- Eliminate PLL prescaler $\Rightarrow$ Saves power / noise.
- 1-bit quantization for simplicity.



CIRCUITS: IFA

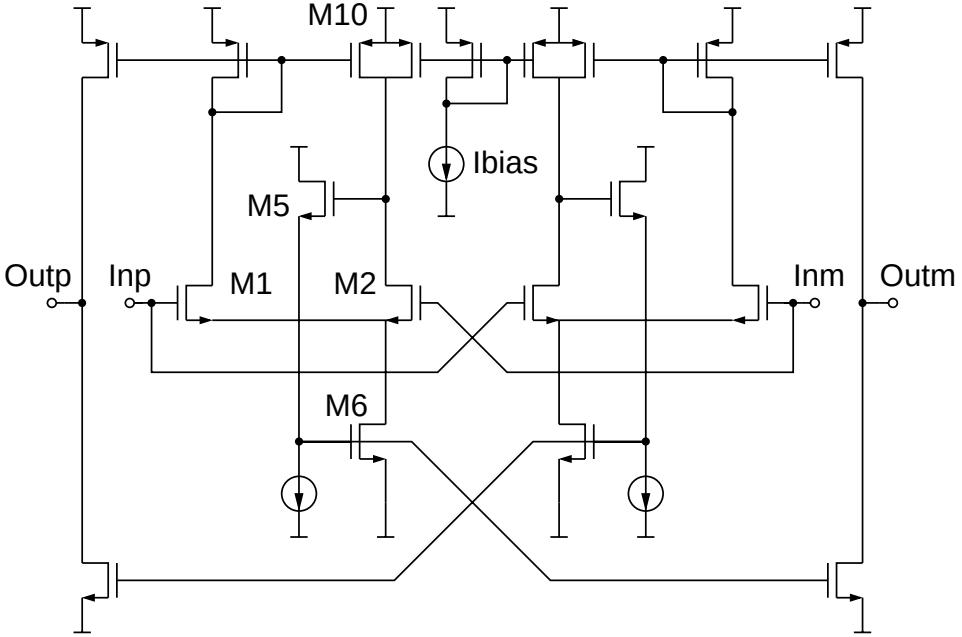
- Low input capacitance, high linearity.
- Load resistors terminate the active filter input.

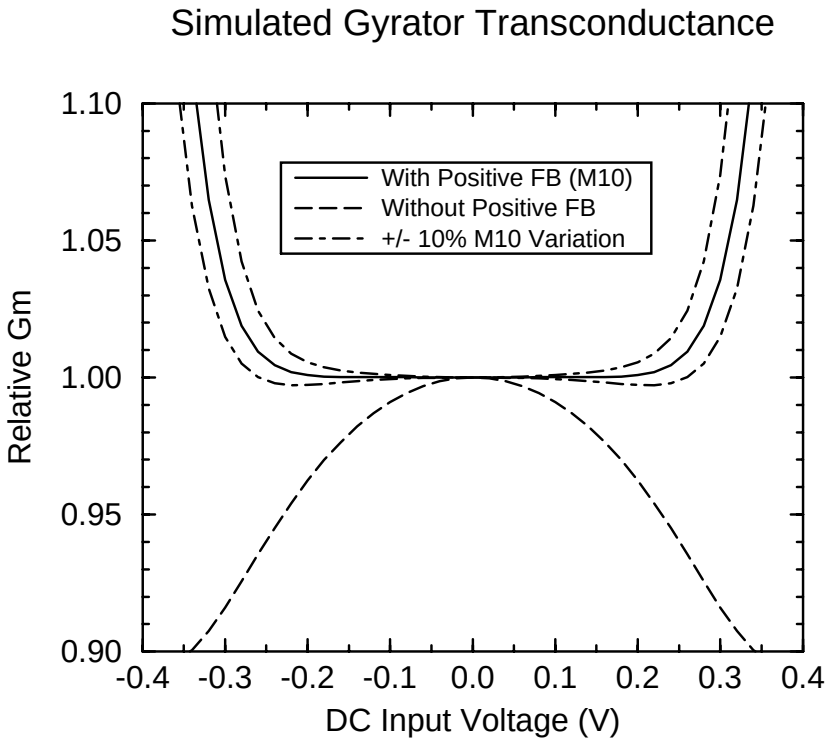




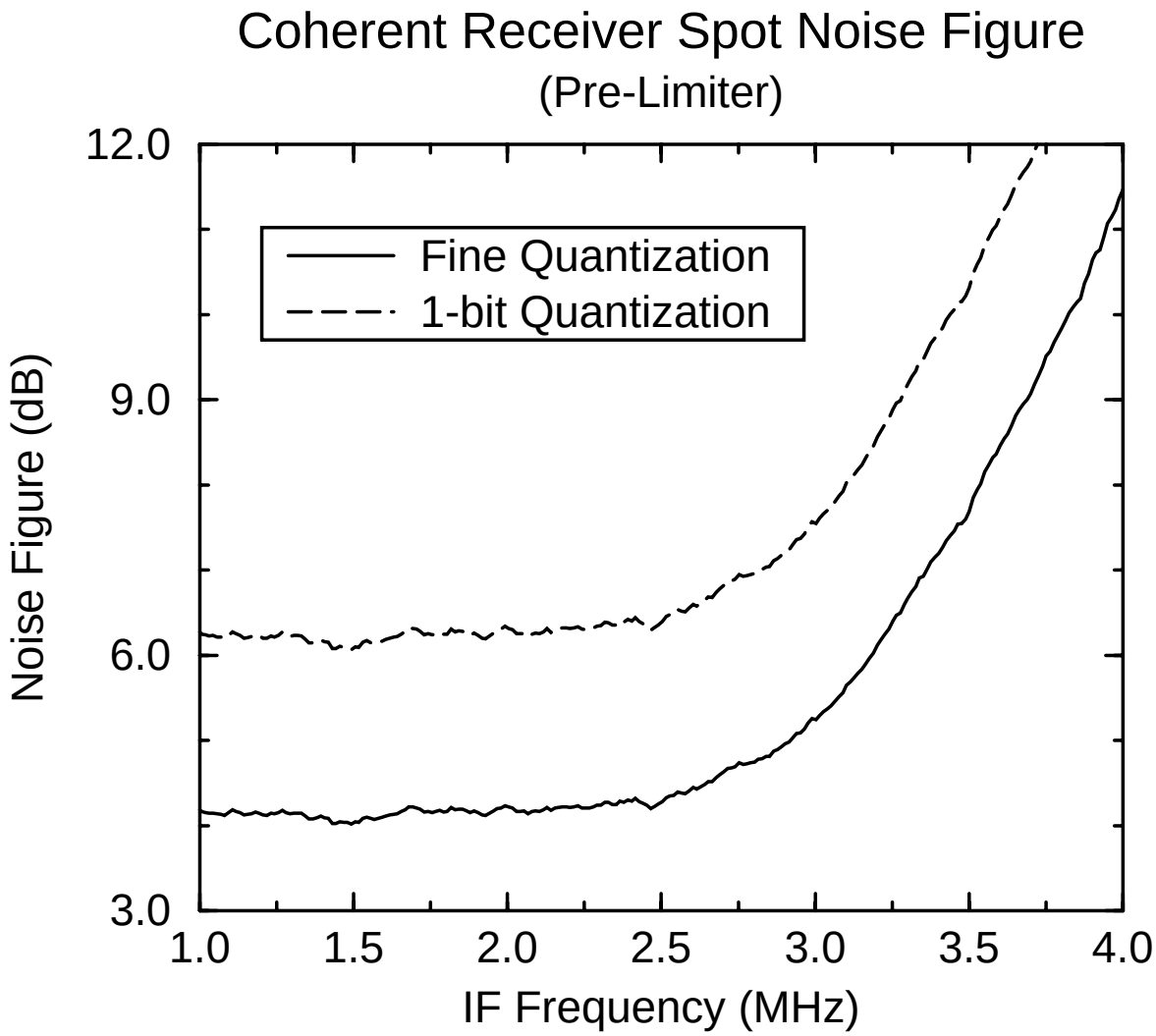
CIRCUITS: GM-C FILTER (TRANSCONDUCTOR)

Use two *square-law* transconductors to build a *linear*, class-AB transconductor. A little positive feedback (M10) compensates for mobility degradation in M1.

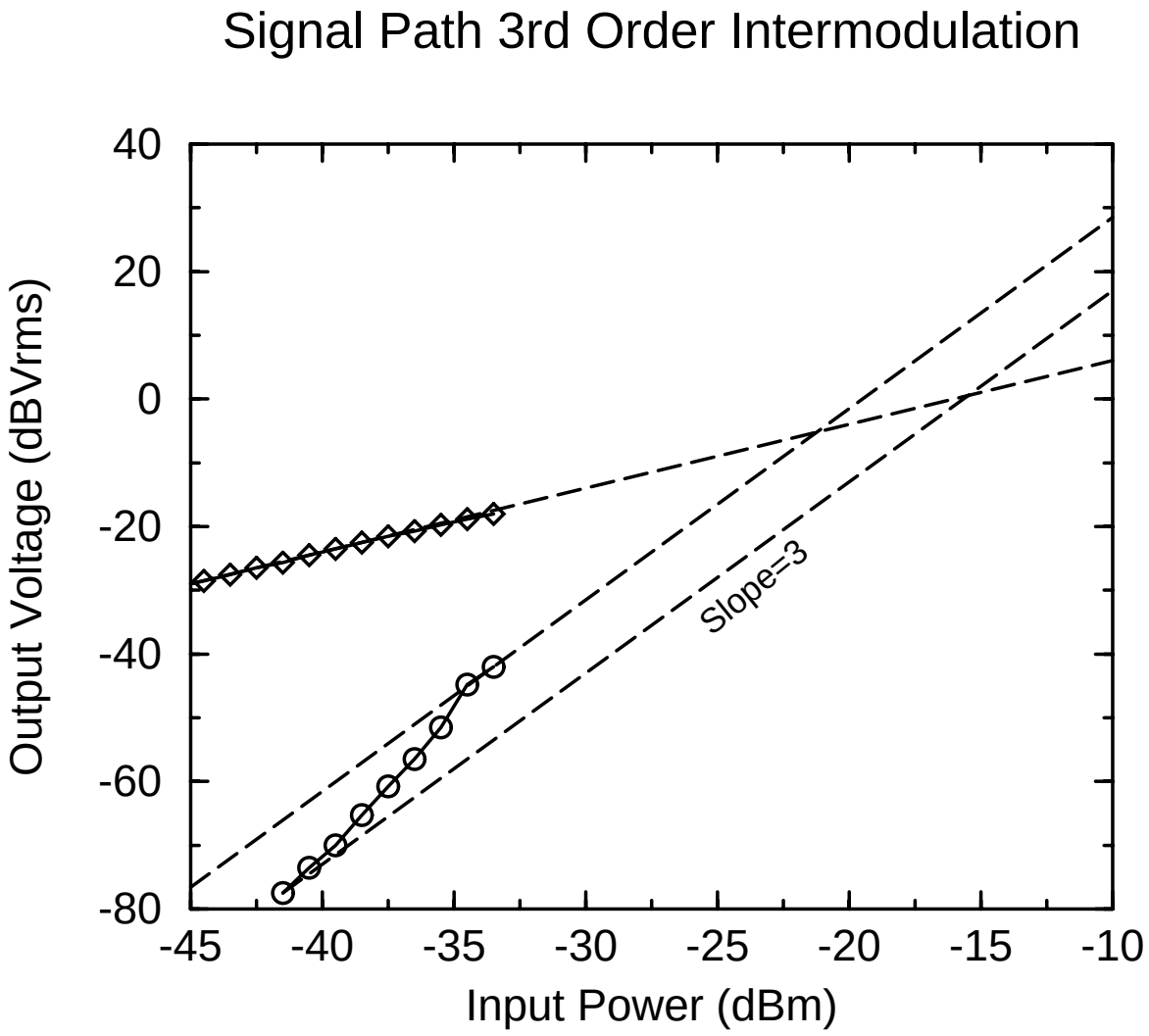




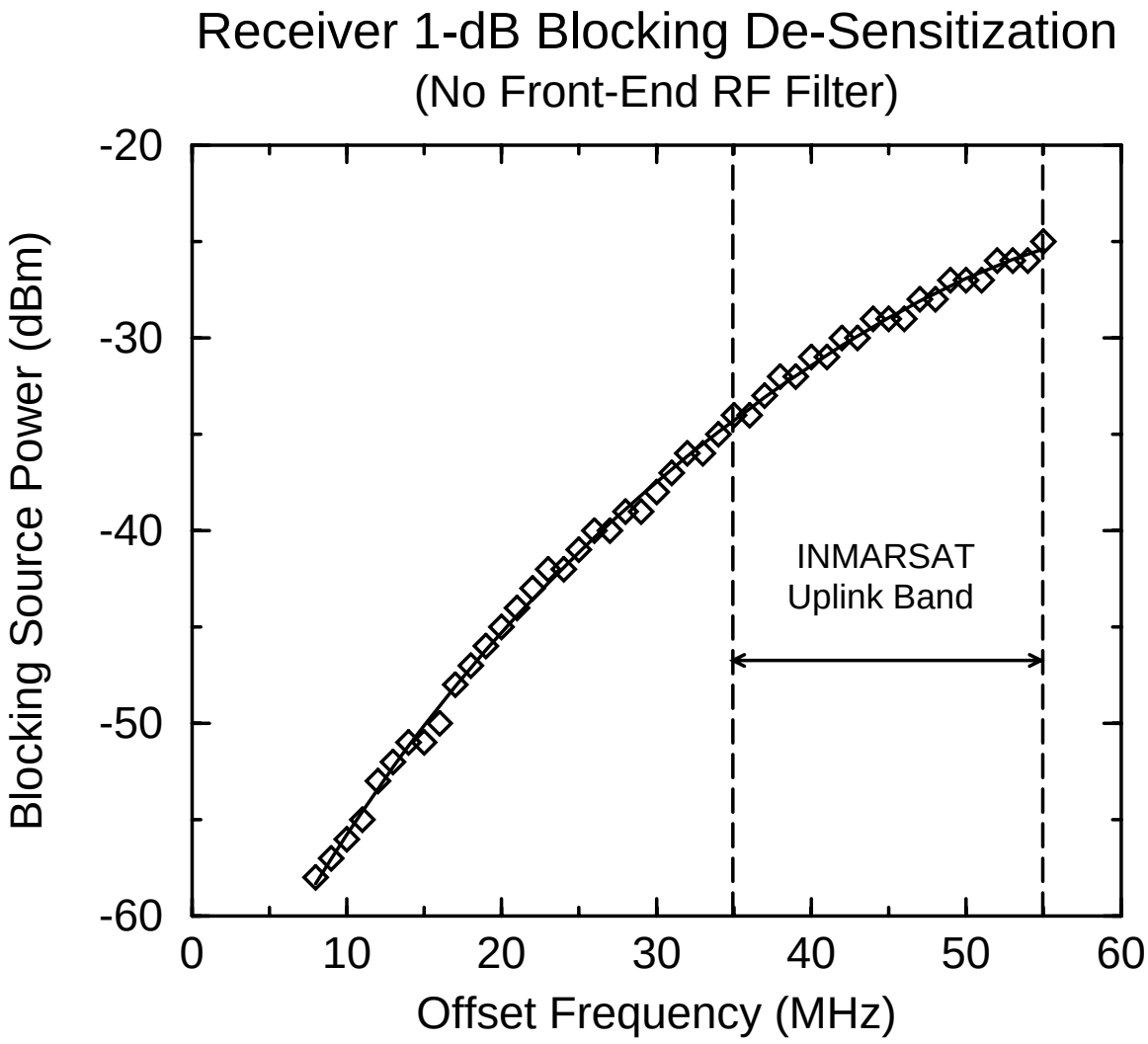
EXPERIMENTAL RESULTS: NOISE FIGURE



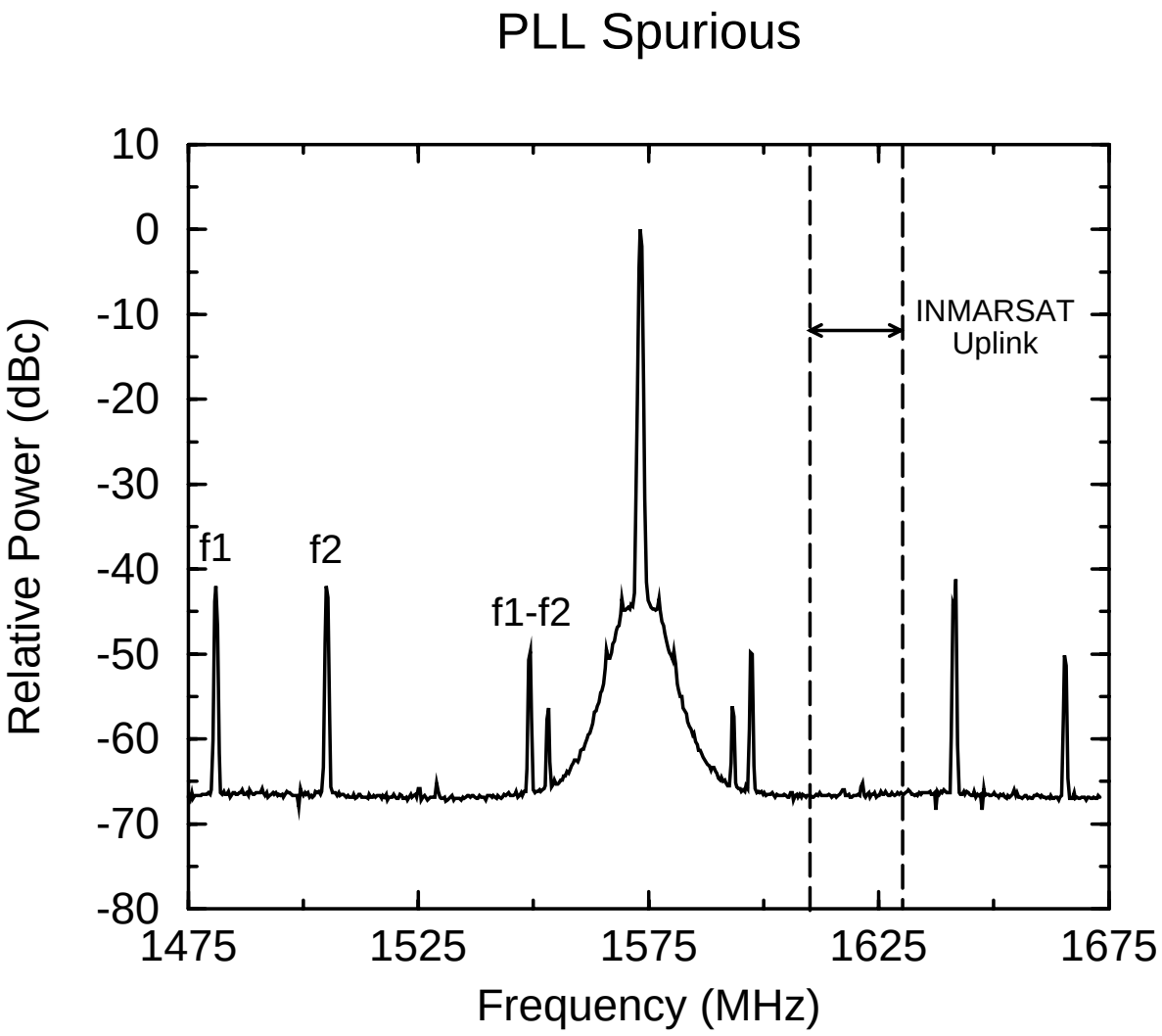
EXPERIMENTAL RESULTS: LINEARITY



EXPERIMENTAL RESULTS: BLOCKING PERFORMANCE



EXPERIMENTAL RESULTS: PLL SPURIOUS



PERFORMANCE SUMMARY

Signal Path Performance		*PLL Performance*	
LNA Noise Figure	2.4dB	Loop Bandwidth	5MHz
LNA S11	$\leq$ -15dB	Spurious Tones	$\leq$ -42dBc
Coherent Receiver NF	4.1dB	VCO Tuning Range	240MHz ($\pm$ 7.6%)
IIP3 (Filter-limited)	-16dBm @ -43dBm P_s	VCO Gain Constant	240MHz/V
Peak SFDR	57dB	LO Leakage @ LNA	$<$ -53dBm
Filter Cutoff Freq.	3.5MHz		
Filter PB Peaking	$\leq$ 1dB	*Power/Technology*	
Filter SB Atten.	$\geq$ 52dB @ 8MHz	Signal Path	79mW
	$\geq$ 68dB @ 10MHz	PLL / VCO	36mW
Pre-Filter G_p	19dB	Supply Voltage	2.5V
Pre-Filter A_v	32dB		
Total G_p	$\approx$ 82dB	Die Area	11.2mm^2
Total A_v	$\approx$ 107dB	Technology	0.5μm CMOS
Non-Coherent Output SNR	15dB		

Closing Thoughts

- CMOS is not ideal, but much more than adequate for many applications.
- Scaling trends will continue to improve CMOS.
- “RF CMOS” is not an oxymoron anymore.

Acknowledgments

- Many slides were prepared, and generously supplied, by the following Stanford Ph.D. candidates:
- Hirad Samavati (fractal capacitors)
- Patrick Yue (spiral inductors)
- Ali Hajimiri (oscillator phase noise)
- Derek Shaeffer and Arvin Shahani (LNA work and GPS receiver)