Low Phase Noise CMOS Ring Oscillator VCOs for Frequency Synthesis

July 27, 1998

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Outline

- Motivation
  - Phase Noise Theory
  - Voltage-controlled Oscillator Design
  - Conclusion and Acknowledgements
What is Phase Noise?

- Undesirable phase fluctuations due to intrinsic device noise
- Output power is not concentrated at the carrier frequency alone
- Phase noise is represented as a ratio of power in 1Hz bandwidth in one sideband to the power of the carrier.
- Specified in dBc/Hz at a frequency offset from the carrier.

\[ L(\Delta f) = \frac{P_{SSB}}{P_C} \]

\[ P_{SSB} \]

\[ P_C \]

\[ f_0 \]

\[ f_0 + \Delta f \]

\[ \frac{1}{f^2} \]

\[ \frac{1}{f^3} \]

Noise Floor
Frequency synthesizers are implemented using phase-locked loops (PLLs).

Major sources of power dissipation are the VCO and the frequency divider.

Frequency reference is usually a crystal oscillator with very low phase noise.

A PLL tracks phase noise of the reference within its loop bandwidth, relaxing the close-in phase noise requirements of the VCO.

Typical CMOS PLL frequency synthesizer

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A frequency-locked loop (FLL) synthesizer may not require a frequency divider.

A FLL tracks frequency, not phase making close-in phase noise of VCO more critical.

Biotelemetry application: 174-216MHz

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Oscillators are Time-Variant Systems

- Current impulse injected at the peak changes the amplitude and has no effect on the phase.

- Current impulse injected at zero-crossing changes the phase and has minimal effect on the amplitude.

**Phase Impulse Response**

\[ h_{\phi}(t, \tau) = \frac{\Gamma(\omega_0 \tau)}{q_{\text{max}}} u(t - \tau) \]

- Impulse Sensitivity Function \( \Gamma(x) \) is periodic.
- \( q_{\text{max}} \) is the maximum charge displacement in the tank.
Impulse Sensitivity Function for Ring Oscillators

\[ \phi(t) = \frac{1}{q_{max}} \left[ \frac{c_0}{2} \int_{-\infty}^{t} i(\tau) \, d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i_n(\tau) \cos(n\omega \tau) \, d\tau \right] \]

- \( \Gamma(\chi) \) is calculated from the output waveform.
- \( \Gamma(\chi) \) is expressed as a Fourier series and used to determine the phase noise resulting from noise sources.
- High sensitivity to noise at the transitions of the output
- Phase noise close to the carrier results from the folding of device noise centered at integer multiples of the carrier frequency.
- Upconversion of device $1/f$ noise occurs through $\Gamma_{dc}$, the DC value of the ISF.
- $\Gamma_{dc}$ is governed by the symmetry properties of the waveform.
Hajimiri Phase Noise Model

- Phase Noise in $1/f^3$ region is due to device $1/f$ noise.
- It is commonly assumed that the $1/f^3$ corner of phase noise is the same as the $1/f$ corner of the device noise spectrum. This is NOT the case.

$$L(\Delta \omega) = 10 \cdot \log \left\{ \frac{\Gamma_{rms}^2 \cdot \frac{i_n^2}{q_{max} \cdot 2 \cdot \Delta \omega^2}}{\Gamma_{dc}^2} \right\}$$

Calculation of $\Gamma_{rms}$ and $\Gamma_{dc}$ for Ring Oscillators$^{4,5}$

\[
\Gamma_{dc} = \frac{1}{2\pi} \int_0^{2\pi} \Gamma(x) dx
\]

\[
\Gamma_{rms} = \frac{1}{2\pi} \int_0^{2\pi} \Gamma^2(x) dx
\]

\[
\frac{\Gamma^2_{dc}}{\Gamma^2_{rms}} = \frac{3}{2N} \cdot \frac{(1 - \beta)^2}{(1 - \beta + \beta^2)}
\]

\[
\beta = \frac{S_{rise}}{S_{fall}}
\]

- $S$ is the maximum slope of the normalized output waveform
- $N$ is the number of stages


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Voltage-controlled Oscillator Design

- Use buffers with replica-feedback biasing.
- NMOS differential pairs with linear PMOS loads.
- $V_{ctl}$ changes the bias $I_{dd}$ of the buffers.
- Replica bias ensures loads are mostly in their linear region by forcing the maximum single-ended swing $V_s = V_{dd} - V_{ctl}$
- Frequency is controlled by changing the bias of the buffers and hence the delay through each cell.
- Power dissipation is determined by frequency and phase noise required.
Power Dissipation of Differential Ring Oscillator

\[ P = 2N^2 C_L V_{dd} V_s f \]

- \( N \) is the number of stages
- \( C_L \) is the total load capacitance at each buffer
- \( V_s \) is the maximum single-ended swing
- \( V_{dd} \) is 3.3V
Phase Noise of Differential Ring Oscillator

\[ L\{\Delta f\} \geq \frac{18kTV_{dd}}{\pi^2 P} \cdot \left(\frac{2.5}{E \cdot L_{\text{eff}}} + 1\right) \cdot \left(\frac{f_o}{\Delta f}\right)^2 \cdot N \]

Lower bound on phase noise in the \(1/f^2\) region

- Minimum length short-channel differential pair devices
- \(L_{\text{eff}} = 0.5\mu\text{m}\)
- \(E_c = 5.6 \times 10^6\text{V/m}\)
Phase Noise vs. Power Dissipation

Selected $W_n=6\mu m$ for 200MHz at 2.1dBm (1.6mW), -90dBc/Hz @ 100KHz
Differential Buffer Topology

Clamped load
- Excellent supply rejection\textsuperscript{6}.
- The cross-coupled loads make delay insensitive to common-mode noise.

Symmetric load
- Good supply noise rejection.
- Used extensively in PLL and clock generators\textsuperscript{7}.

Cross-coupled load
- Sweep width of cross-coupling devices with fixed total width ($W_1 + W_2 = W_3 = 6\, \mu m$) of the loads.
- Maximum symmetry for $W_1 = W_2 = 0.5W_3$


Comparison of Phase Noise

- Assumed $f_{1/f} = 3$MHz
- $1/f^2$ regions are within 2.6dB as expected for similarly sized noise sources.
- $1/f^3$ corner for cross-coupled load buffer is 20 times lower than that of the clamped load.
- Good agreement with measurements previously reported for clamped load

<table>
<thead>
<tr>
<th>Oscillator</th>
<th>$1/f^3$ corner</th>
<th>$L{100\text{KHz}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) Clamped Load</td>
<td>137KHz</td>
<td>-75dBc/Hz</td>
</tr>
<tr>
<td>(b) Symmetric Load</td>
<td>36KHz</td>
<td>-77dBc/Hz</td>
</tr>
<tr>
<td>(c) Cross-coupled Load</td>
<td>6.5KHz</td>
<td>-80dBc/Hz</td>
</tr>
</tbody>
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Conclusions and Acknowledgements

- A design technique based on the Hajimiri model was presented for the design of low phase noise VCOs.

- We compared the phase noise performance of three differential buffer stages.

- We proposed a cross-coupled load buffer that achieves lower phase noise in the $1/f^3$ region by exploiting single-ended symmetry in the oscillator’s waveform.

- This work was partially supported by NASA-Ames Research Center through a Training Grant No. NGT 2-52211.

- We wish to thank Ali Hajimiri, and Miguel Gabino-Perez for their assistance.