

# **Outline**

- Introduction**

- Interconnect Scaling in conventional CMOS

- Distributed Amplifier Design**

- Transmission Line Parameter Optimization

- Experimental Results

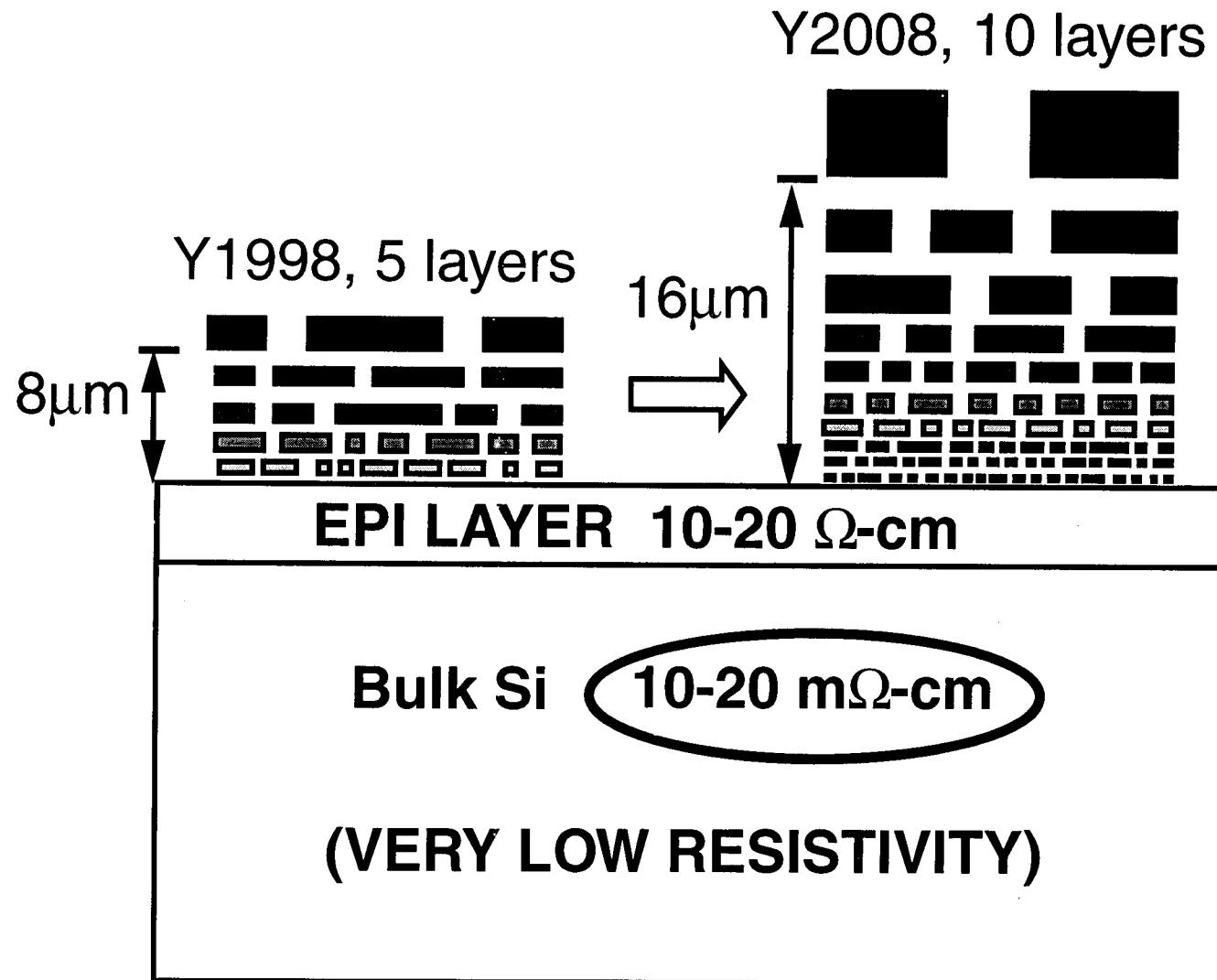
- Distributed Oscillator Design**

- One-stage Ring Oscillator

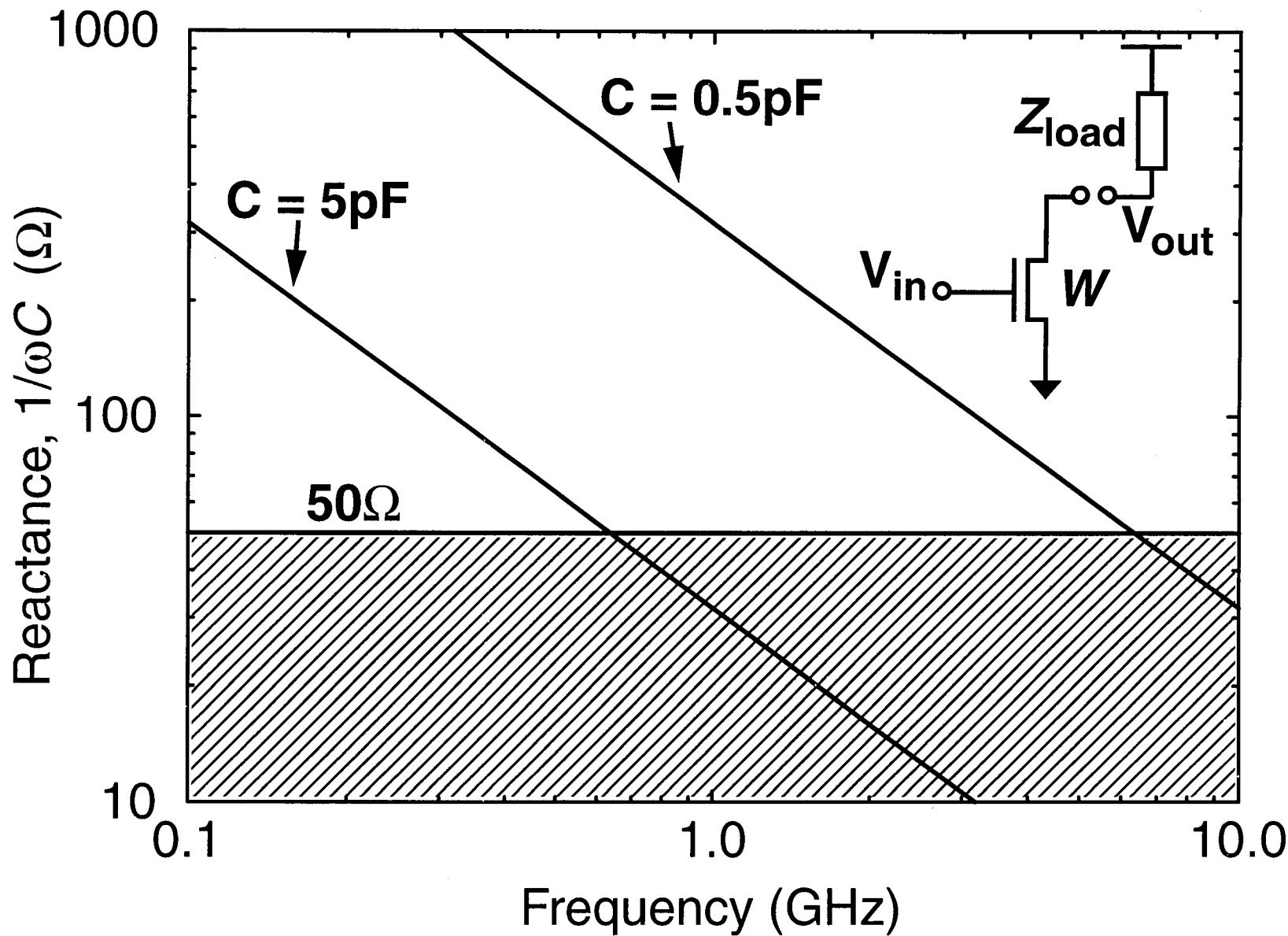
- Experimental Results and Comparisons

- Conclusions**

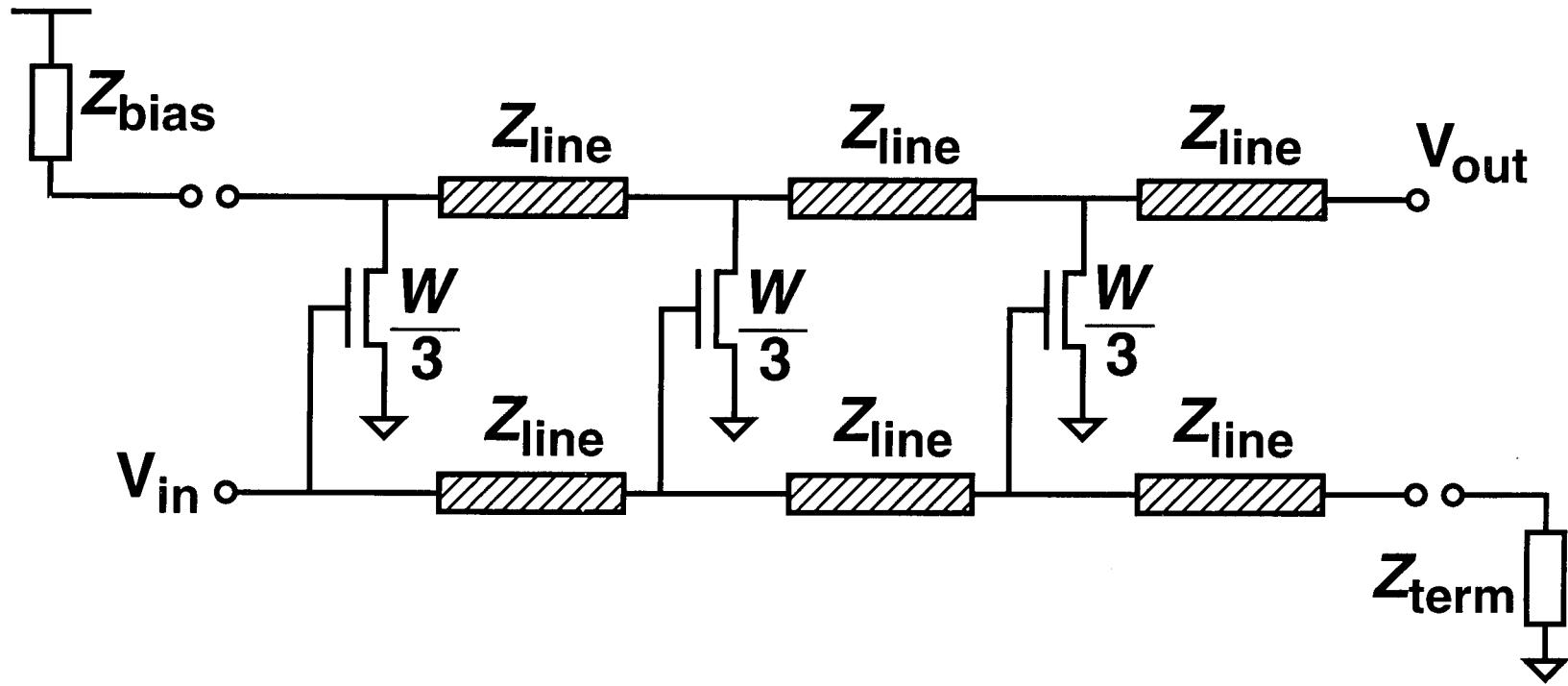
# Microwave Engineer's View of CMOS



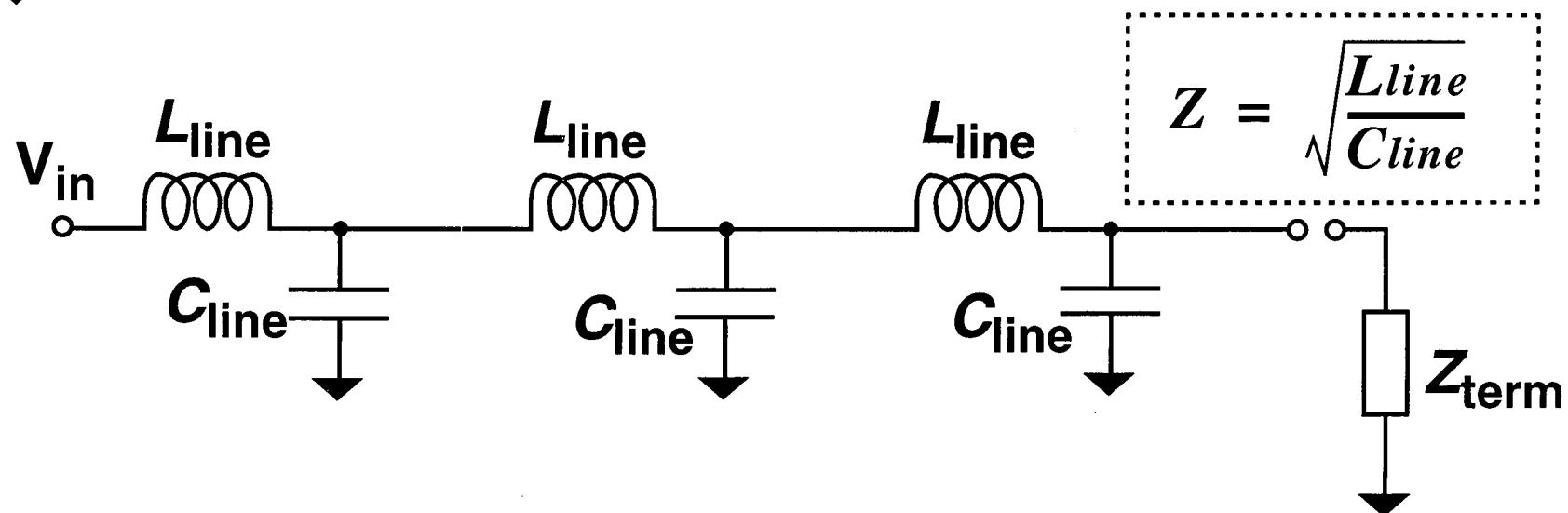
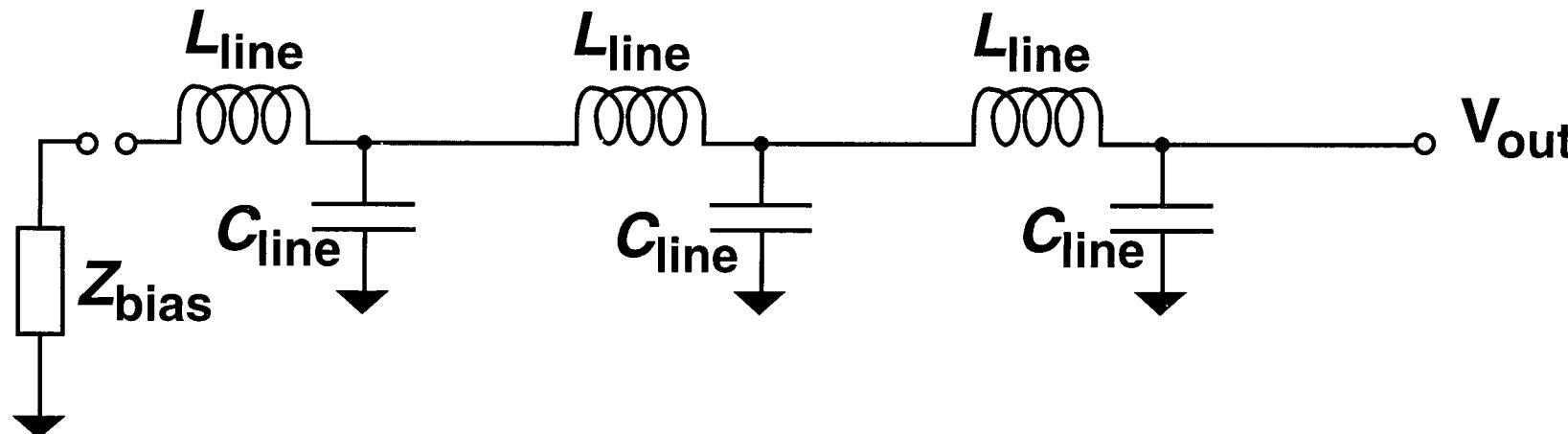
# Lumped Amplifier Capacitance



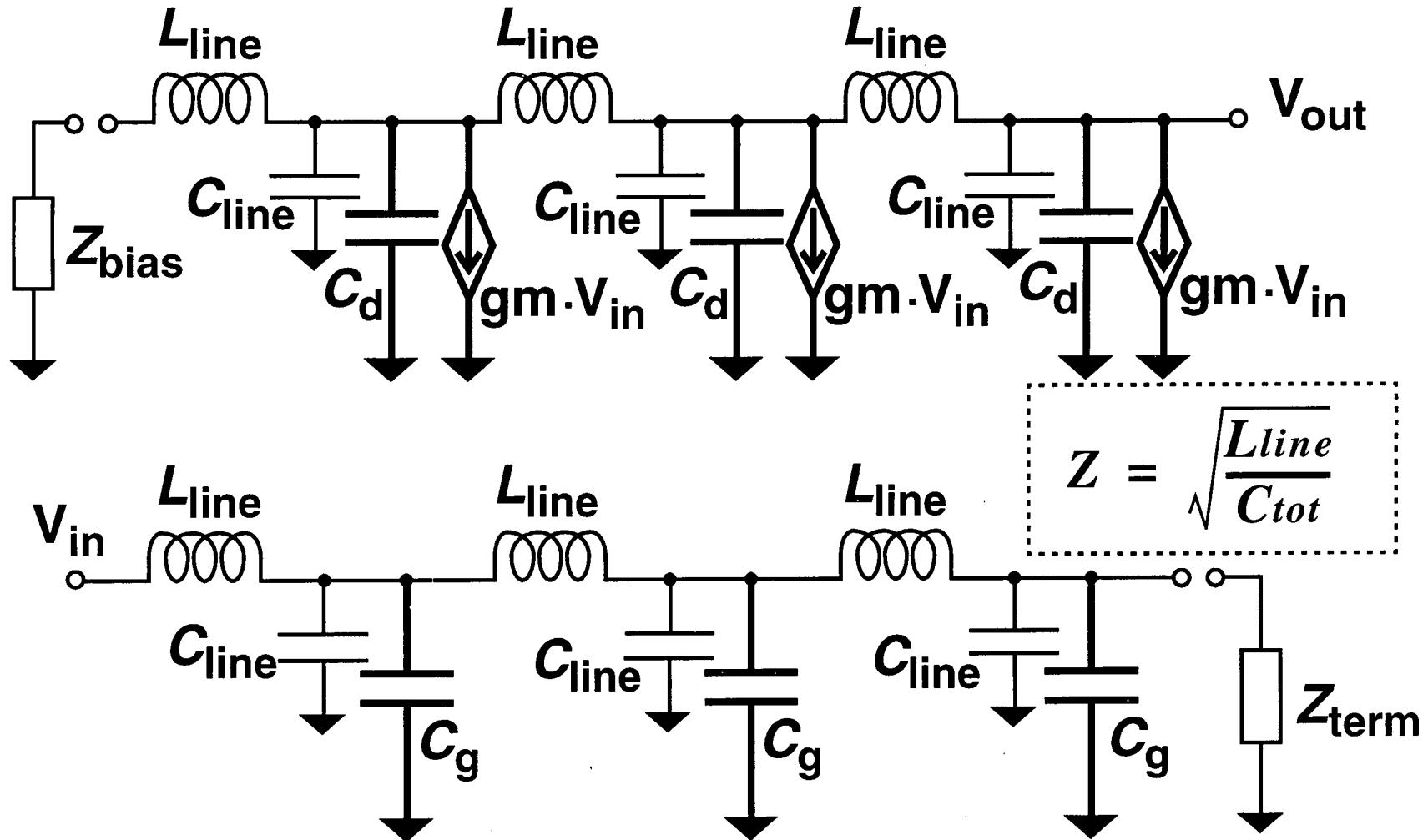
# Traveling-Wave: Gain-Bandwidth-Delay



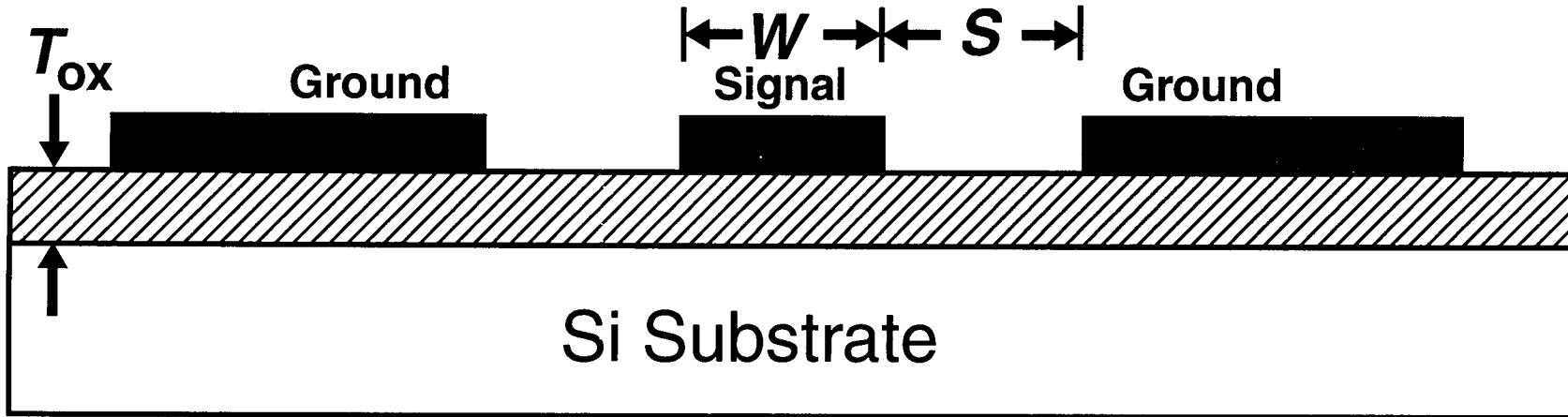
# Transmission Line Model



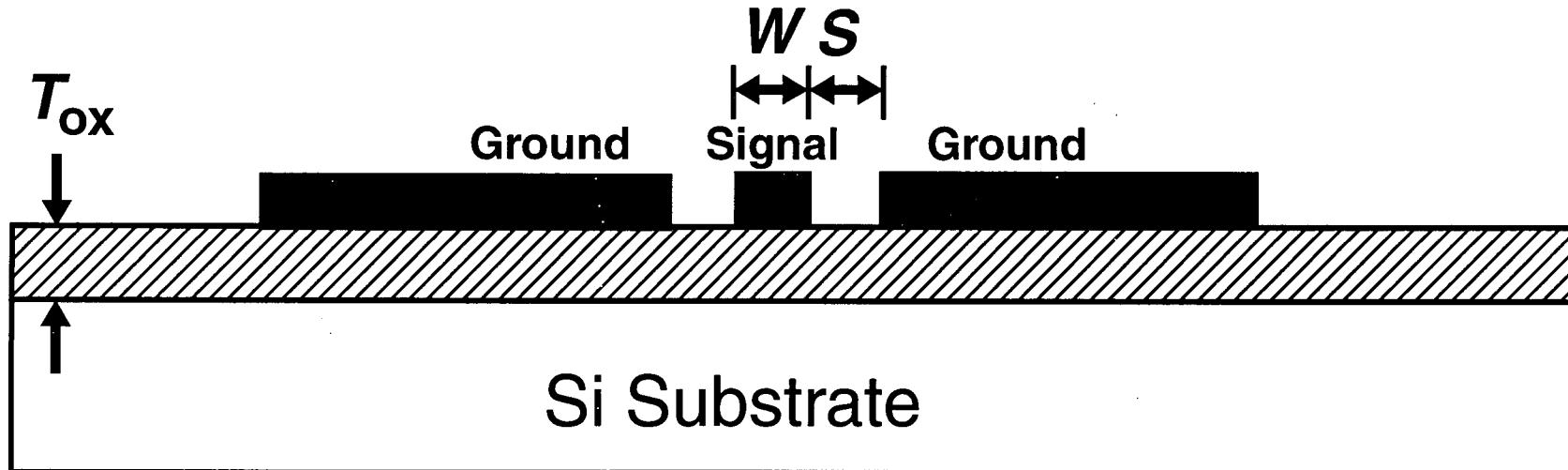
# Distributed Amplifier Model



# Coplanar Lines in Top Level Metal

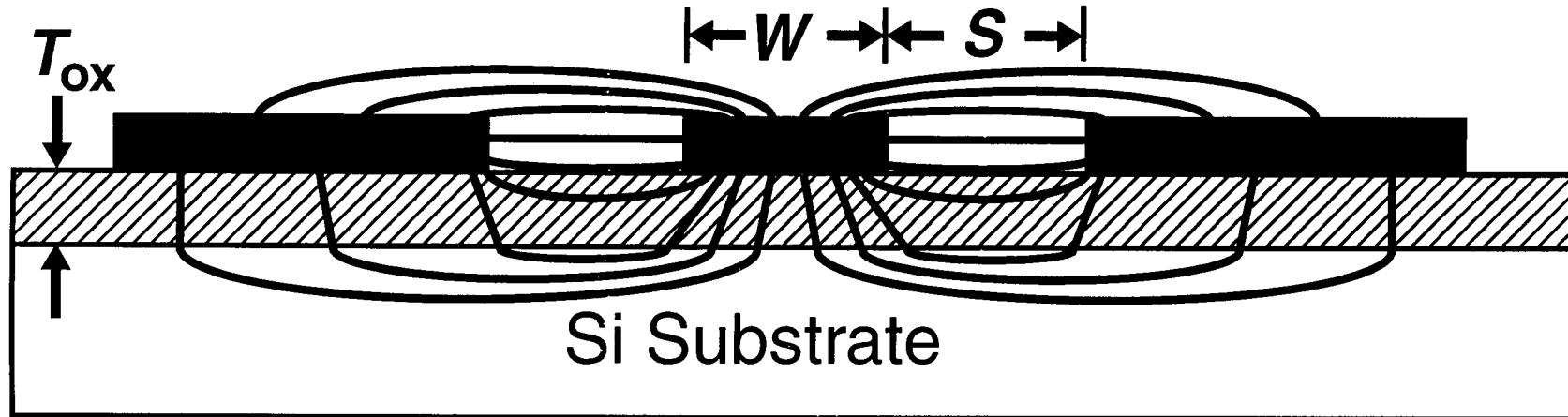


Large Width, Space  $\rightarrow$  small resistive line losses

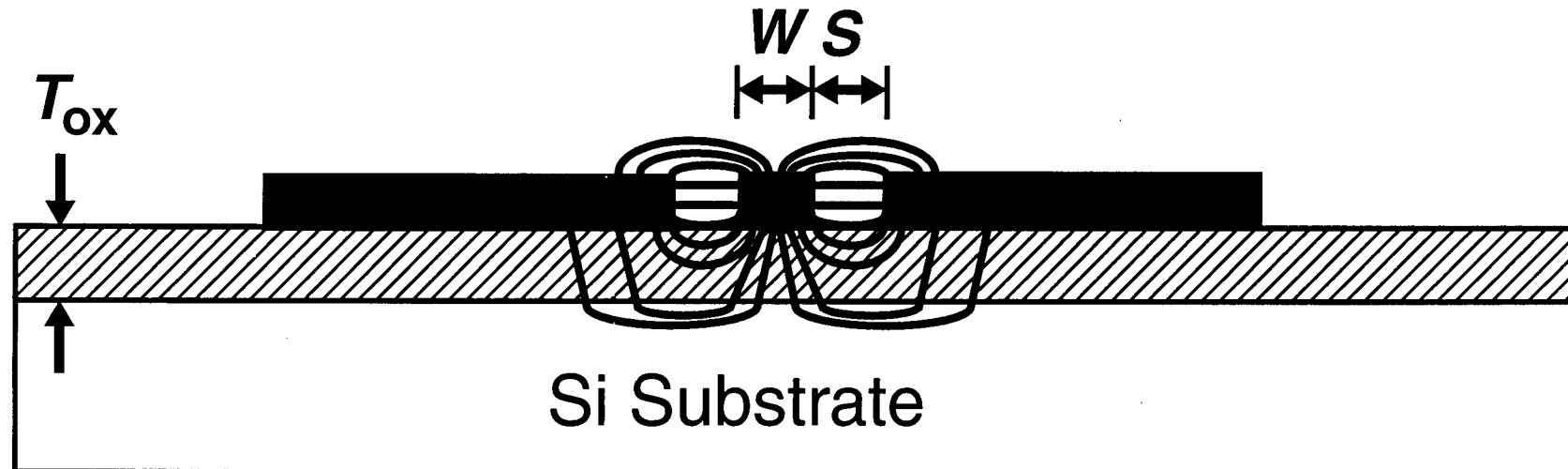


Width, Space  $\rightarrow$  large resistive line losses

# Reduce Coupling Through Si Substrate

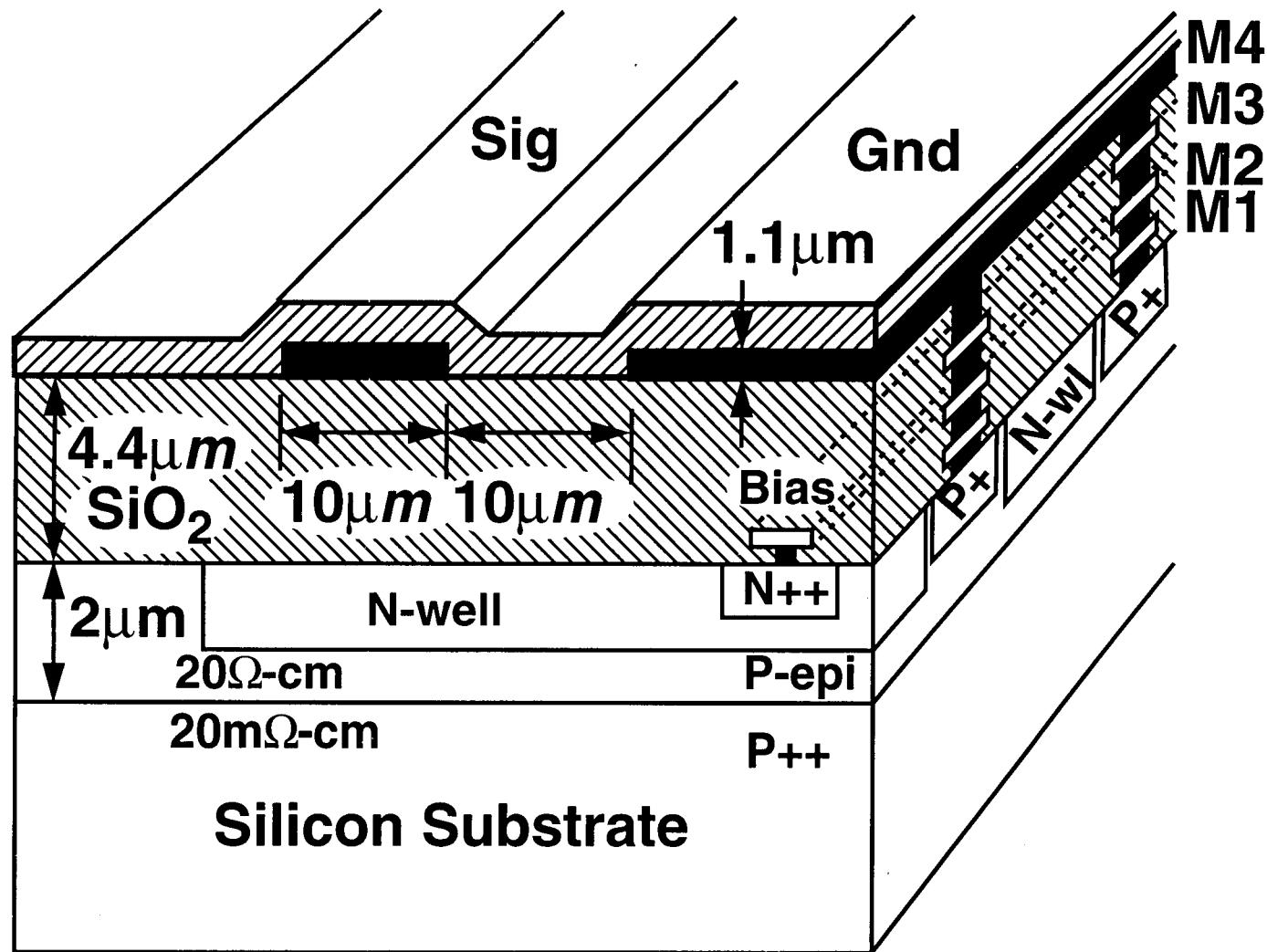


Large Width, Space  $\rightarrow$  large coupling through substrate

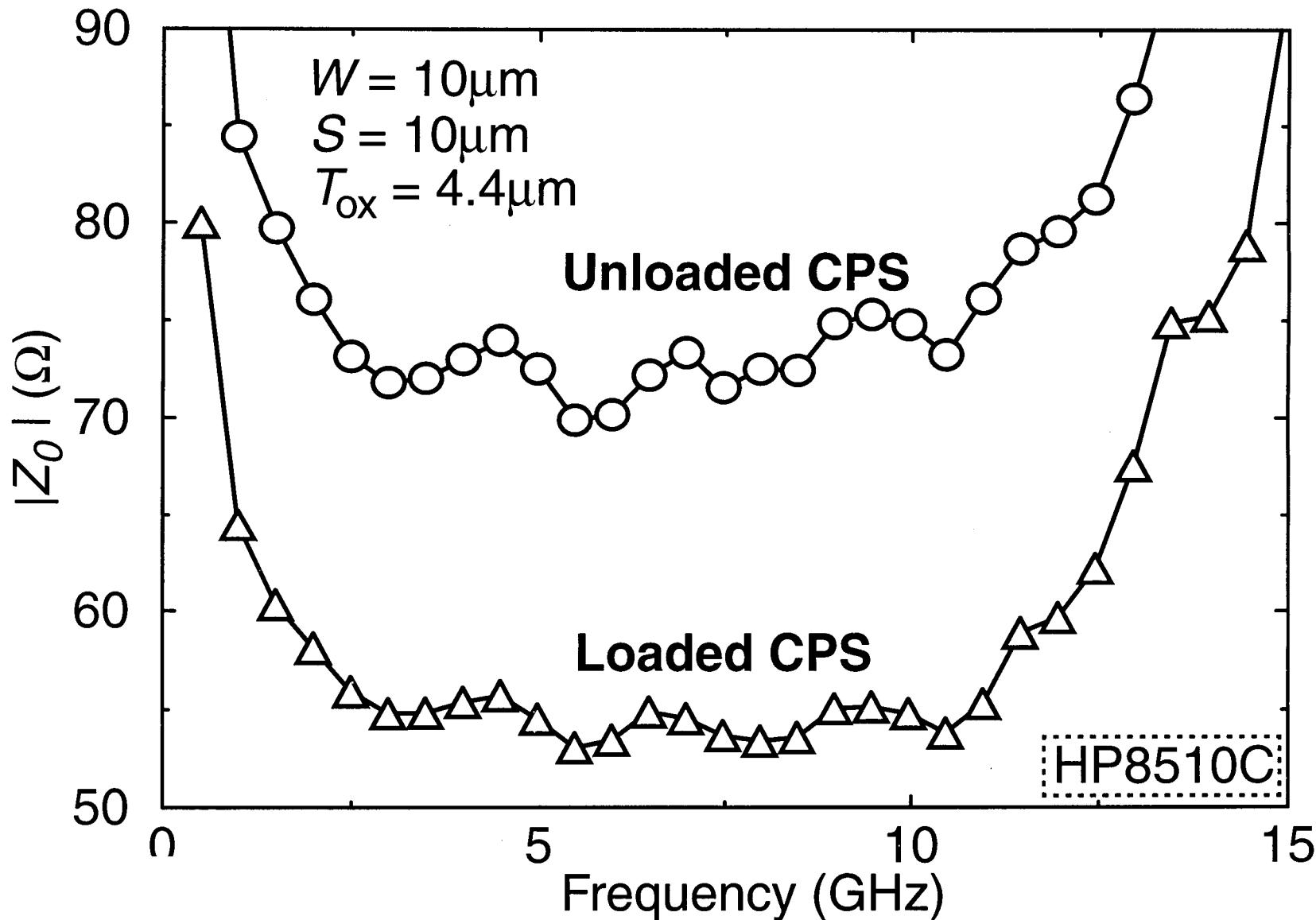


Width, Space  $\rightarrow$  small coupling through substrate

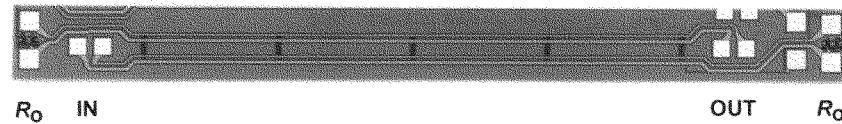
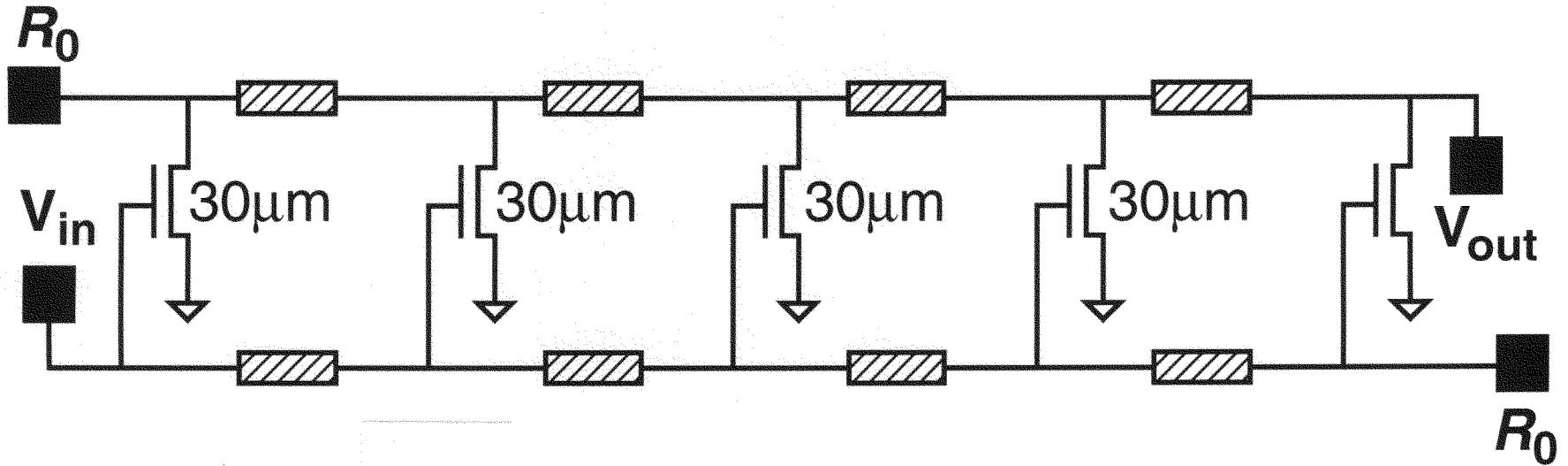
# Coplanar Stripline in HP's Process



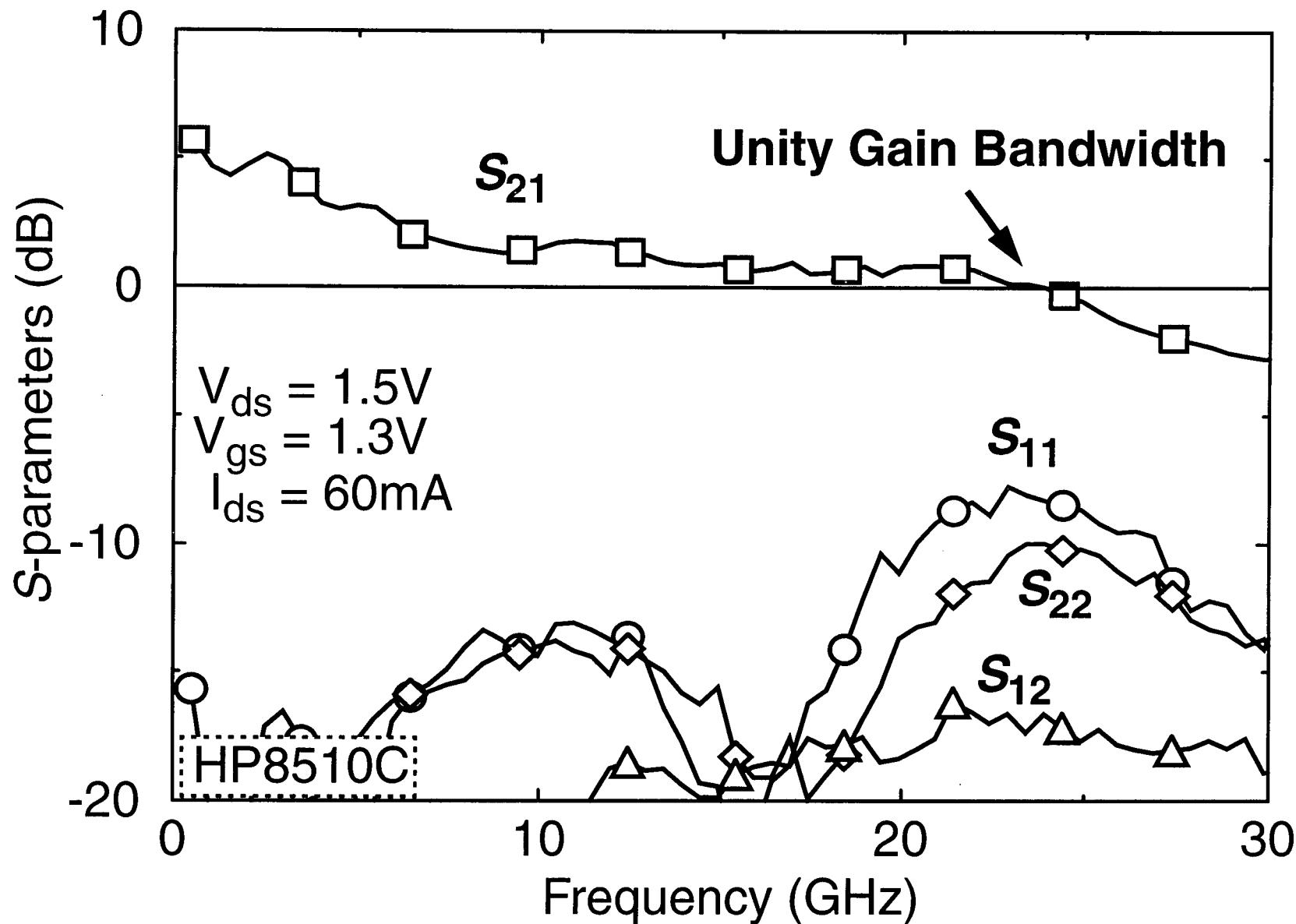
# Measured Characteristic Impedance



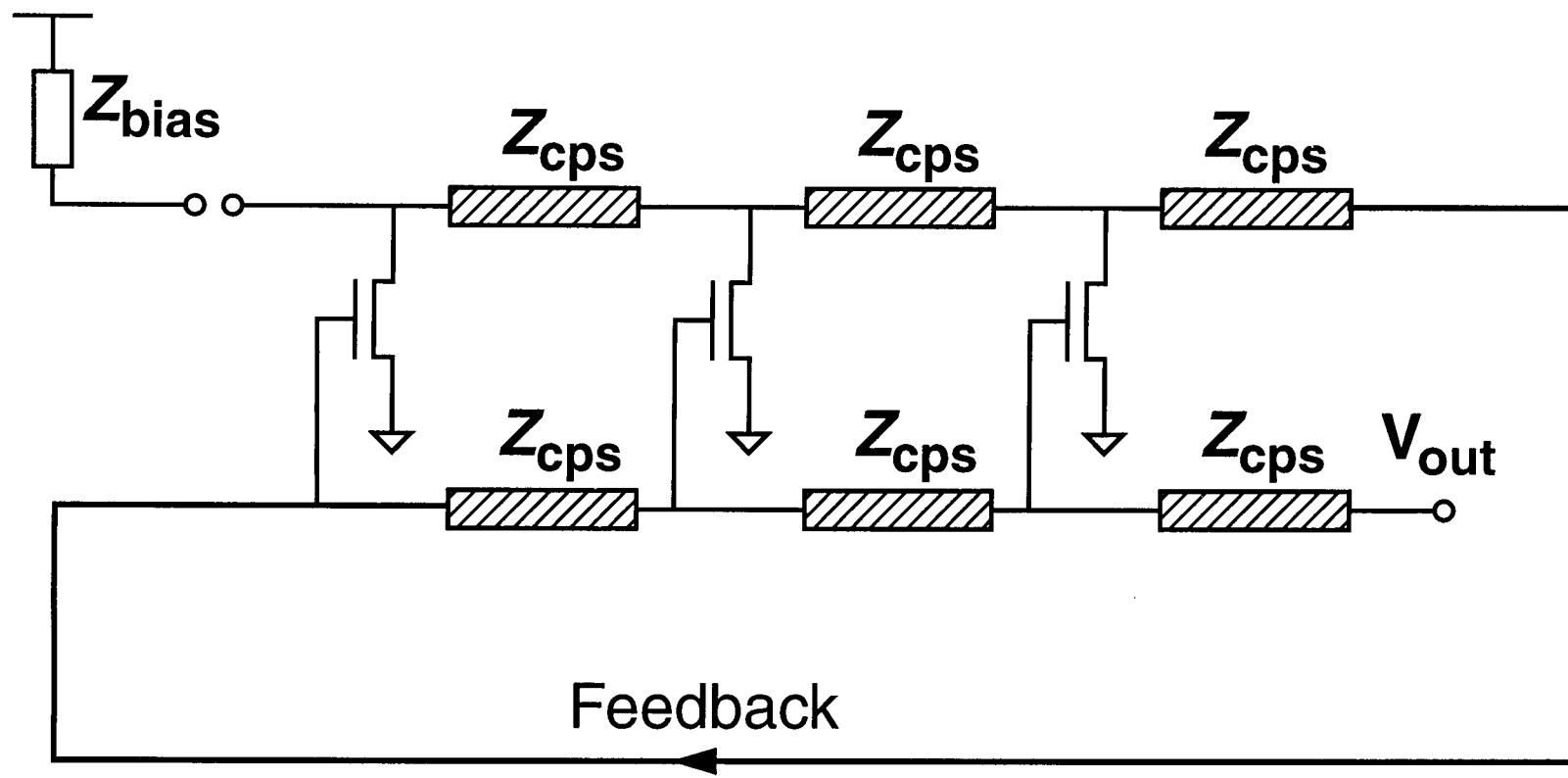
# Die Photo of Distributed Amplifier



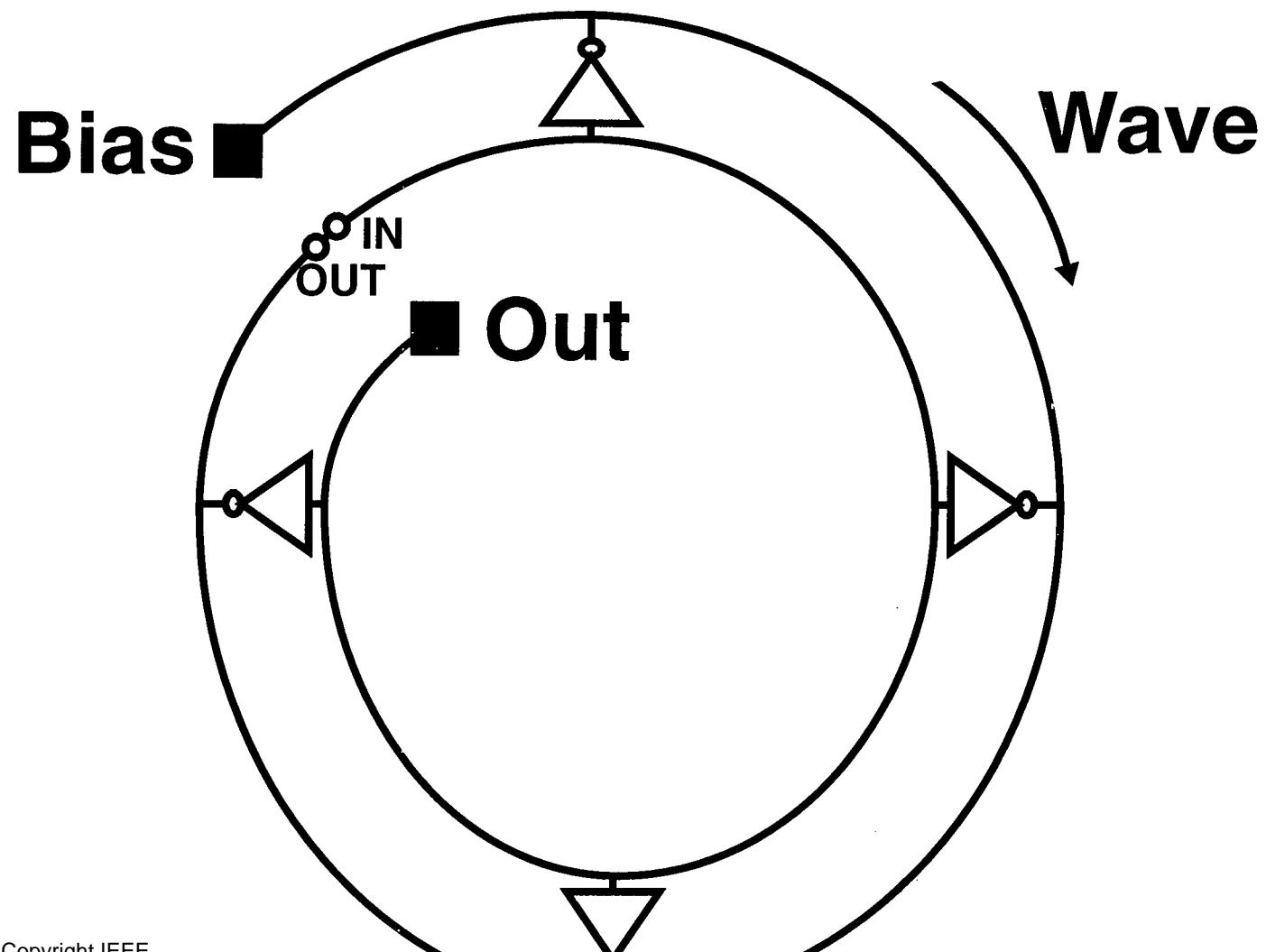
# Distributed Amplifier S-parameters



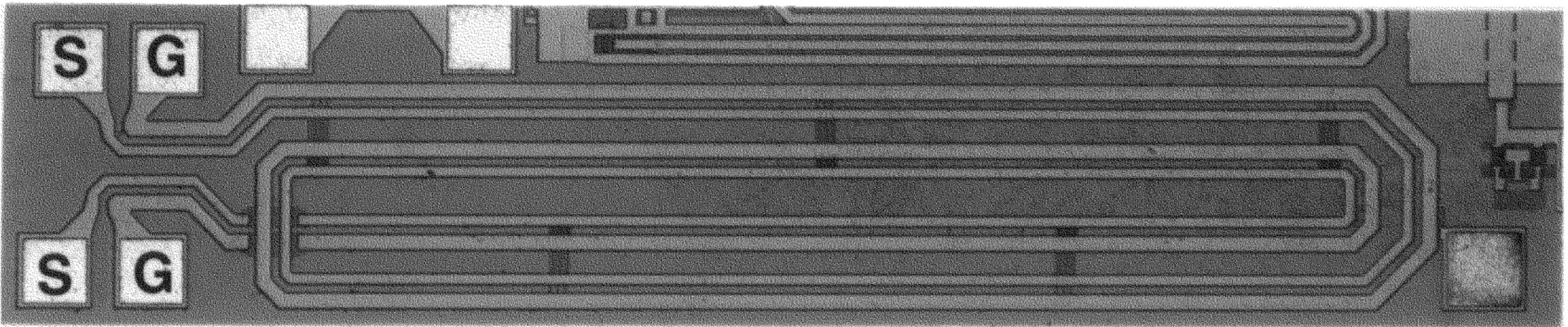
# Distributed Oscillator Schematic



# Ideal Ring Oscillator Layout



$V_{bias}$

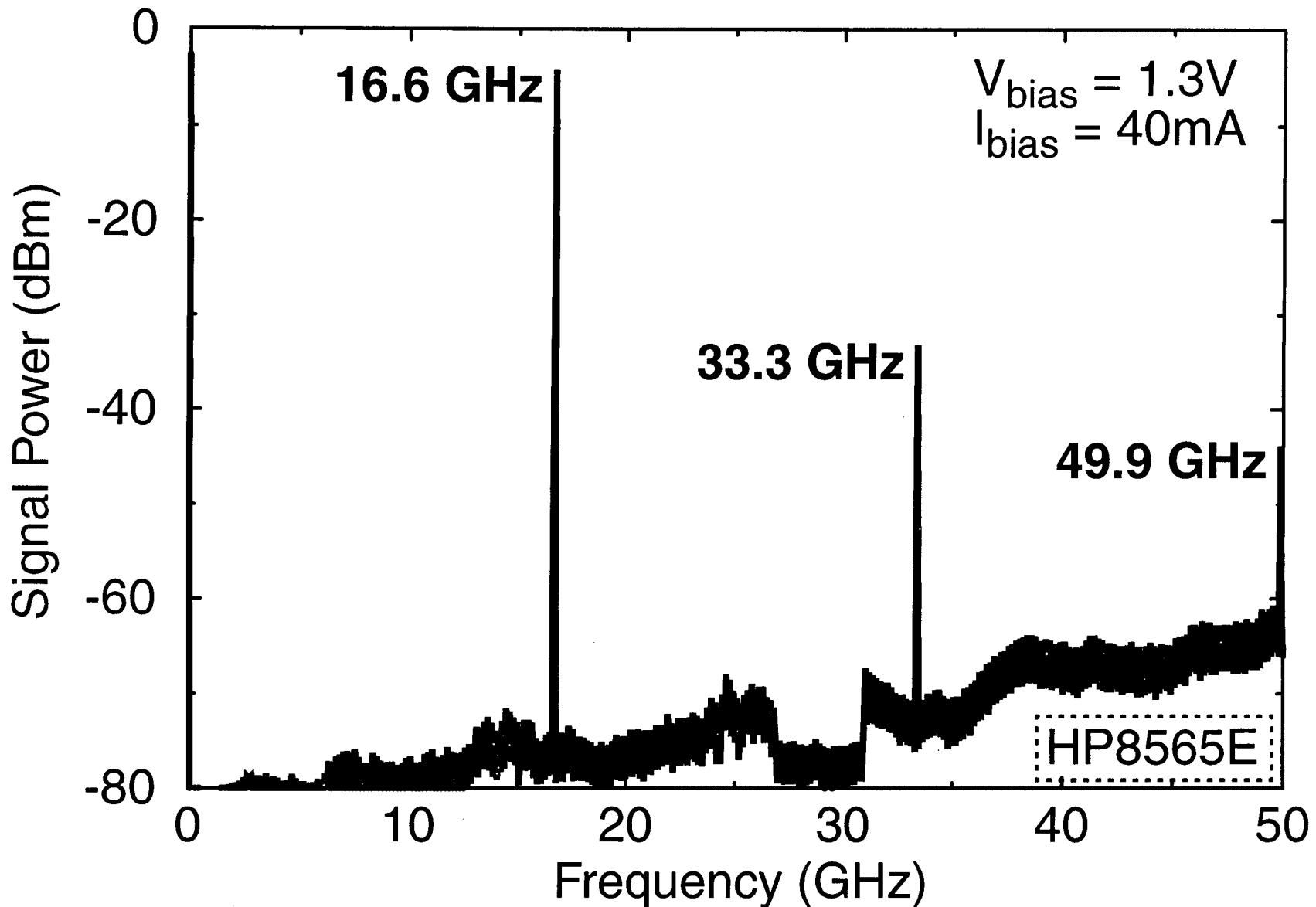


$V_{out\ osc}$

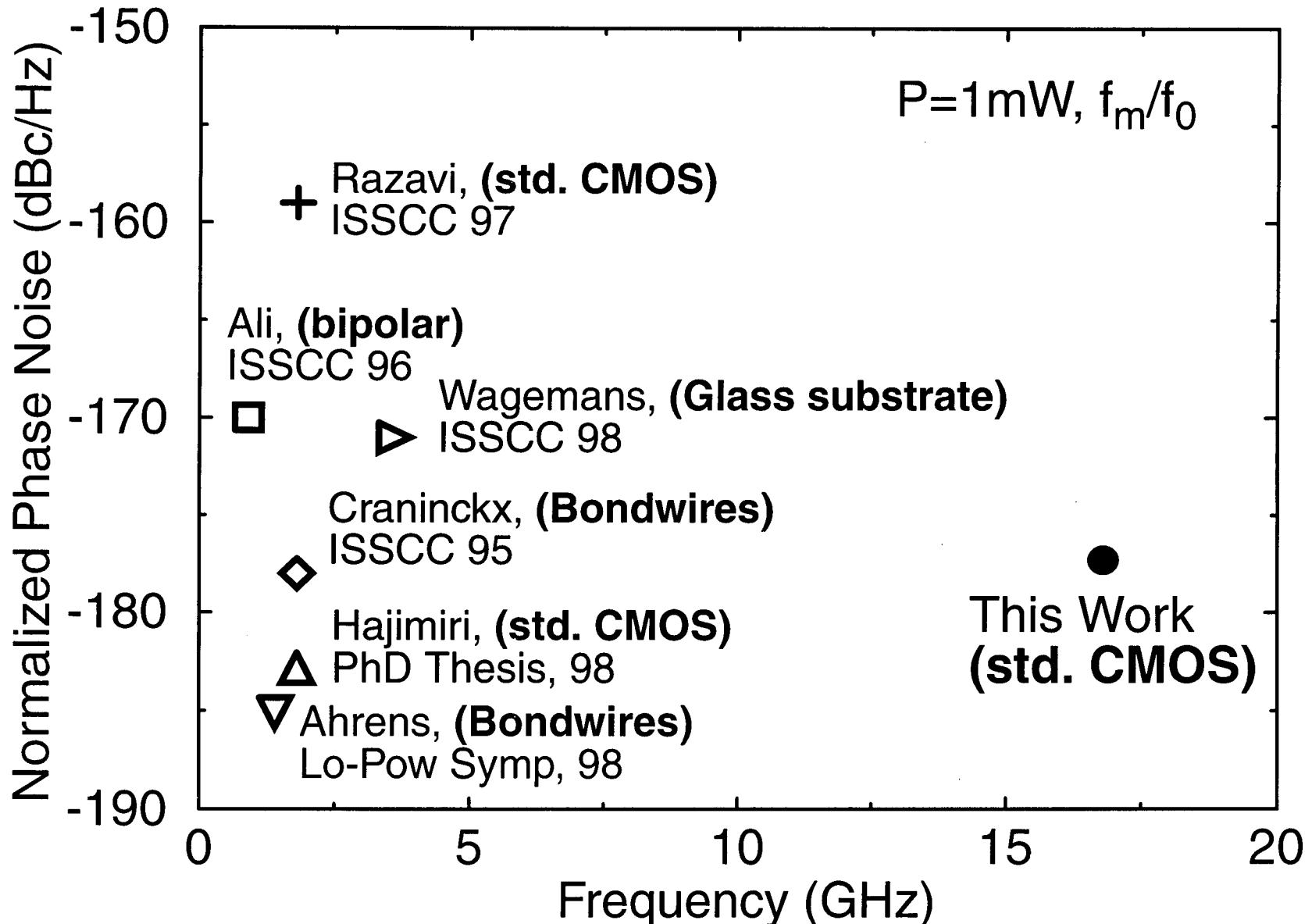
100 $\mu$ m

$V_{n\text{-}well}$

# Oscillator Power Spectrum



# Oscillator Phase Noise Comparison



# Conclusions

- Low-loss transmission lines in conventional CMOS  
70- $\Omega$  CPS with 0.7dB/mm at 17 GHz
- Monolithic 50- $\Omega$  CMOS distributed amplifier  
UGBW: 23 GHz, -1dB compr: +5dBm, IP3: +15dBm
- First monolithic CMOS distributed oscillator  
 $f_0$ : 16.3-16.8 GHz,  $L$ : –110dBc/Hz at 1MHz offset
- CMOS will continue to scale into microwave region