Fractal Capacitors

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Outline

- Motivation

- Fractal capacitors

- CAD tool

- Measurements

- Conclusions

Motivation

- Demand for linear capacitors

- Area efficiency

- Improvement with process scaling

- Reduction of bottom-plate capacitance

Traditional Capacitors

- ## Gate Capacitance:

  High capacitance per unit area
  Nonlinear
  Requires DC bias voltage
  Low breakdown voltage
  Medium Q

- ## Junction Capacitance:
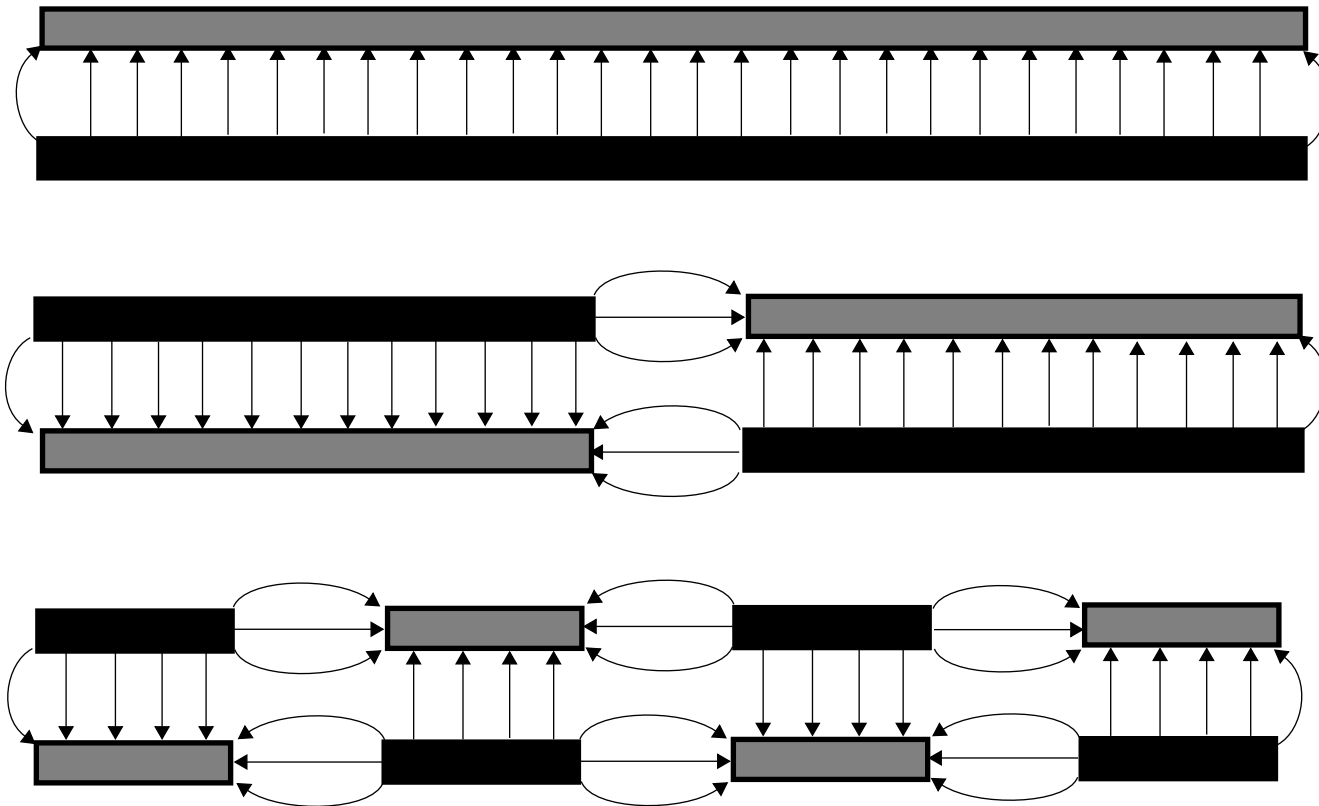
  Highly nonlinear
  Requires DC bias voltage
  Sensitive to process variations
  Low Q
  Large temperature variation

- ## Metal to Metal / Poly Capacitance:

  Linear
  High Q
  Small temperature variation
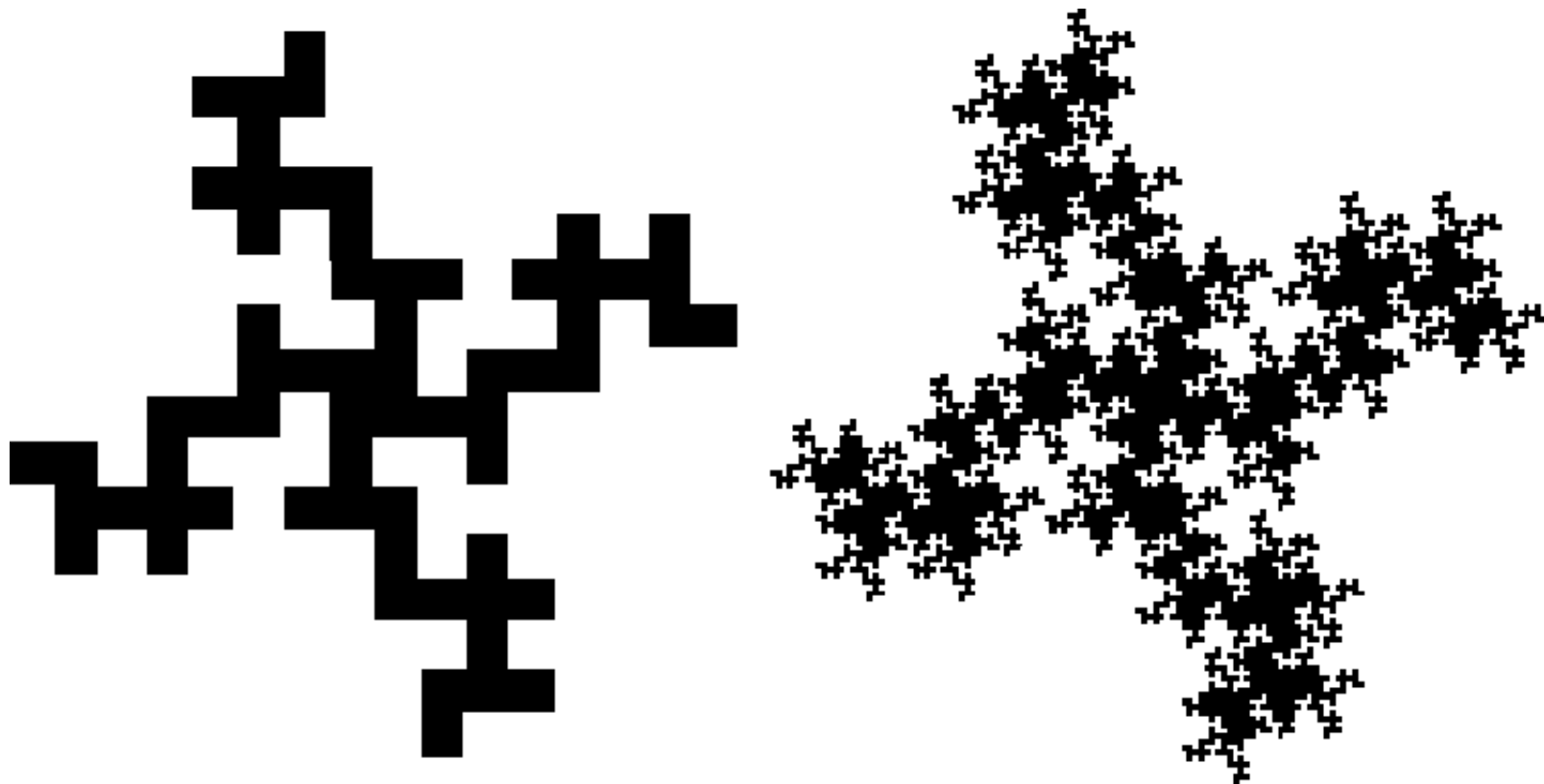 Low capacitance per unit area

Vertical vs. Lateral Flux

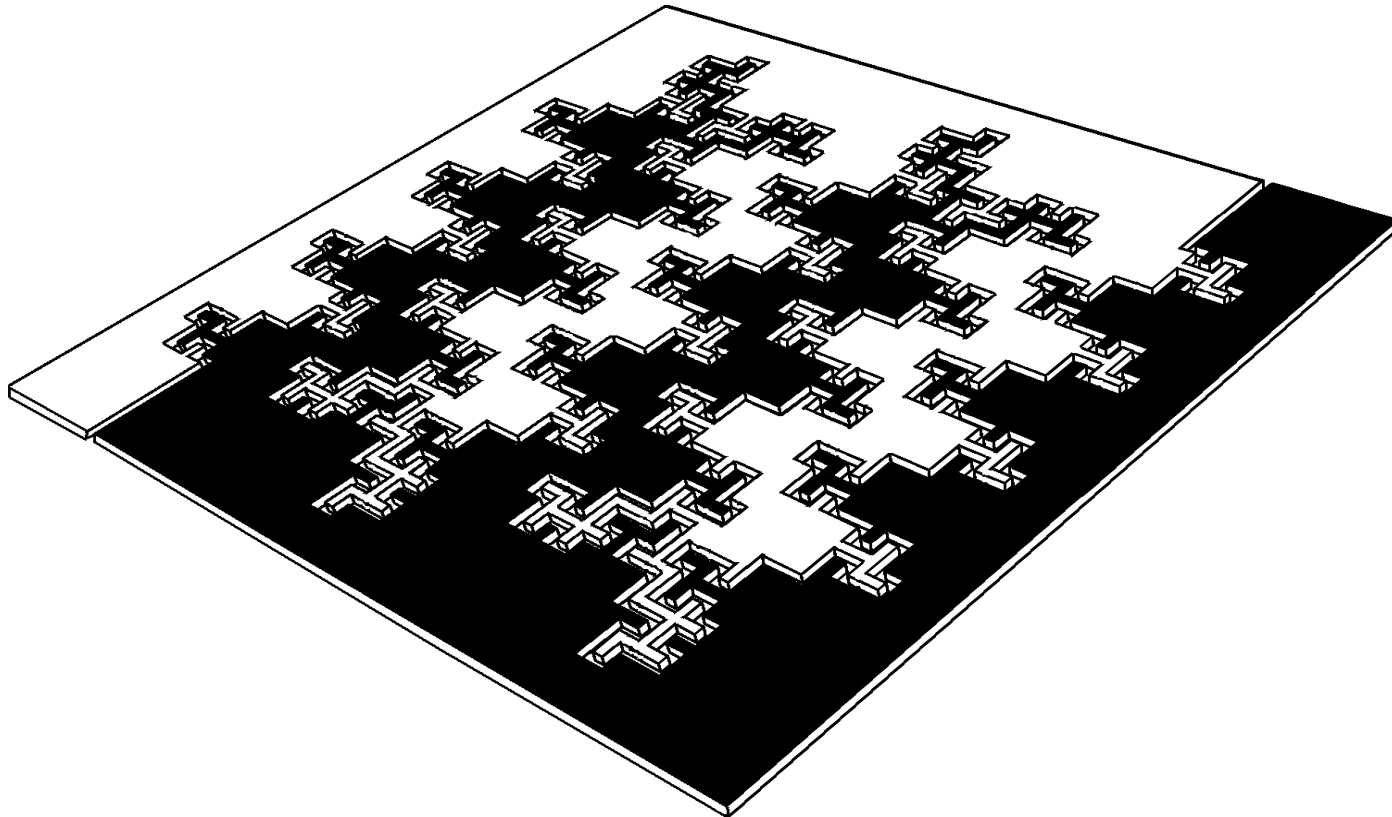- Lateral flux increases the total amount of capacitance.

Fractal Geometries

- Some fractals have finite area but infinite perimeter.
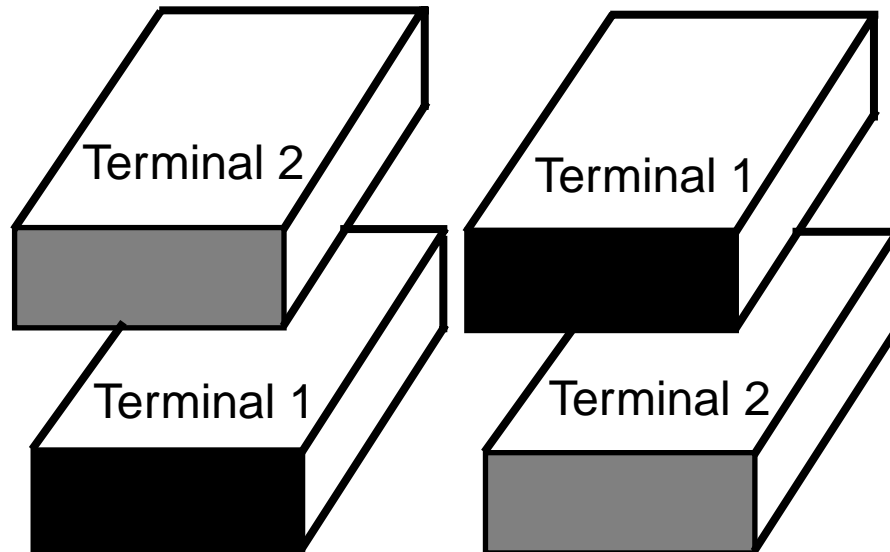
Fractal Capacitor

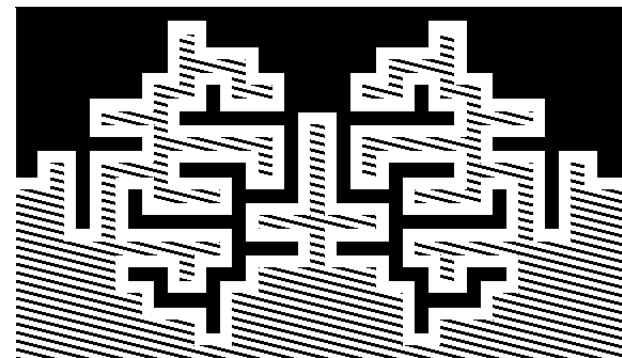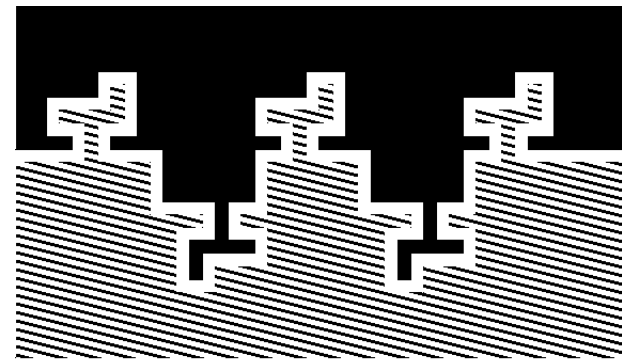- Quasi fractal geometries can be utilized to increase capacitance per unit area.

3-D representation of a fractal capacitor using a single metal layer.
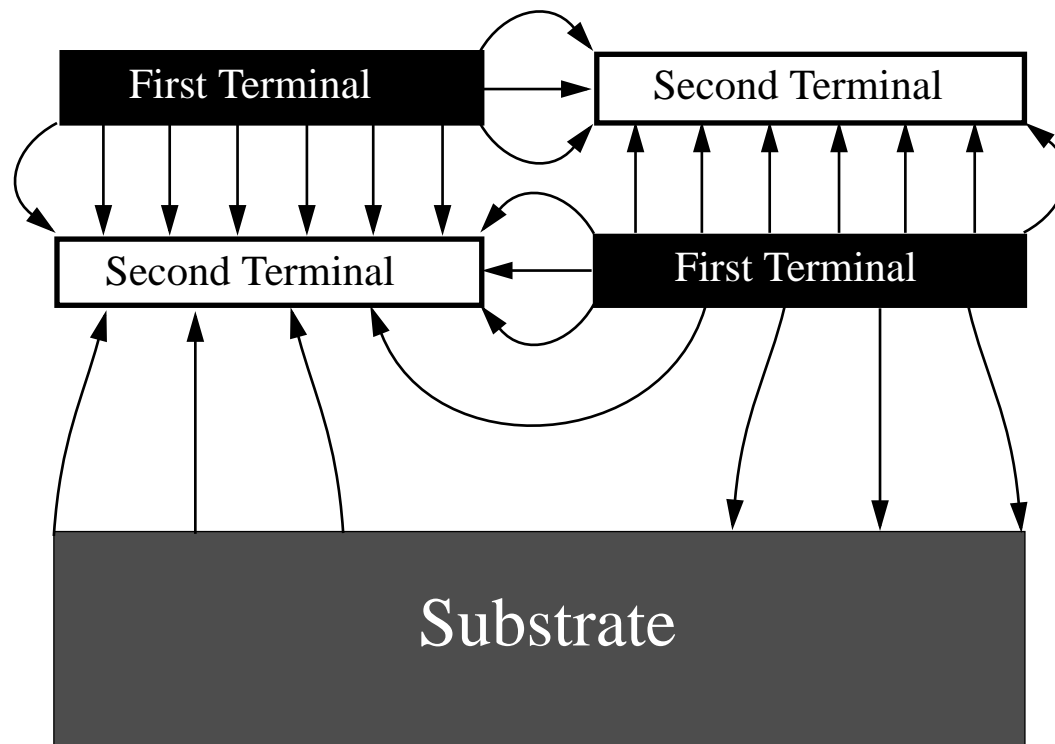
Layout Issues

- Cross connection

- Fractal dimension

Terminal 2
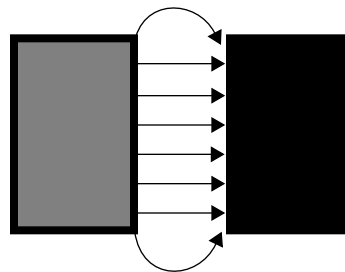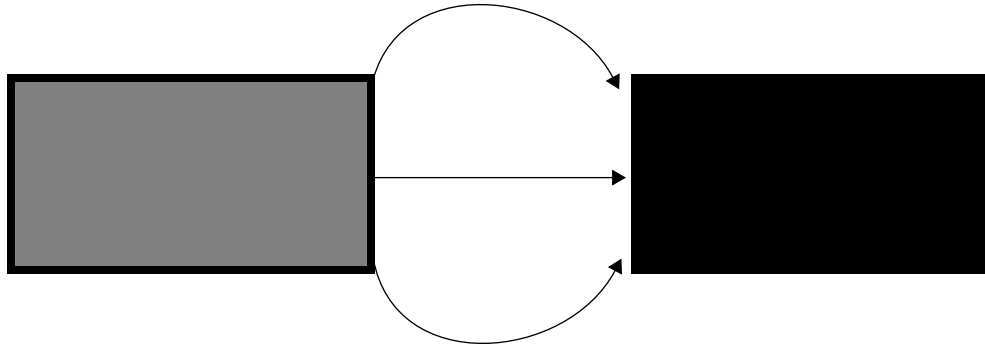
Terminal 1

Terminal 1

Terminal 2

Reduction of the Bottom-Plate Capacitance

- Area is smaller.

- Some of the field lines terminate on the adjacent plate instead of the substrate.

Scaling

- Unlike conventional parallel-plate structures, the capacitance per unit area increases as the process technologies scale.

Other Advantages

- Lateral flux capacitors shift the burden of matching away from oxide thickness to lithography.

- The effect of systematic lithography offset is reduced due to pseudo-random nature of the structure.

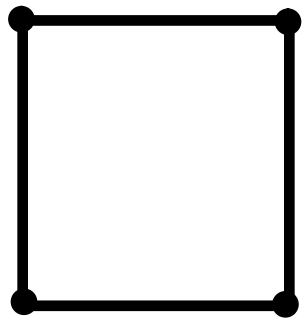- Capacitance density can be traded for lower series resistance.

CAD Tool
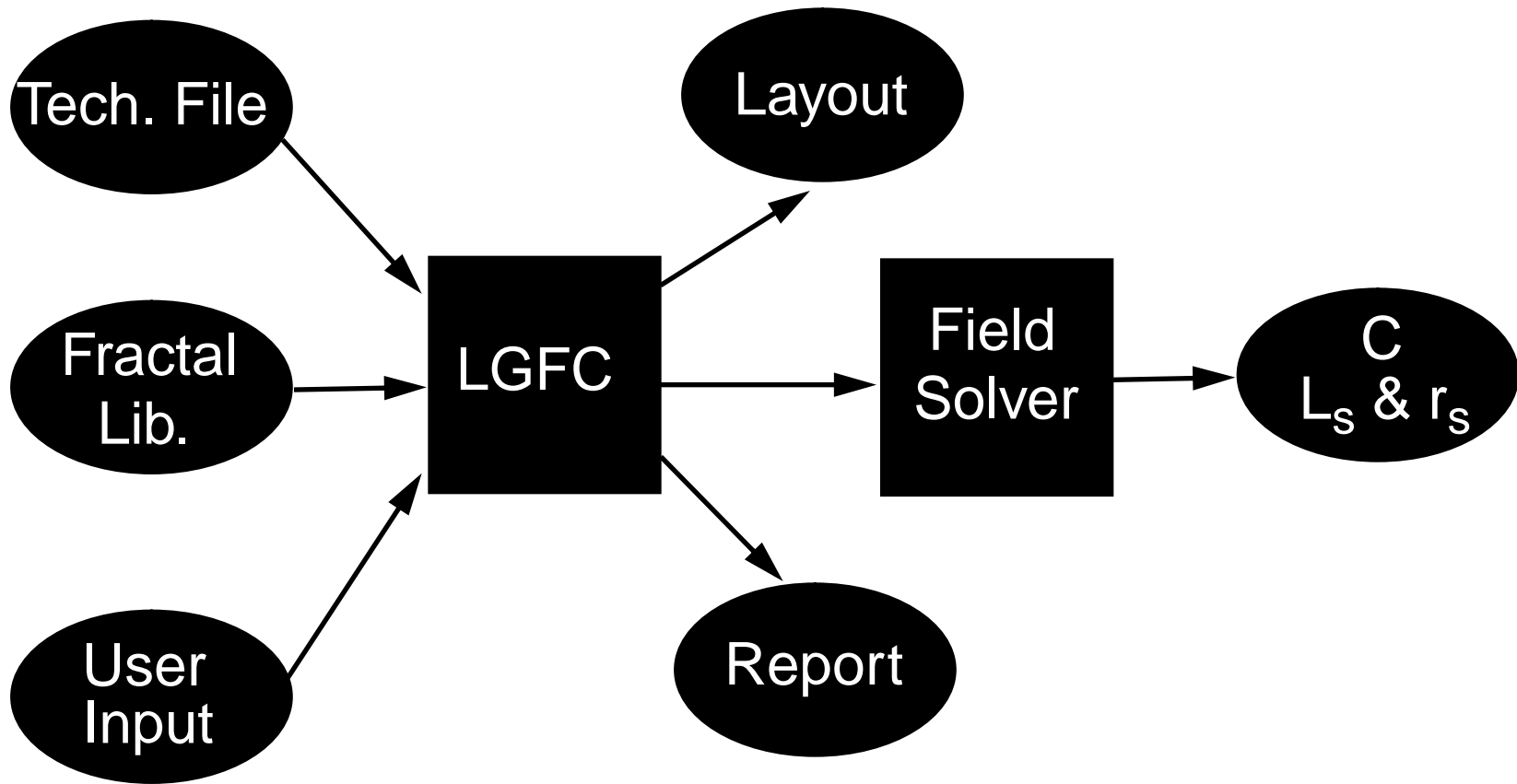
LGFC

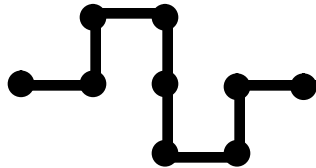Layout Generator for Fractal Capacitors

Fractal Construction: An Example

- Choose an "initiator."

- Replace each segment of the initiator by a "generator."
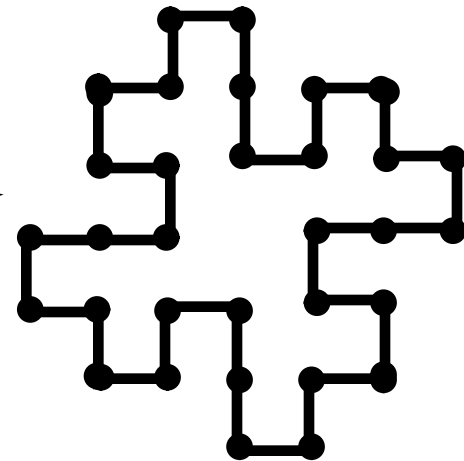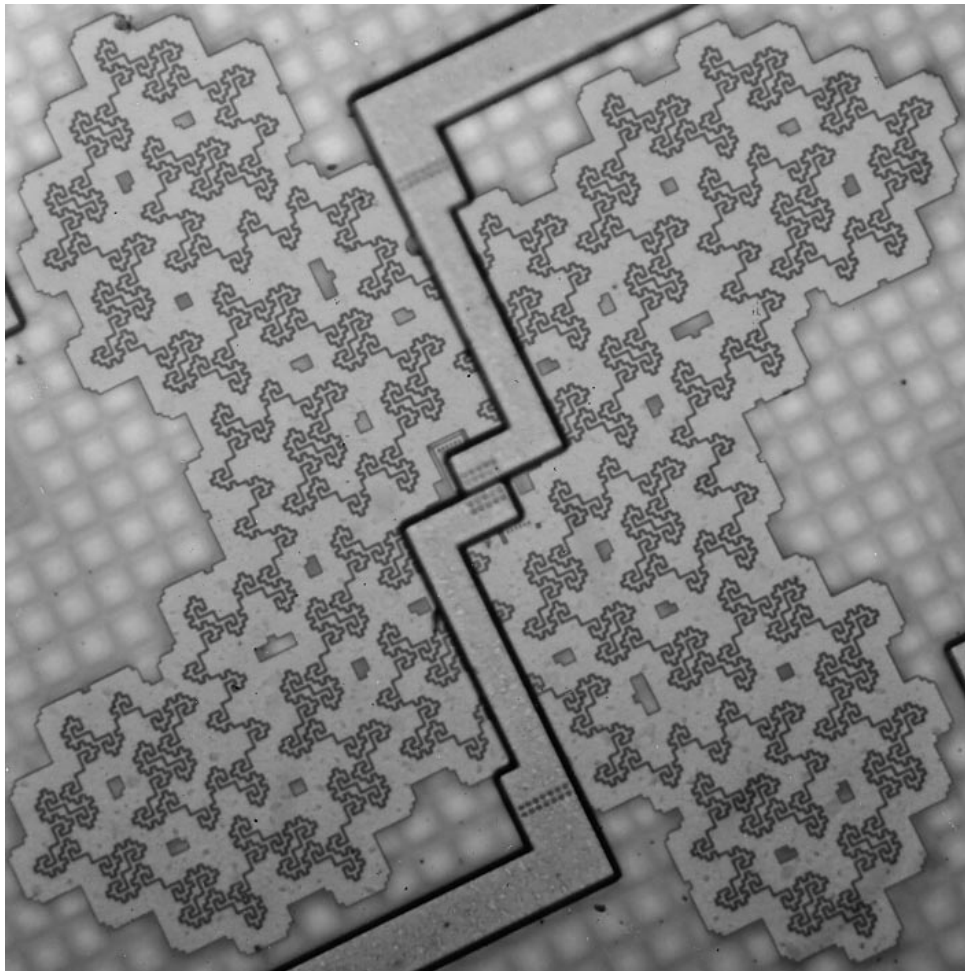
- Continue recursively.

An Initiator   A Generator

$M = 4$ $N=8$, $r=1/4$, $D=log(N)/log(1/r)=1.5$

Die Micrograph


Horizontal spacing=0.6 μm

Vertical spacing=0.8μm
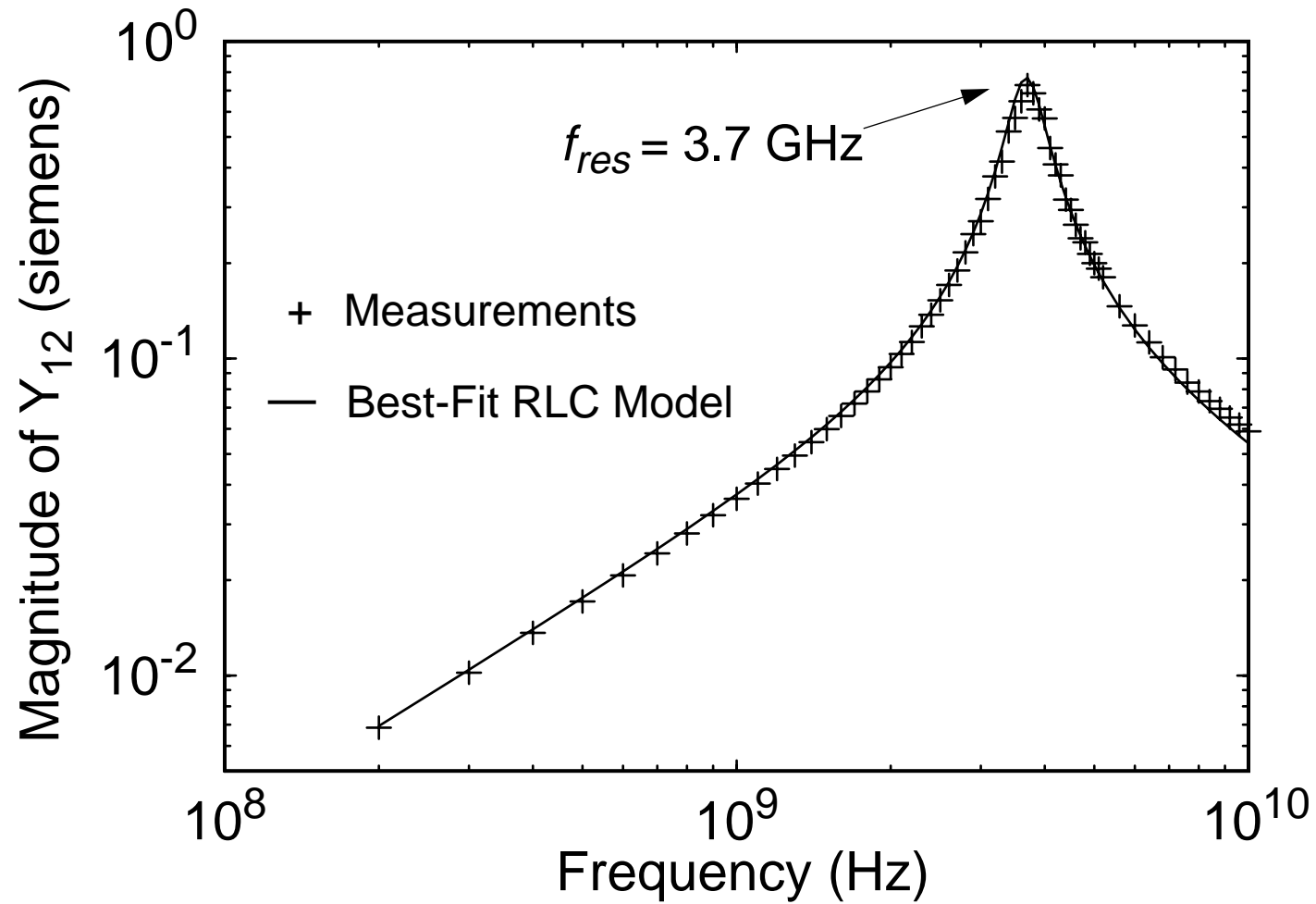
Area=24,000 μm^2

Capacitance Estimation

$$C_{lateral} = K \frac{(\sqrt{A})^D}{(w + s)^{D-1}} \times t$$

- w: Minimum width of the metal.

- s: Minimum spacing between two adjacent strips.

- A: Area of the fractal capacitance.

- t: Thickness of the metal layers.

- K: Proportionality factor that depends on the family of fractals being used.

- D: Fractal dimension.

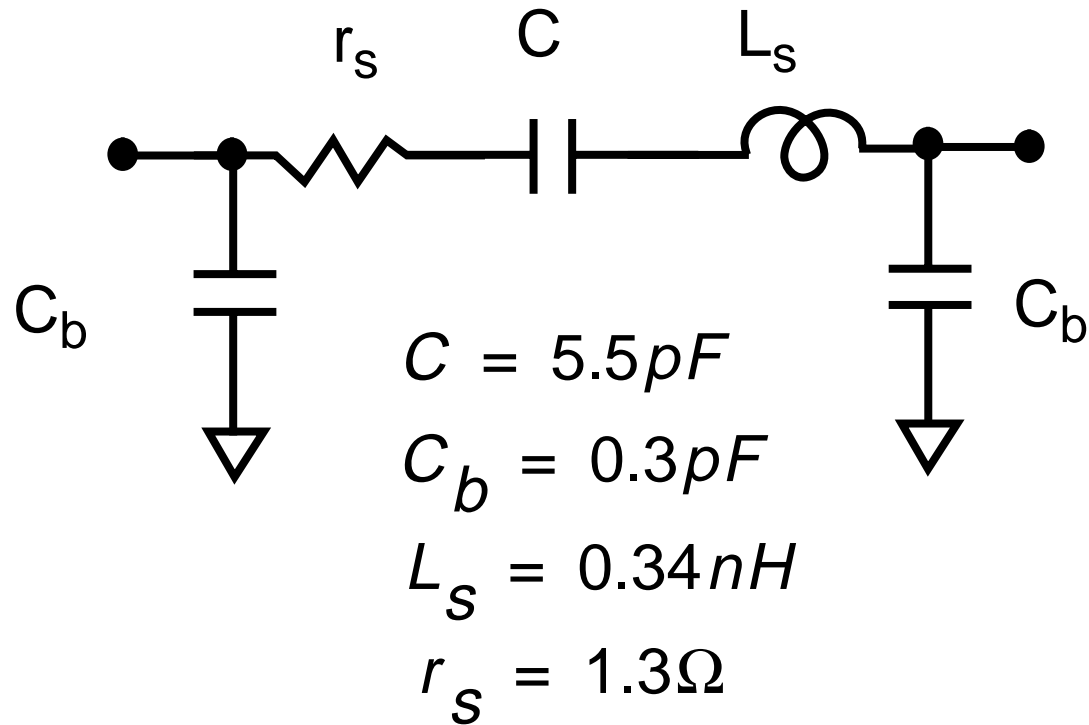# Boost Factor *vs.* Lateral Spacing
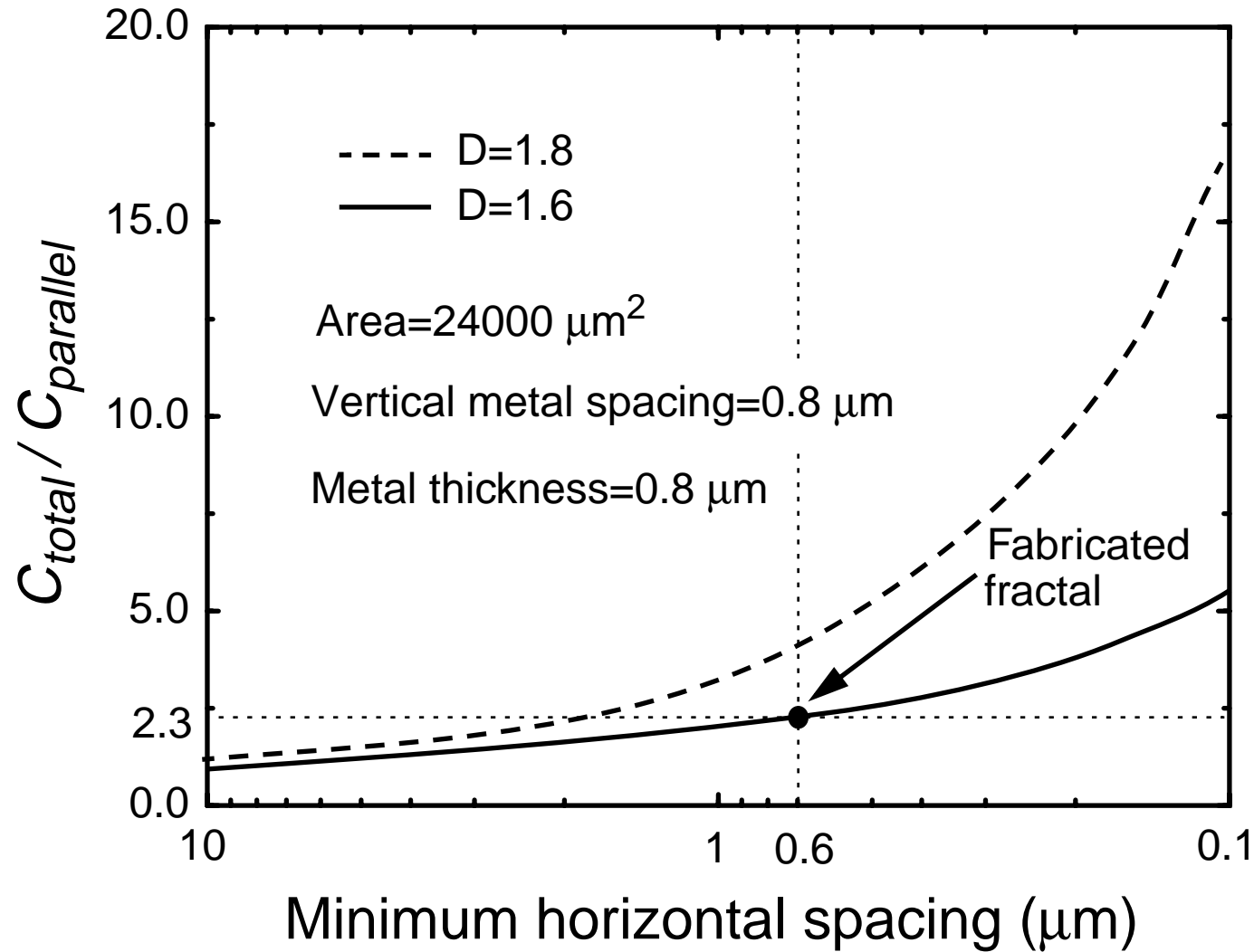
Measurements

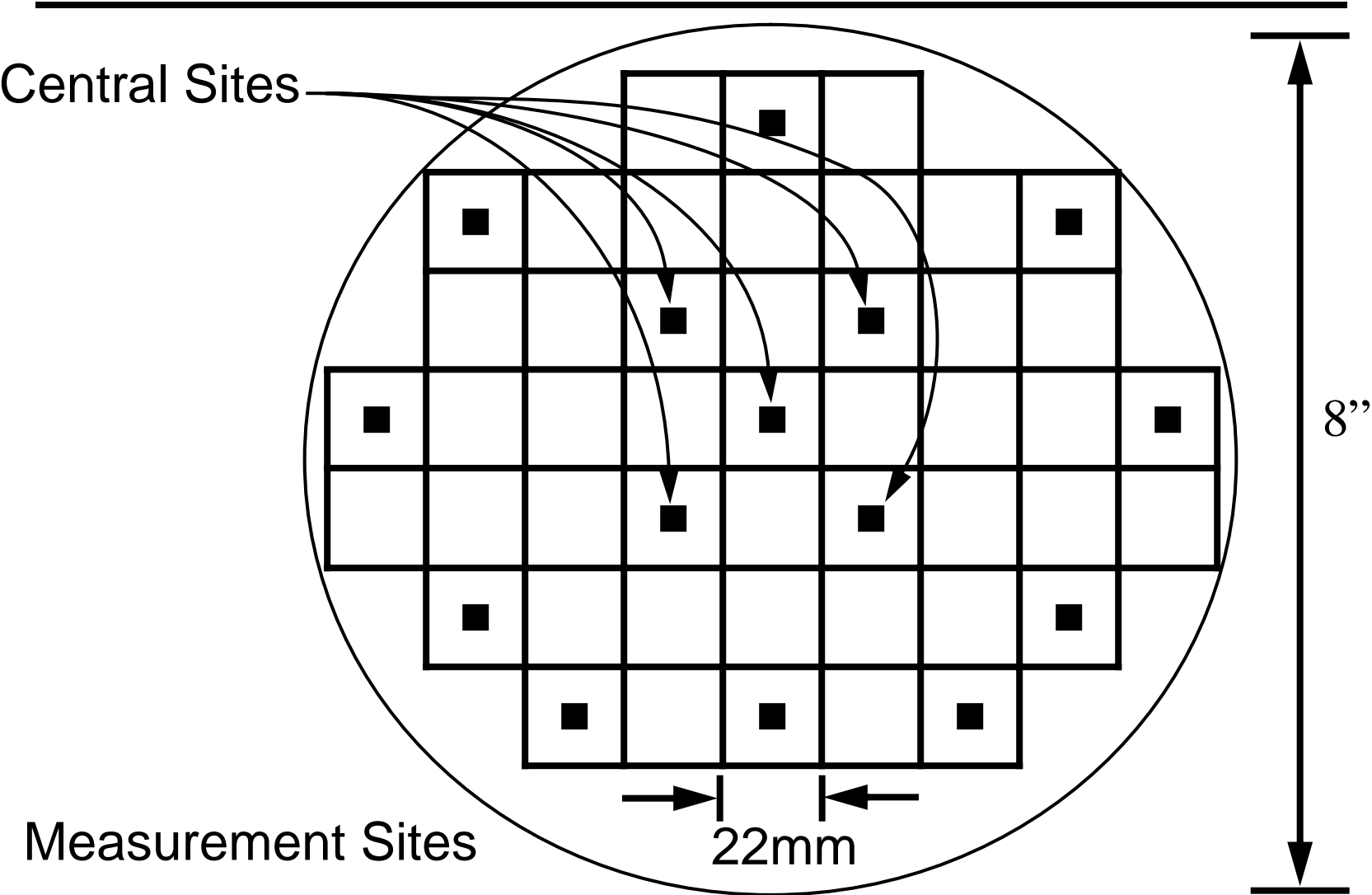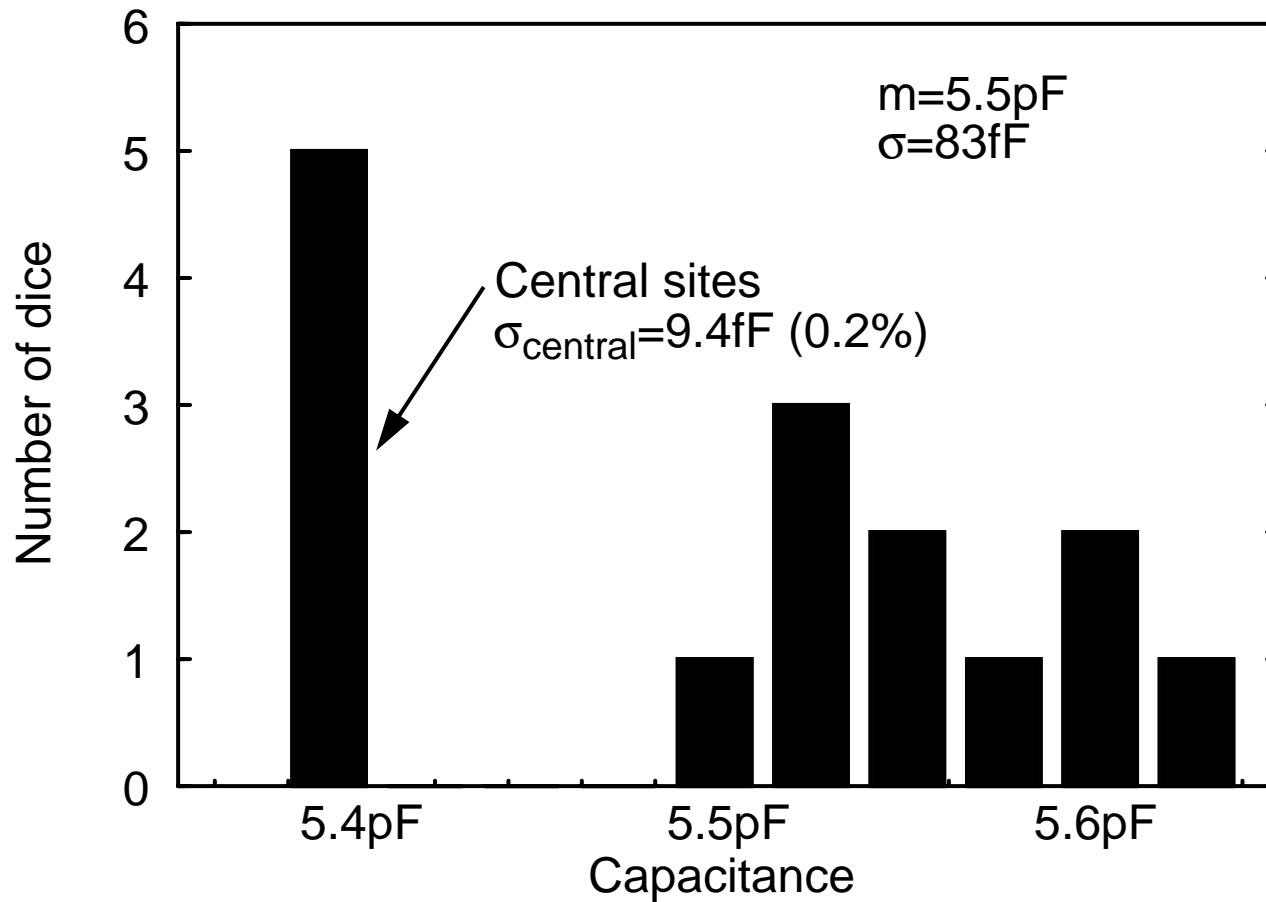High-frequency two-port measurements

Measurements

$C = 5.5pF$

$C_b = 0.3pF$

$L_s = 0.34nH$

$r_s = 1.3\Omega$

Best-Fit Parameters

Measurements

Central Sites

Measurement Sites

22mm

8"

Measurements

Capacitance distribution across the wafer

Measurements

- There is a good agreement between the measurements (5.5pF mean) and the simulations (5.4pF).

- 90% of the measured series inductance is due to connecting stubs.

- About 80% of the series resistance can be attributed to vias and connecting stubs.

- Both series resistance and inductance are dominated by non fundamental mechanisms.

- The overall improvement over a standard parallel plate capacitor is a factor of 2.3.

Conclusions

- Fractal capacitors use chip area more efficiently.

- Fractal capacitors are linear.

- The capacitance density improves with the scaling of process technologies.

- Bottom-plate parasitic capacitance is reduced.

- A CAD tool to automatically generate custom fractal layouts has been developed.