A 1.5mW, 200MHz CMOS VCO for Wireless Biotelemetry

July 30, 1997

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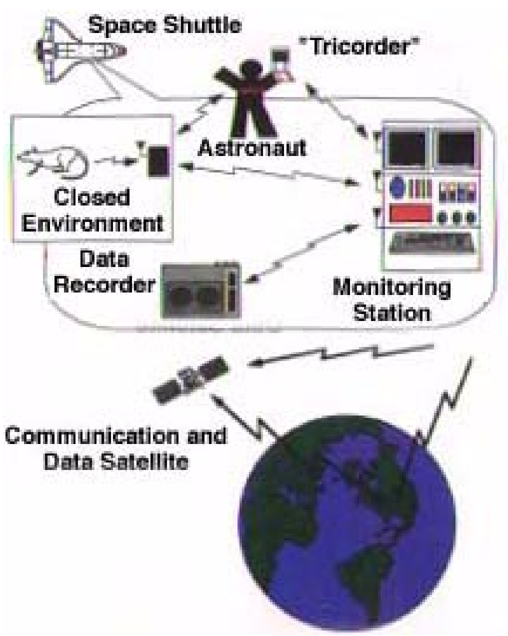
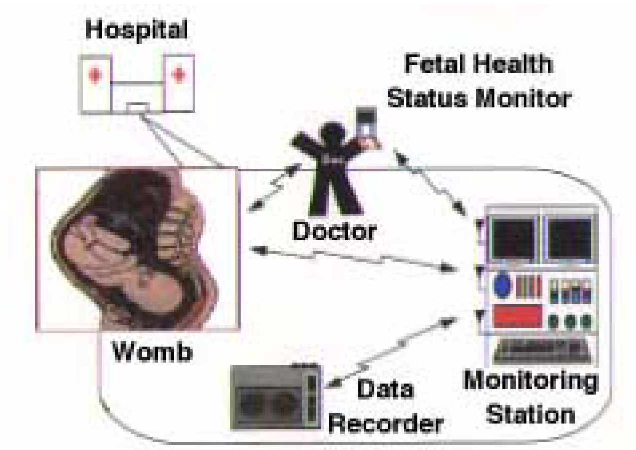
Biotelemetry is Crucial for Space Life Sciences

- On the ground, animals can be housed separately for data collection, and tethered systems are feasible. In space, where volume is very costly, animals must be group-housed, making tethers undesirable.
- *In vivo* experiments often require anesthetized animals and hard-wired connections to the implant, creating a risk of infection due to transcutaneous leads.



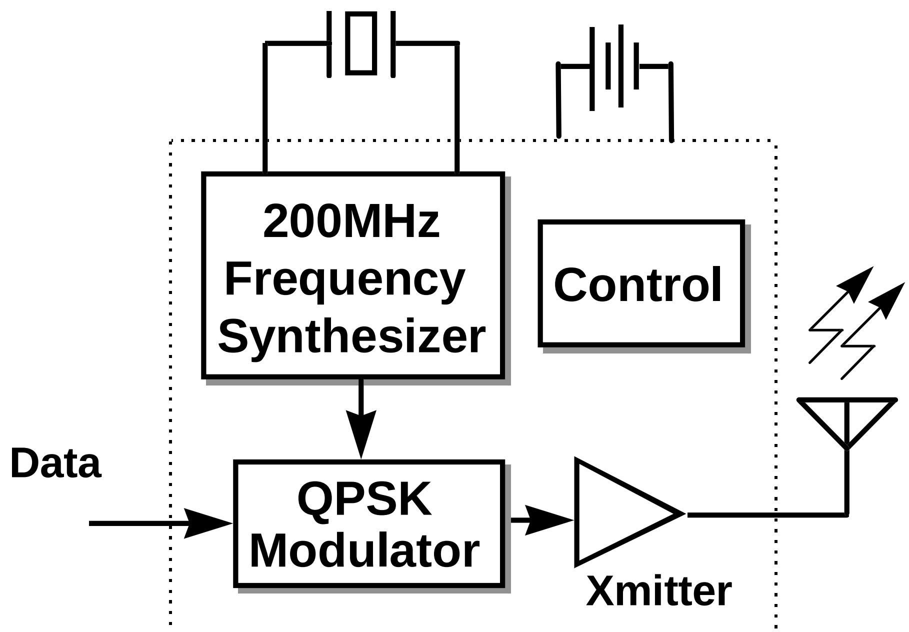
- **NASA-Ames Research Center** is developing the Advanced BioTelemetry System (ABTS) to conduct space-based animal research.
- Implantable biotelemetry supports real-time data gathering. It allows experiments with awake and unrestrained animals, and eliminates problems with lead breakage, movement artifacts, and ground loops.
- **NASA** needs a low power implantable transmitter that can relay biosensor data using the 174-216MHz band.

Human Applications for Biotelemetry



- **NASA** researchers are collaborating with doctors at the **University of California-San Francisco's (UCSF) Fetal Treatment Center** to adapt space biosensor and biotelemetry technology for the monitoring of fetuses with life-threatening congenital conditions.
- At **UCSF's Fetal Treatment Center** there is a need for telemetry of physiological parameters of human fetuses for monitoring and identifying distress after surgery.
- A telemetry implant that will monitor heart rate, temperature, pH, and amniotic fluid pressure is required to operate *in utero* for up to 3 months.

Goal: An Implantable Biotelemetry Transmitter

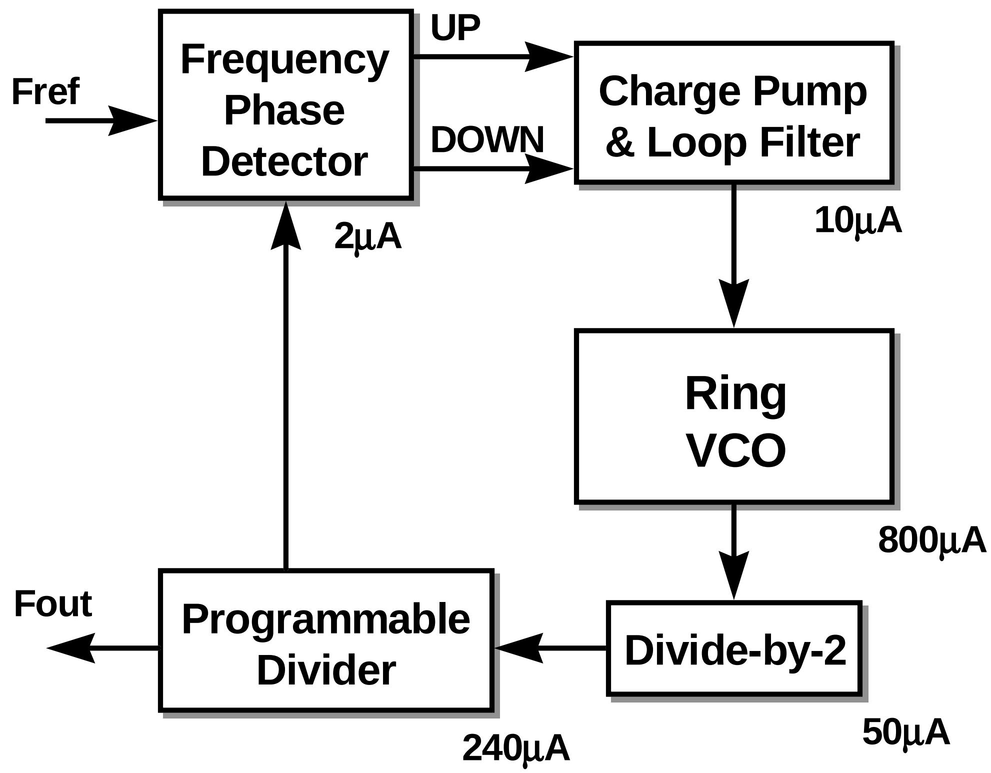


- Frequency: 174-216MHz
- Data Rate: 100 kbps
- Modulation: Quadrature Phase Shift Keying (QPSK)
- Range: 1 meter
- Power source: 3.6 V, 750mAH lithium
- Implant lifetime: 100 hours (continuous)
- Implant volume: 5 cm^3 (including battery)

Our goal is to design and build a low-power radio transmitter in CMOS suitable for short range biosensor and implantable use.

Phase-locked Loop Frequency Synthesizer

- The most important parameter of an implanted biotelemetry system is power dissipation.
- A significant portion of the power budget is allocated to the generation of the RF carrier.
- Traditionally, frequency synthesizers have been implemented using phase-locked loops (PLLs).
- The major sources of power dissipation are the VCO (73%) and the frequency divider (22%).

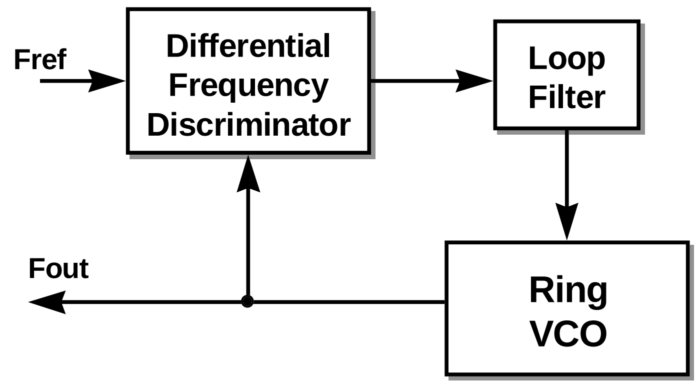


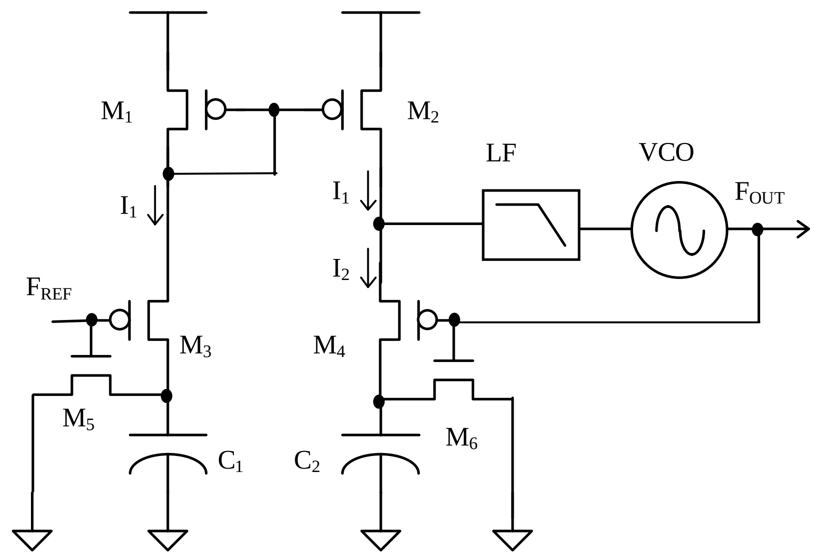
Power budget for a typical CMOS PLL frequency synthesizer used in microprocessor clock generation[1].

[1] V. Kaenel, et al., "A 320MHz, 1.5mW at 1.35V CMOS PLL for Microprocessor Clock Generation", *Intl. Solid-State Circuits Conference*, Feb. 1996, pp.132-133.

Frequency-locked Loop Frequency Synthesizer

- We describe a frequency-locked loop (FLL) architecture that uses a differential frequency discriminator (DFD).
- This FLL does not require a frequency divider, which represents 22% of the power budget for the PLL example just shown.
- The FLL can perform frequency comparison directly without a divider by using a DFD implemented with switched capacitor circuits.
- The output frequency is determined by the capacitor ratio, C1/C2, and the reference frequency.
- A linear analysis using a single pole filter shows that this is a first order system, and thus inherently stable (neglecting sampled-data effects).



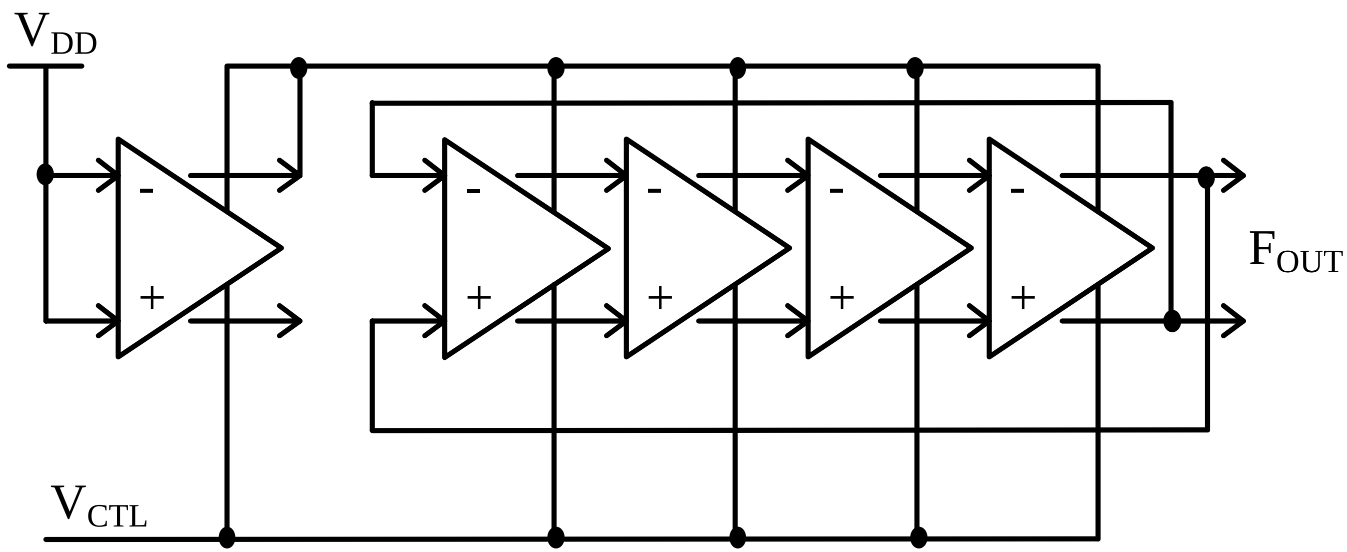


$$F_{OUT} = F_{REF} \cdot \left(\frac{C_1}{C_2}\right)$$

Voltage-controlled Oscillator Design

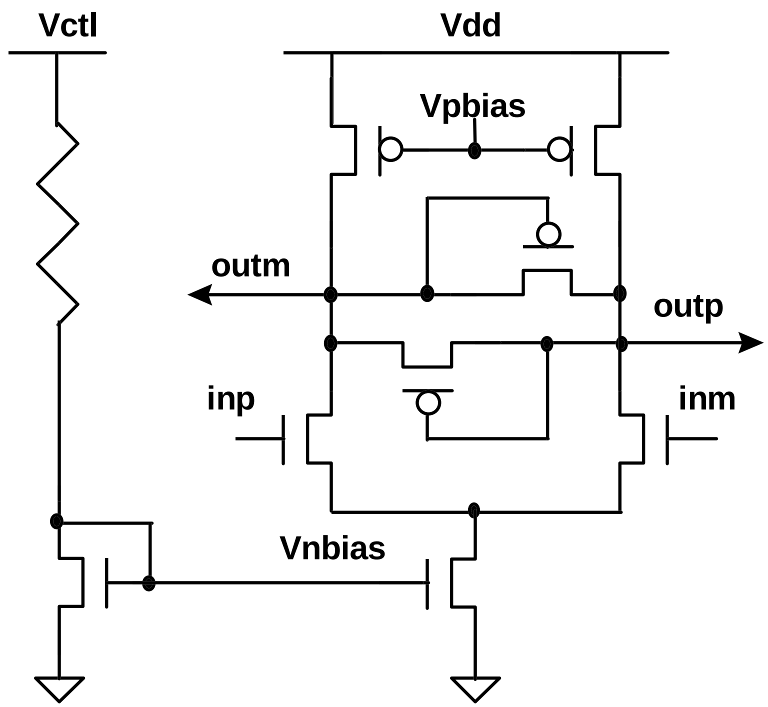
- In a synthesizer application, the reference frequency source is usually a crystal oscillator with very low phase noise.
- A PLL tracks the phase noise of the reference signal, relaxing the close-in phase noise requirements of the VCO.
- However, a FLL tracks the VCO’s frequency, not phase, forcing more stringent requirements on the VCO.
- The VCO’s power dissipation is determined by the frequency of operation and the phase noise performance required.
- In biotelemetry, data rates are low (10-100kbps), and channel spacing wide (4MHz), relaxing the phase noise requirements for the VCO.

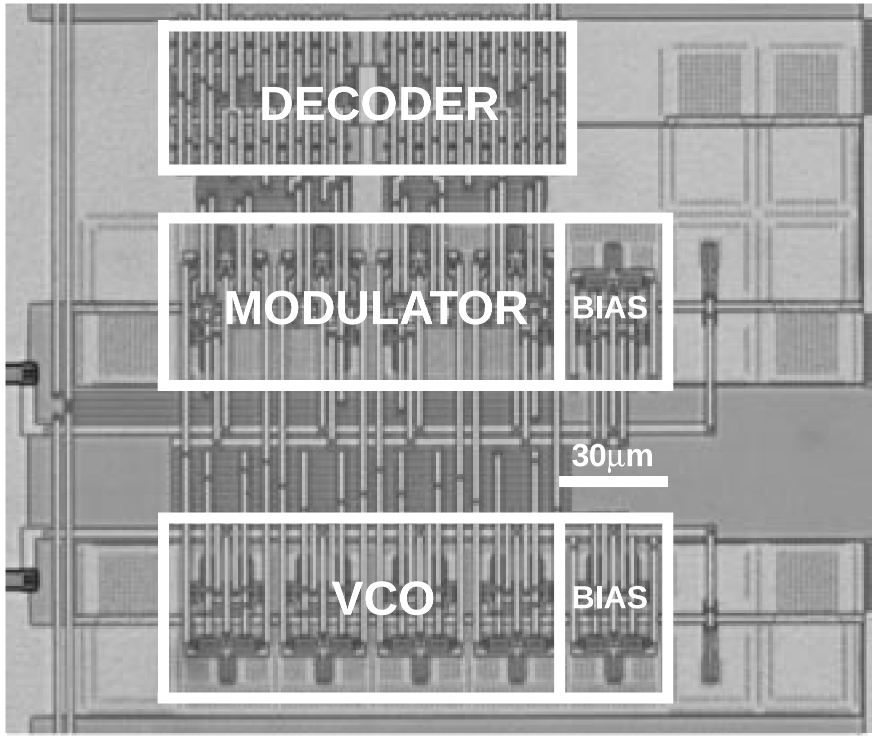
Voltage-controlled Oscillator Design



- The VCO design is critical in the performance of the FLL synthesizer as the phase noise at the output of the FLL is solely a function of the phase noise of the VCO.
- The VCO consists of a 4-stage differential ring oscillator.
- Frequency control is achieved by changing the biasing of the buffer stages which determines the delay through each cell.

Differential Delay Buffer Design





- The differential buffers used have been shown to have excellent noise and power supply rejection characteristics[2].
- The layout of the ring oscillator is symmetrical and load balanced to avoid any skewing between the phases.

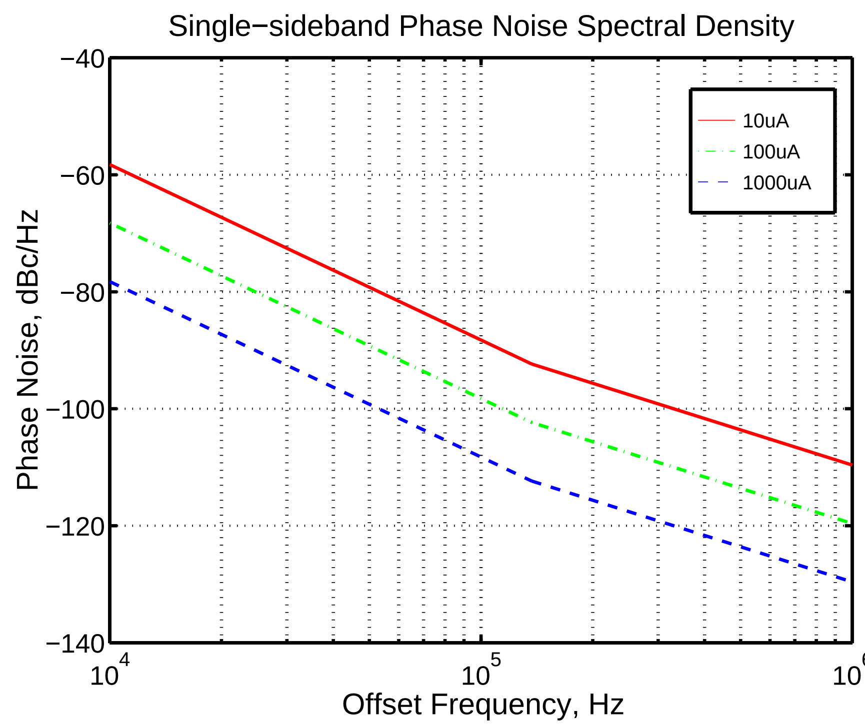
[2] M. Horowitz, et al., "PLL Design for a 500MB/s Interface", *Intl. Solid-State Circuits Conference*, Feb. 1993, pp.160-161.

Hajimiri Phase Noise Model

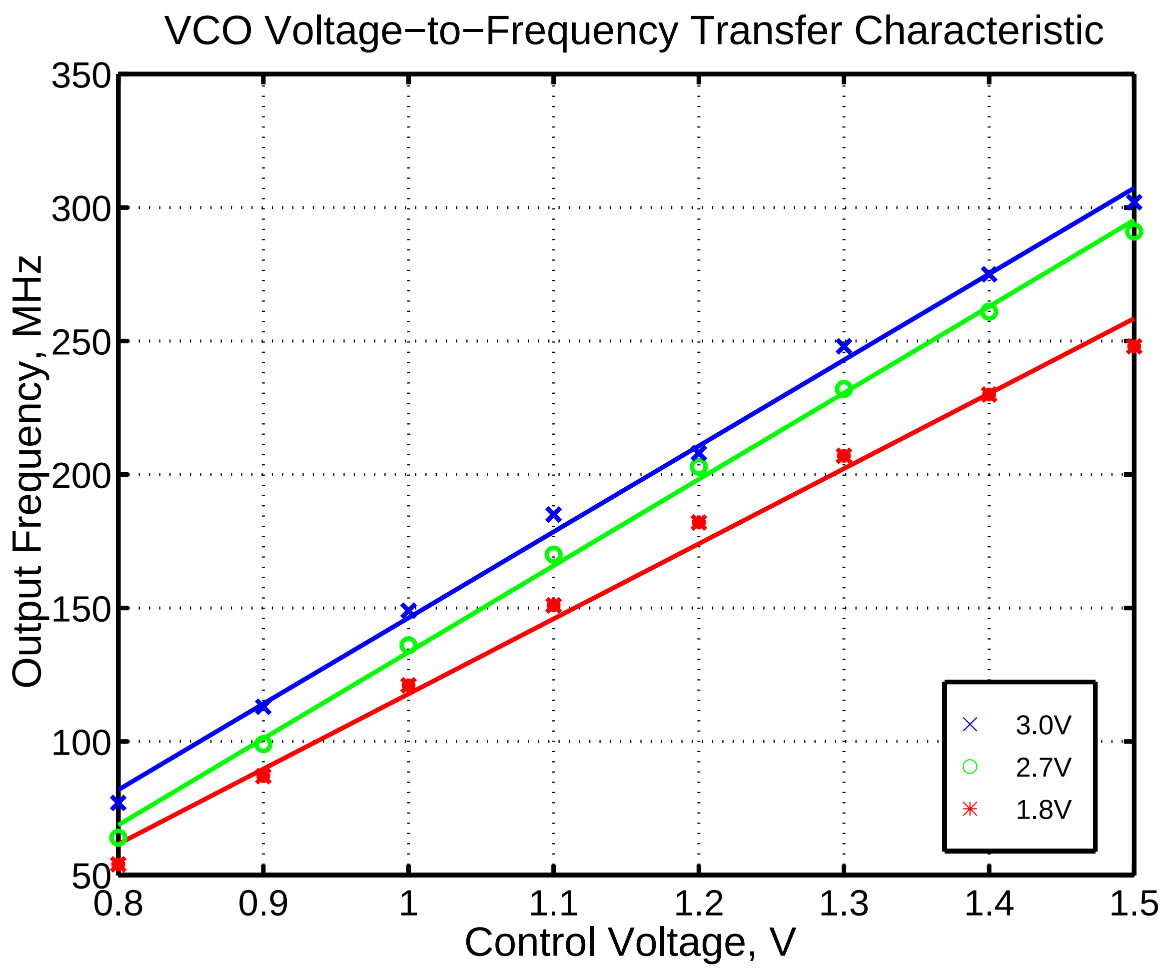
$$L\{\Delta\omega\} = 10 \cdot \log\left\{\frac{64kT}{I_{DD}E_C L_{EFF}}\left(\frac{f_o^2}{\Delta\omega^2}\right)\right\}$$

Single-sideband phase noise (dBc/Hz) for a differential ring oscillator in the 1/f^2 region

- I_{DD} is the tail current of a single stage
- E_C is the critical field (e.g., 4.918 V/µm)
- L_{EFF} is the gate length of the differential-pair devices (e.g., 0.5µm)
- We selected the 100µA curve, for a total current drain of 500µA at 200MHz.

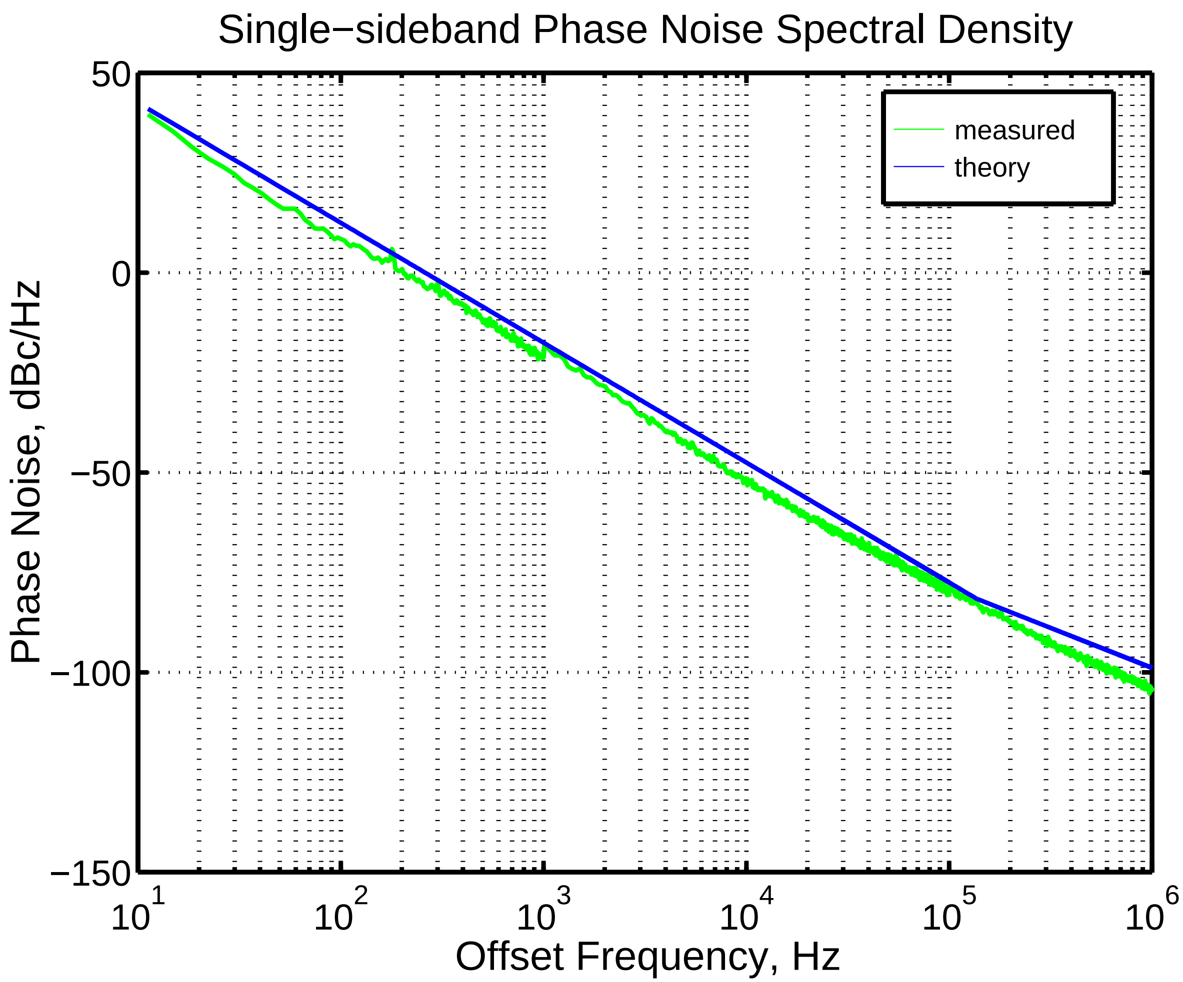


Test Results: VCO Transfer Characteristic



- Fabricated through MOSIS using the HP 0.5µm CMOS process.
- The VCO voltage-to-frequency transfer characteristic was measured for different supply voltages.
- Tuning Range: 350kHz-707MHz @3V
- VCO Gain = 321MHz/V @3V

Test Results: Phase Noise

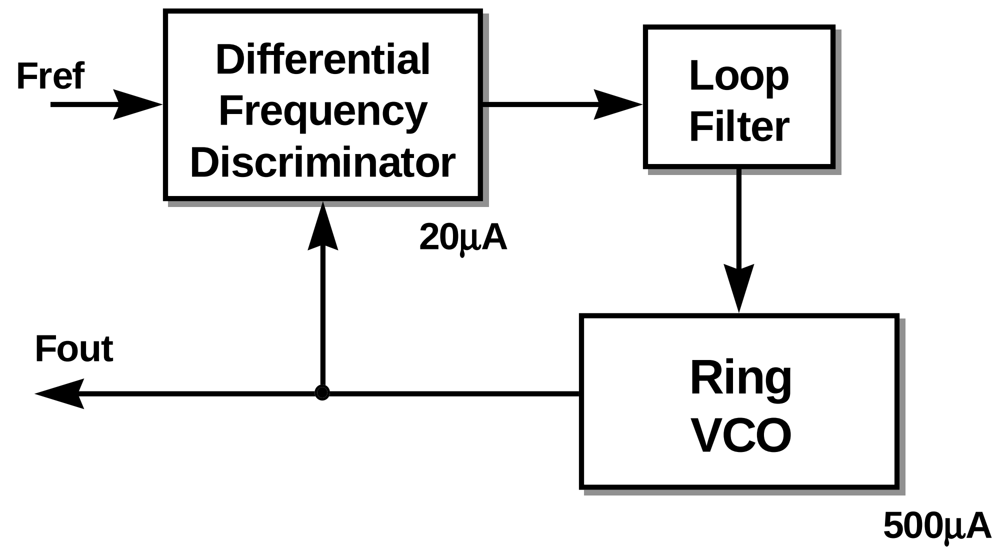


- Using an HP8590B spectrum analyzer, the phase noise was measured at -82dBc/Hz for 100kHz offset from a 200MHz carrier.
- These measurements are within 2dB of the predicted values for frequency offsets between 10Hz and 1MHz.

Test results using RDI's NTS-1000A phase noise measurement test set, along with the theoretical phase noise performance predicted by the Hajimiri model (f_c=150.9MHz).

Conclusions

- The frequency-locked loop (FLL) synthesizer imposes more stringent phase noise requirements on the VCO.
- A design technique using the Hajimiri phase noise model was presented.
- A 200MHz ring oscillator VCO was designed and fabricated in 0.5µm CMOS.
- Measurements of phase noise show good agreement with the theory.



Acknowledgements

- This work was partially supported by NASA-Ames Research Center through a Training Grant No. NGT 2-52211.
- We gratefully acknowledge the support of John W. Hines, manager of the Sensors 2000! program at NASA-Ames Research Center.