A 12.4mW CMOS Front-End for a 5GHz Wireless-LAN Receiver

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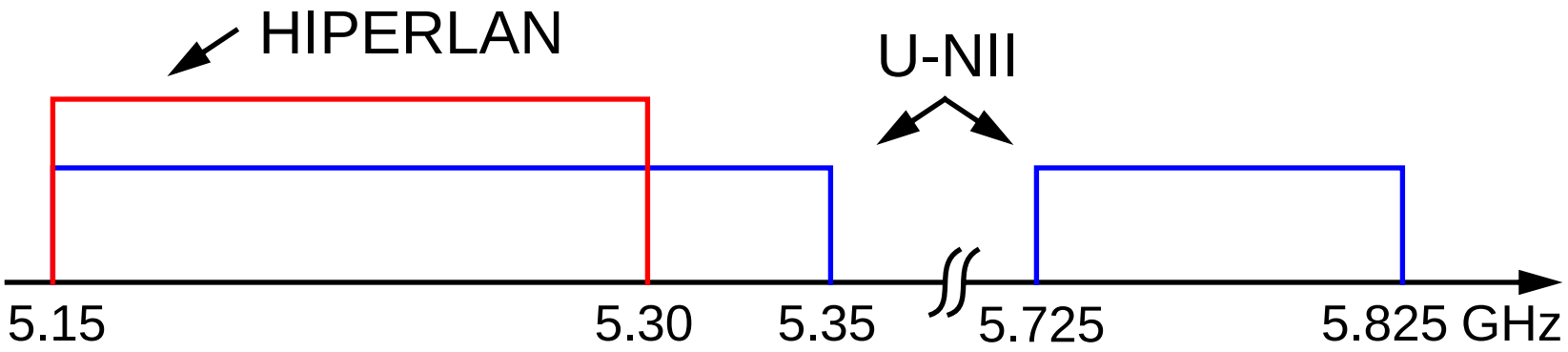
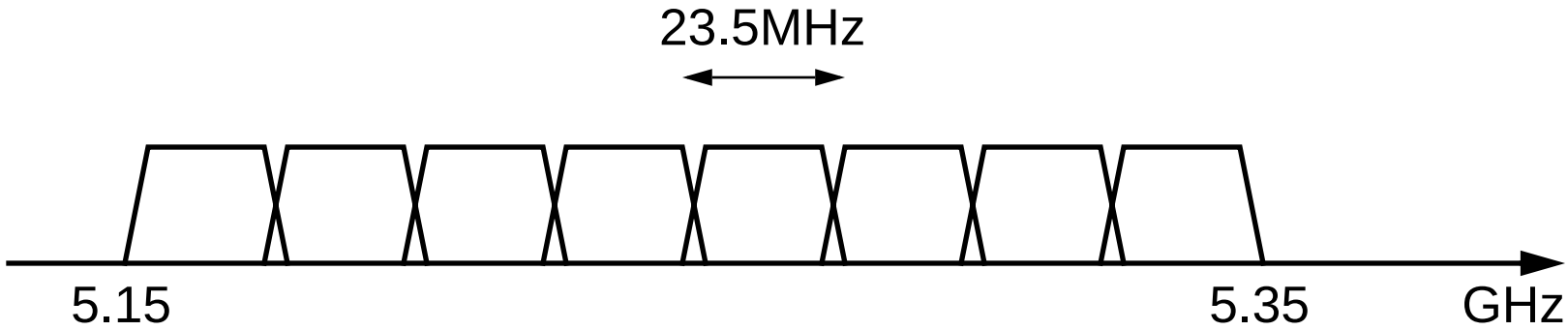
Outline

- Introduction
- Receiver Architecture
- Circuit Implementation
- Measurements
- Conclusion

Available Frequency Bands



- U-NII and HIPERLAN frequency bands.



- Proposed channel allocation for a U-NII band WLAN system.

  →Compatible with HIPERLAN.

Dynamic Range Requirements

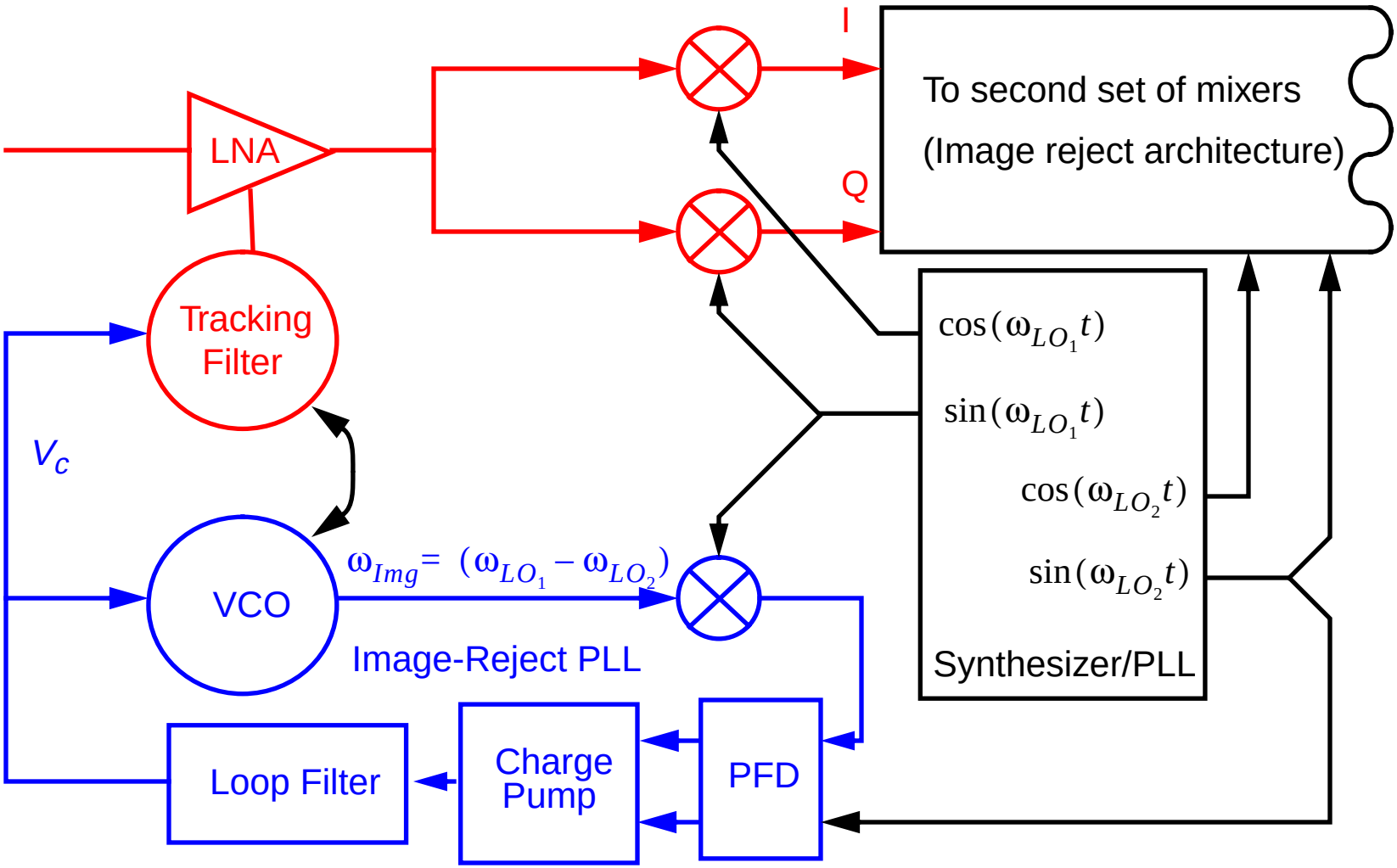
- Signal levels as high as -20dBm
- Signal levels as low as –148dBm/Hz (–74dBm for a 23.5MHz channel)

NF < –148dBm/Hz – 12dB – (–174dBm/Hz)=14dB

Pre-detection SNR

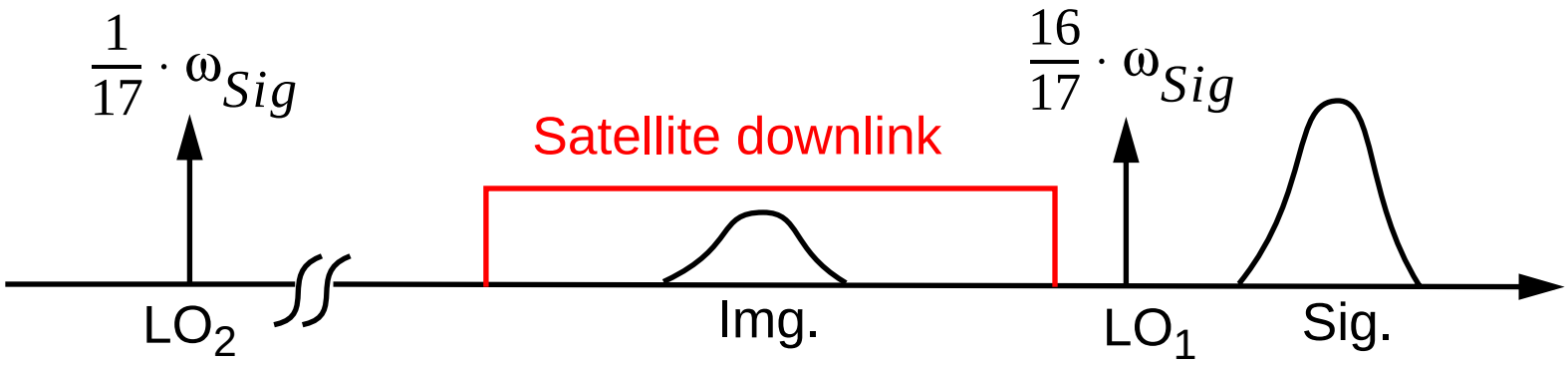
Available noise power of the source

Receiver Architecture

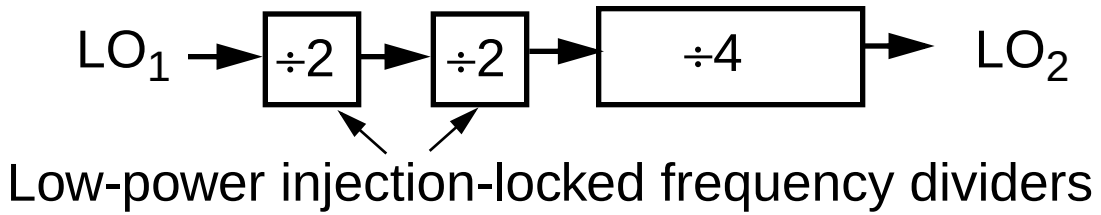


Synthesizer Architecture

To be presented at Symp. on VLSI Circuits, Session 12.1.

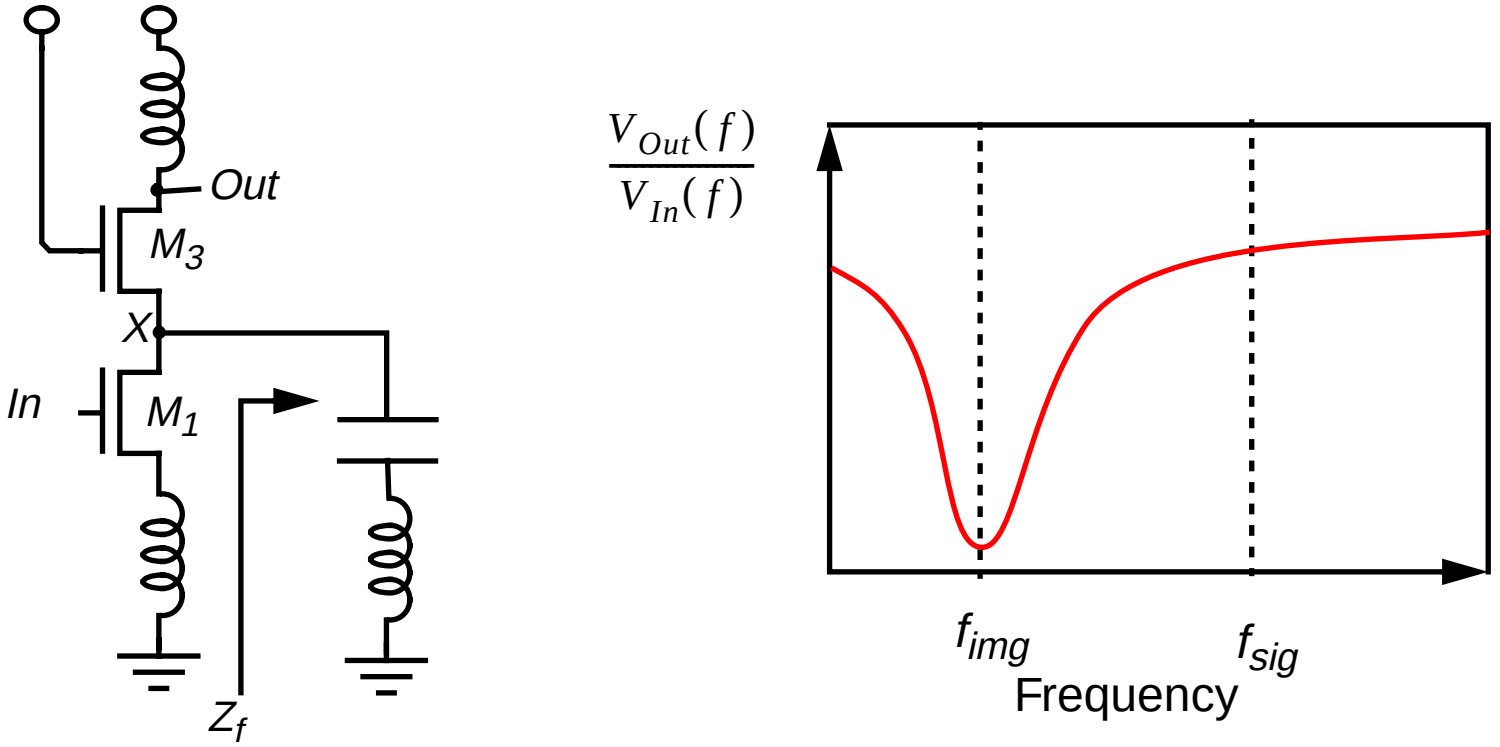


- Image signal is small.



- LO_2 easily obtained from LO_1.

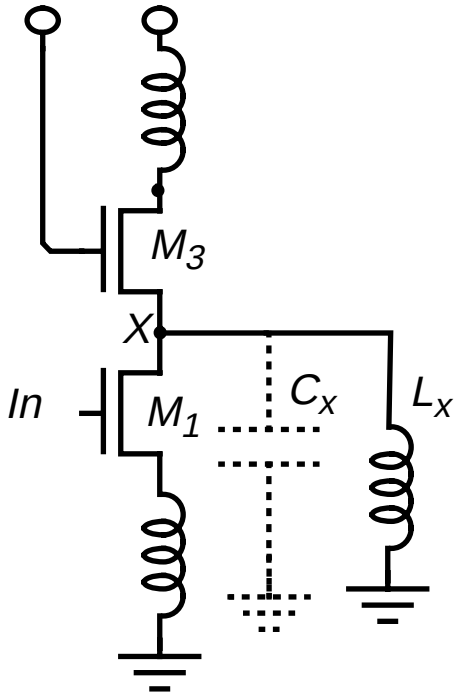
Image Rejection

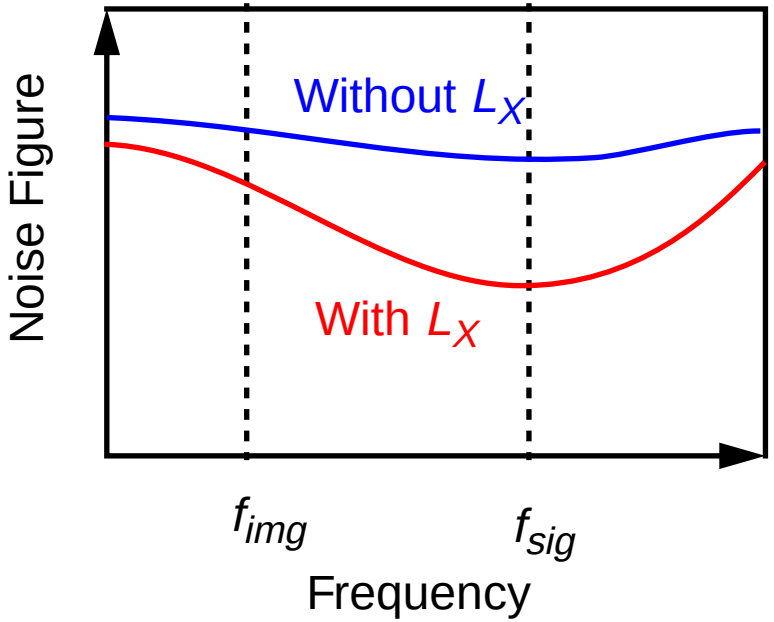


- Series resonance @f_{Img}→ improves image rejection

Noise Rejection

Parasitic capacitance C_X degrades the noise performance.





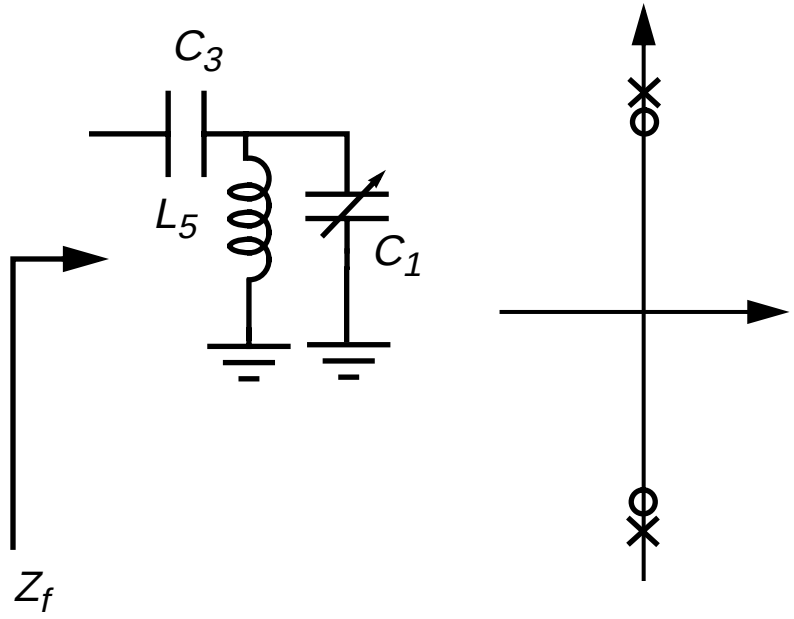
- Parallel resonance @f_{Sig}→ improves noise figure

Solution: Third-Order Filter

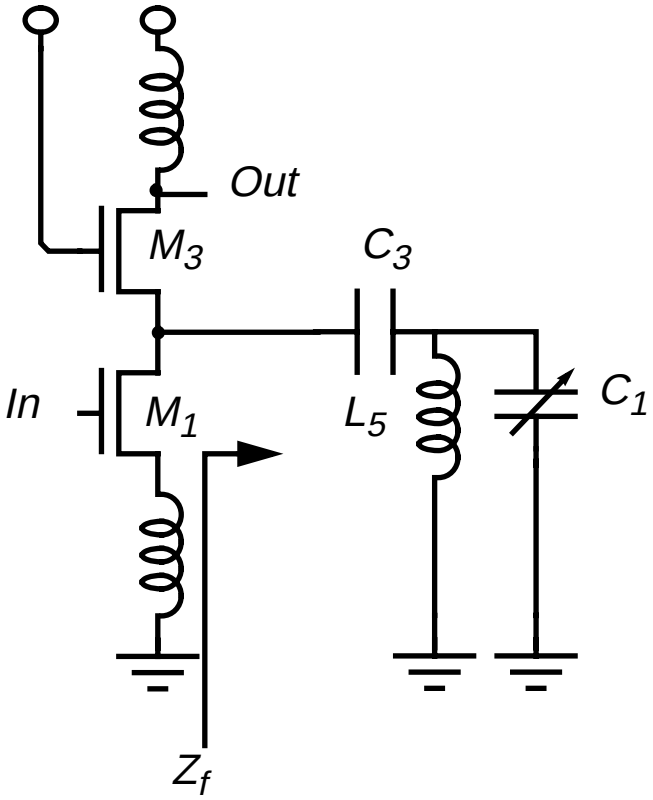
$$Z_f(s) = \frac{L_5 \cdot (C_3 + C_1) \cdot s^2 + 1}{C_1 \cdot C_3 \cdot L_5 \cdot s^3 + C_3 \cdot s}$$

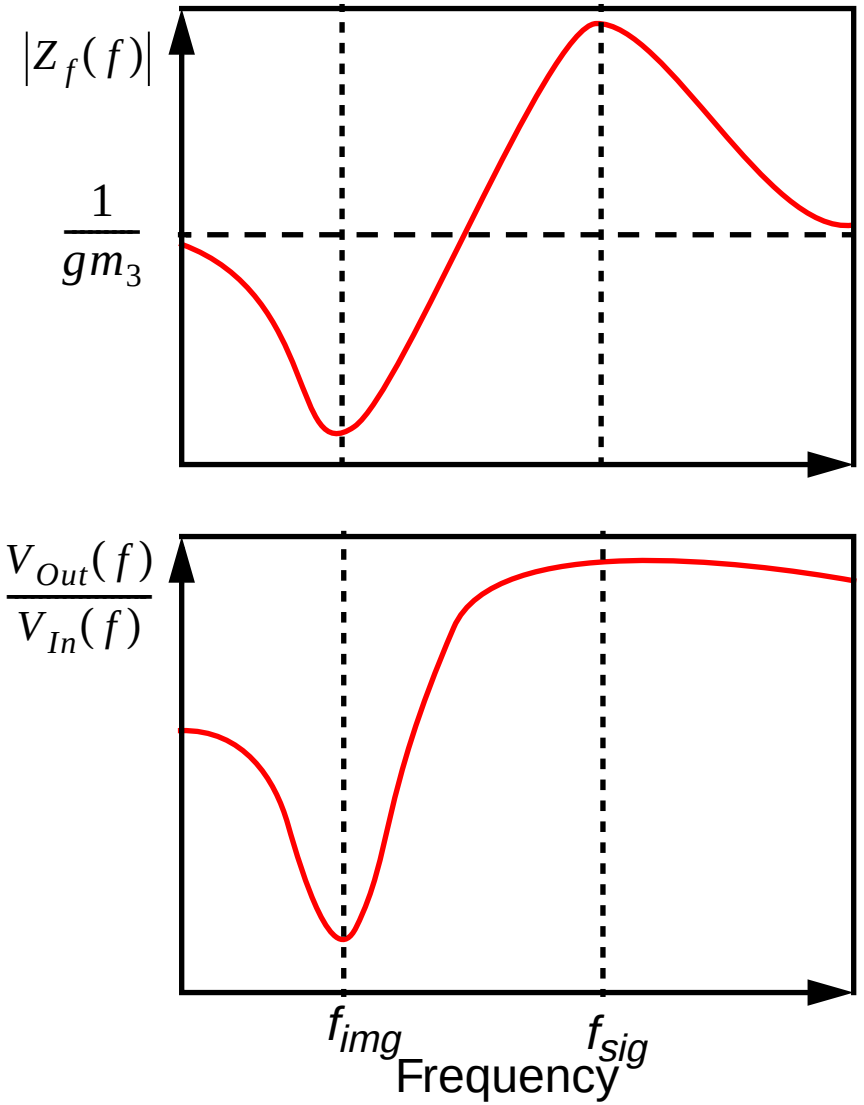
$$\omega_z = \pm \frac{1}{\sqrt{L_5 \cdot (C_3 + C_1)}}$$

$$\omega_p = \pm \frac{1}{\sqrt{L_5 \cdot C_1}}$$

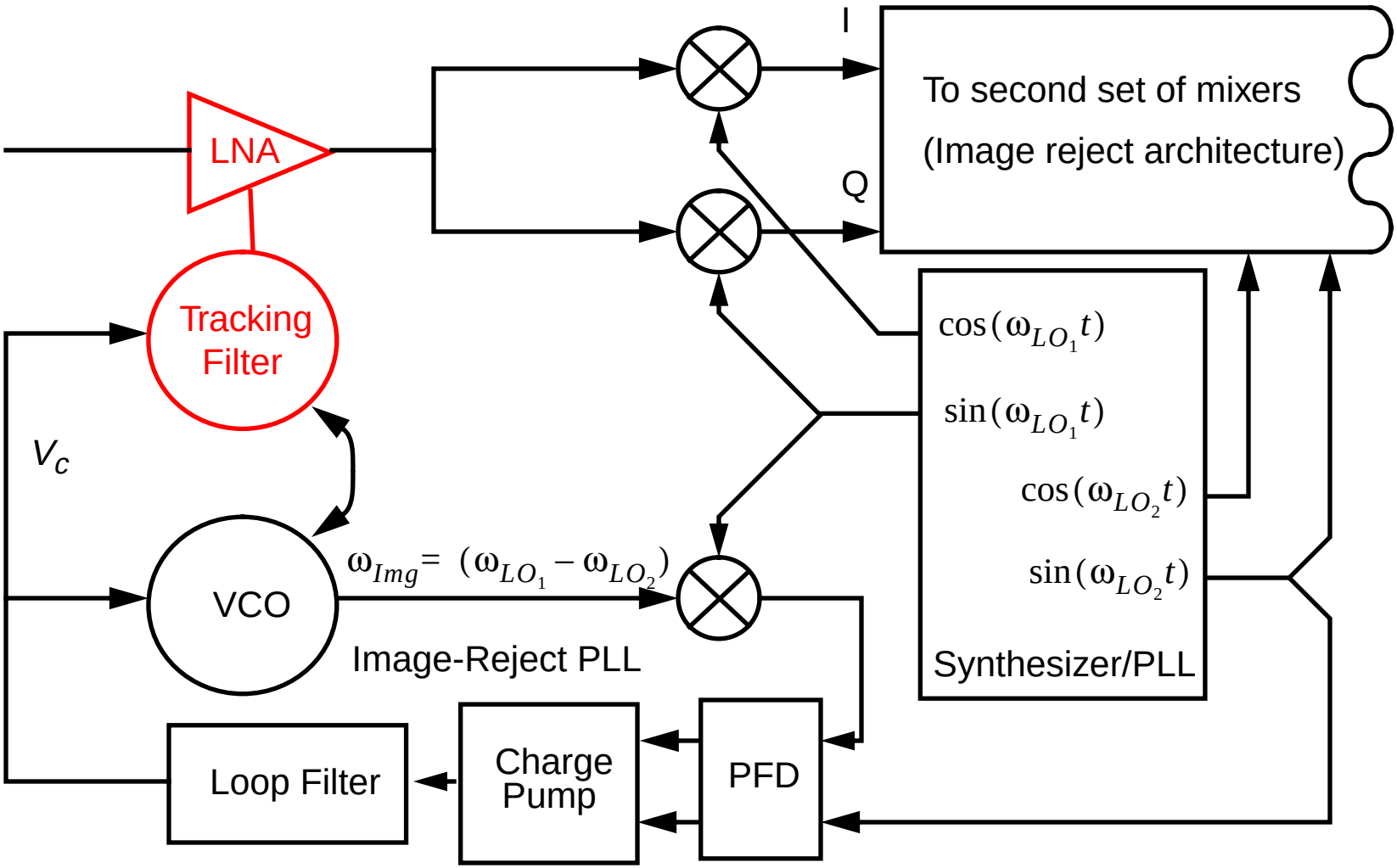


LNA/Filter Transfer Function

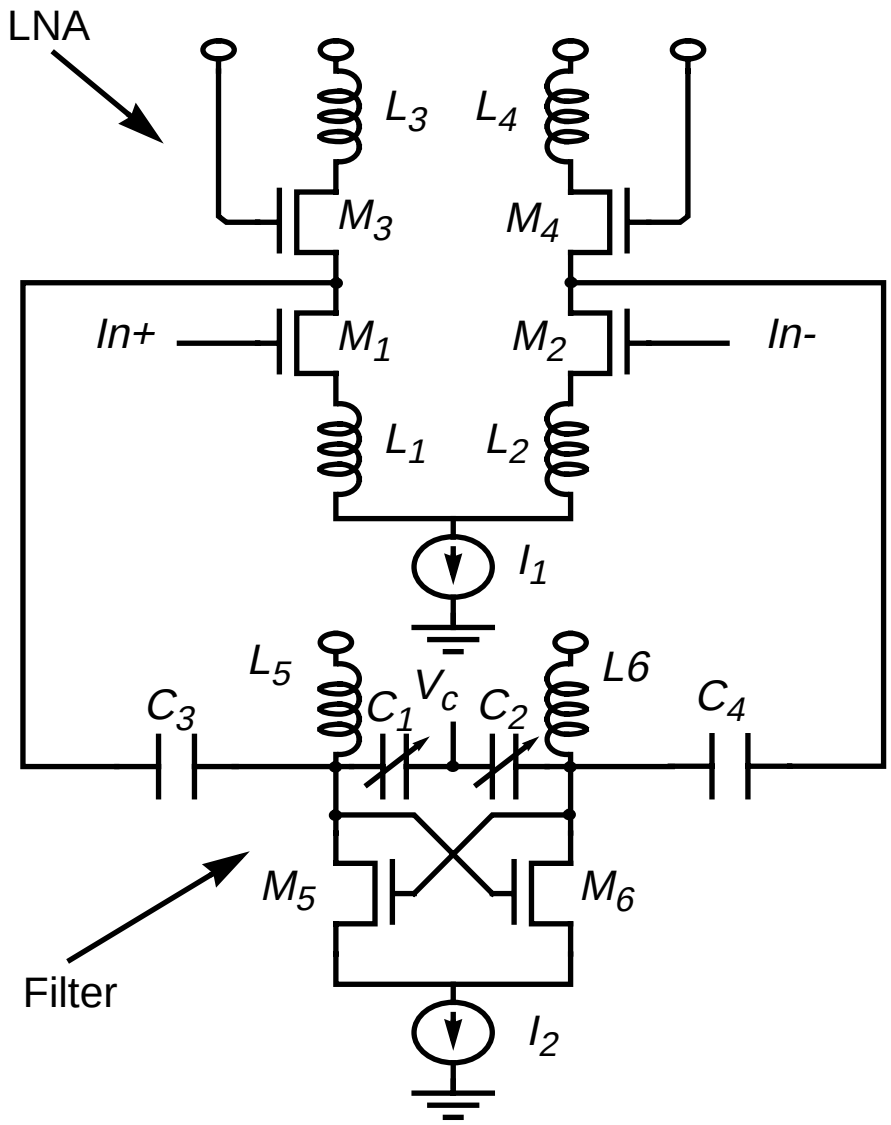




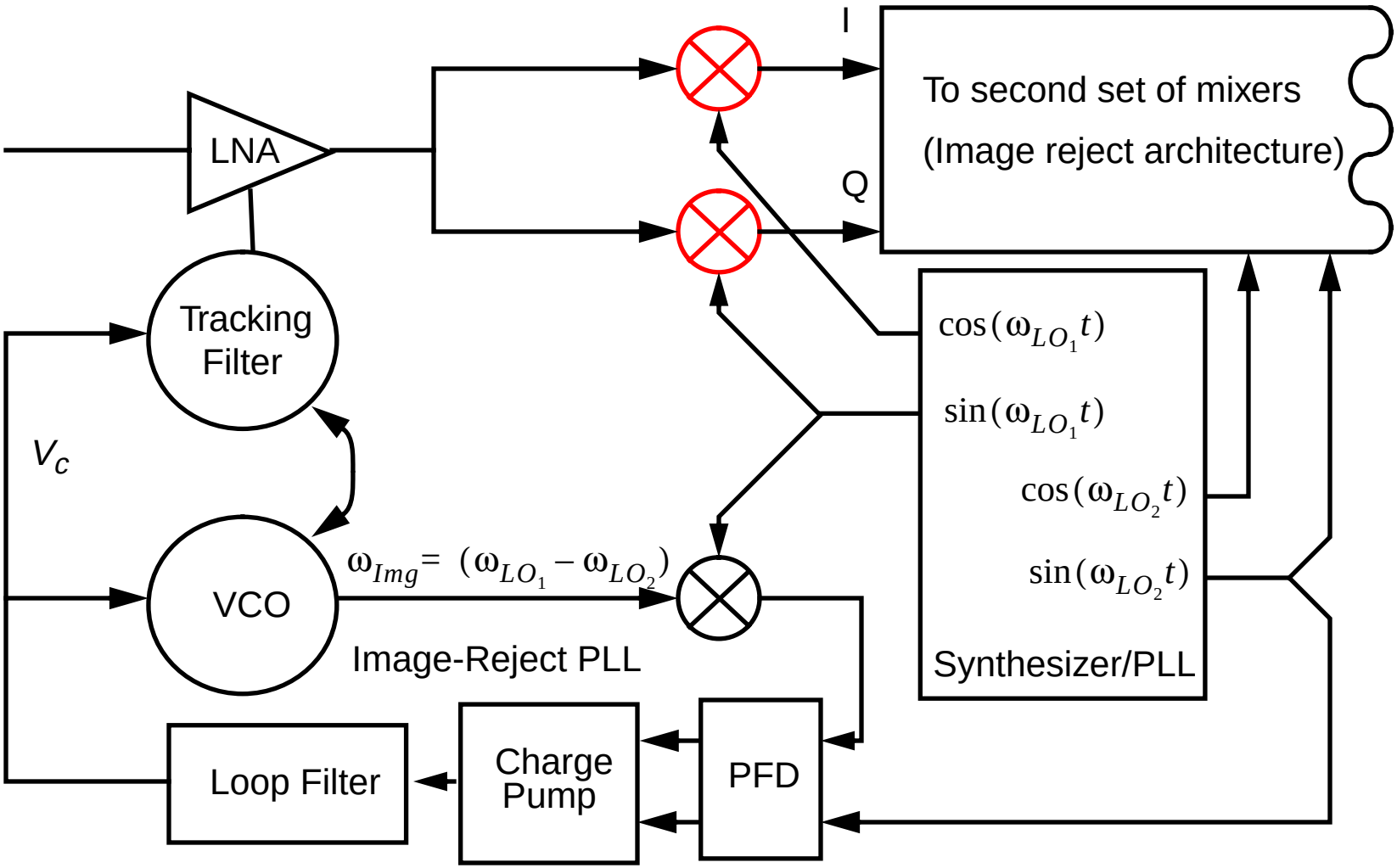
Receiver Architecture



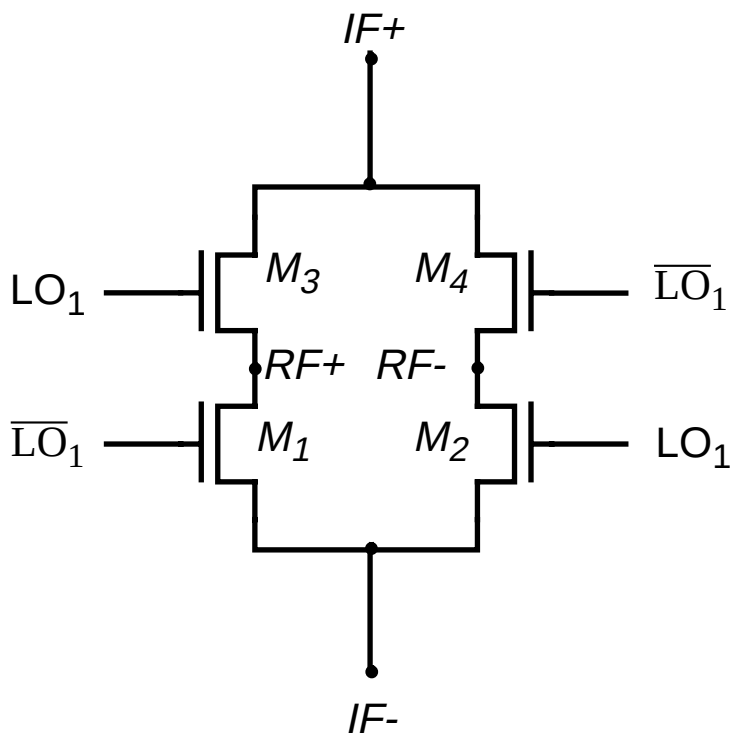
Circuit Implementation: LNA and filter



Receiver Architecture

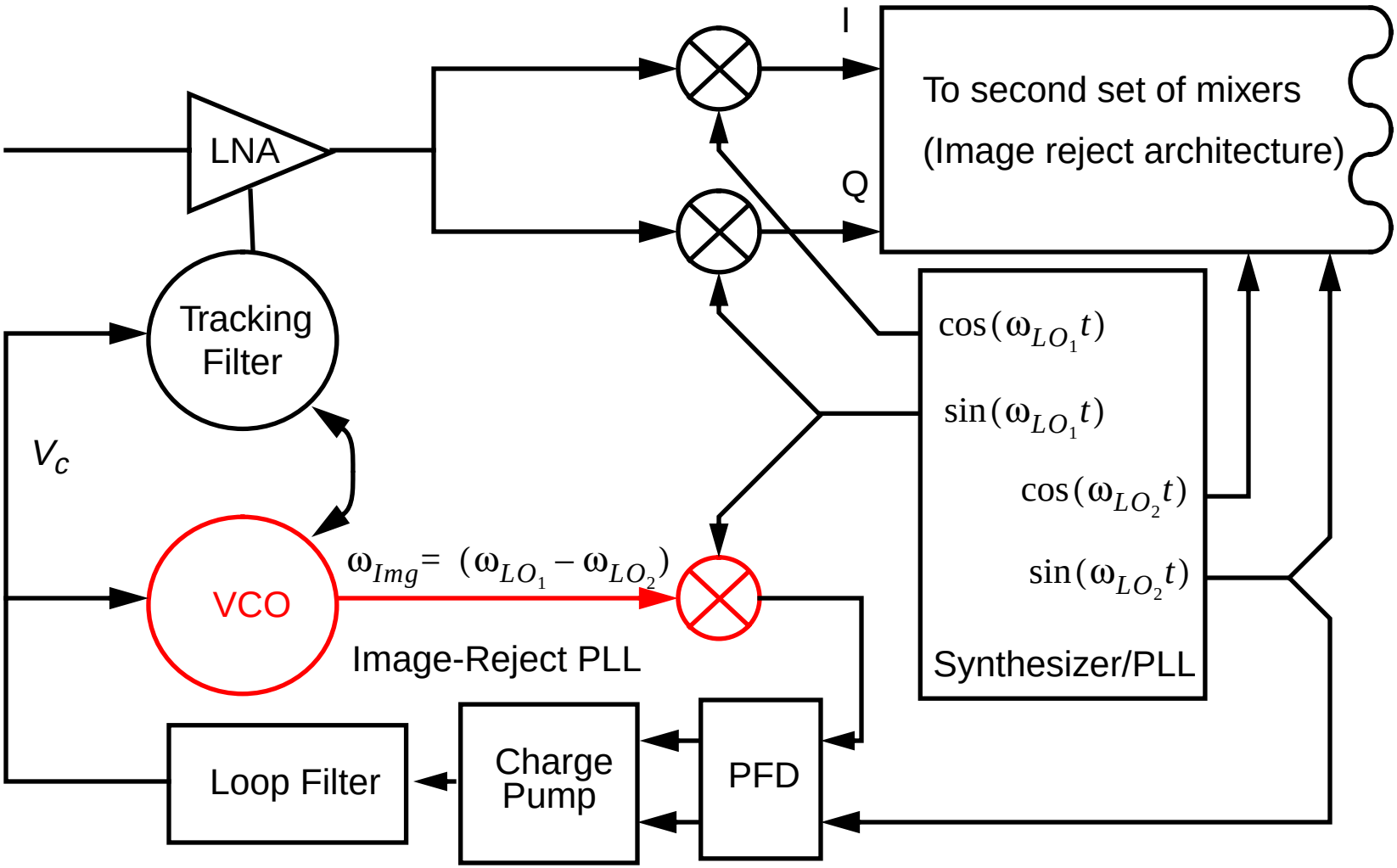


Circuit Implementation: Signal-Path Mixers

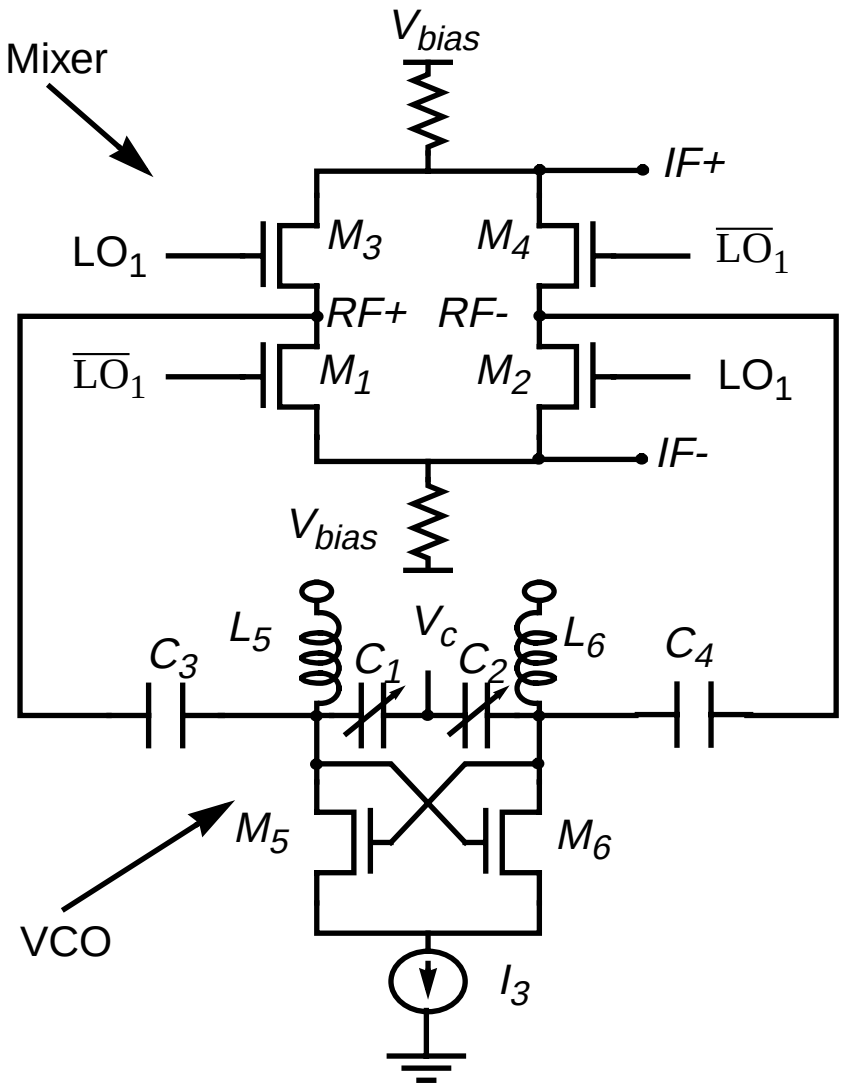


→A. Shahani, et al, “A 12-mW wide dynamic range front-end for a portable GPS receiver,” *IEEE J. Solid-State Circuits*, vol. 32, pp. 2061-2070, Dec. 97.

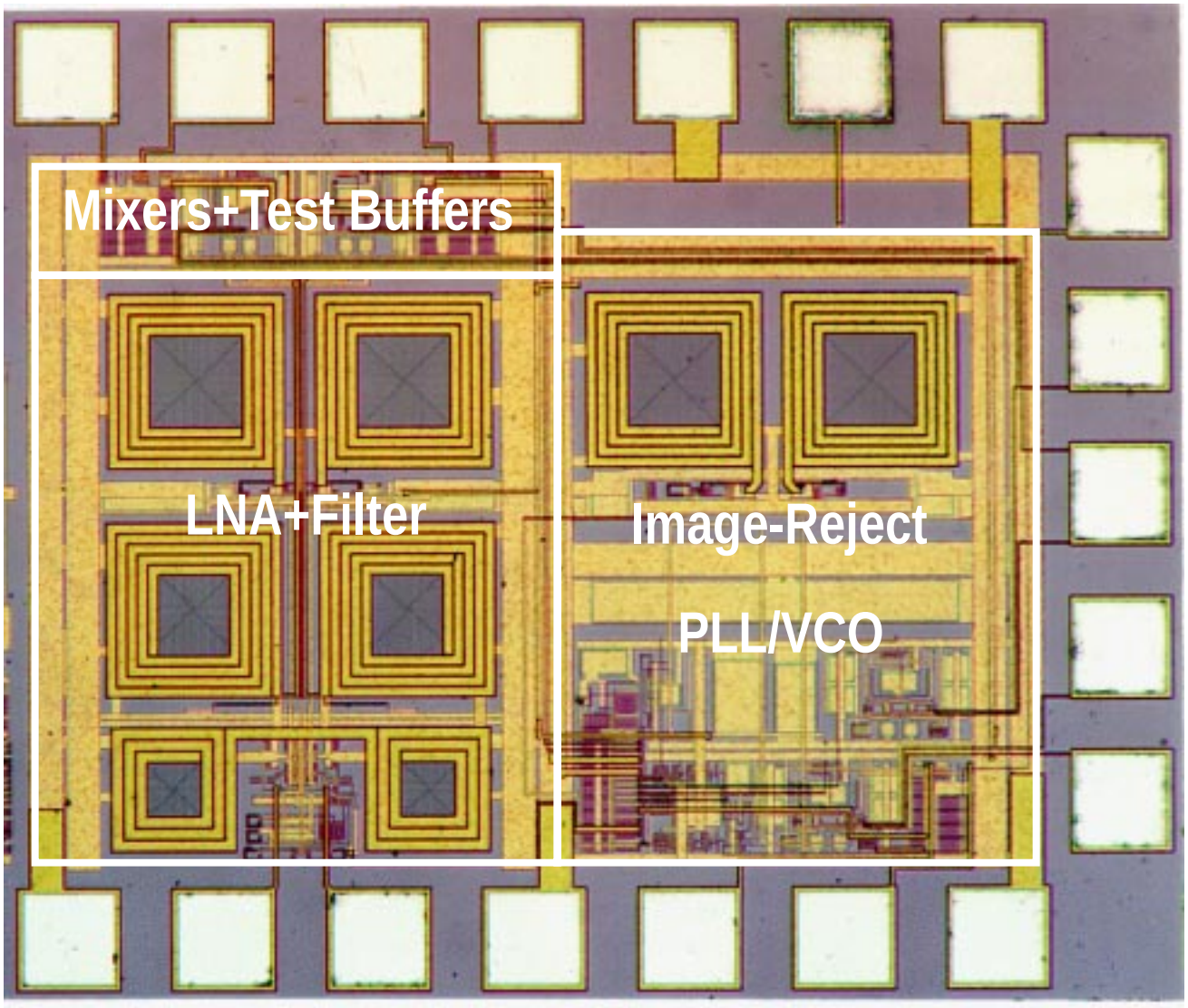
Receiver Architecture



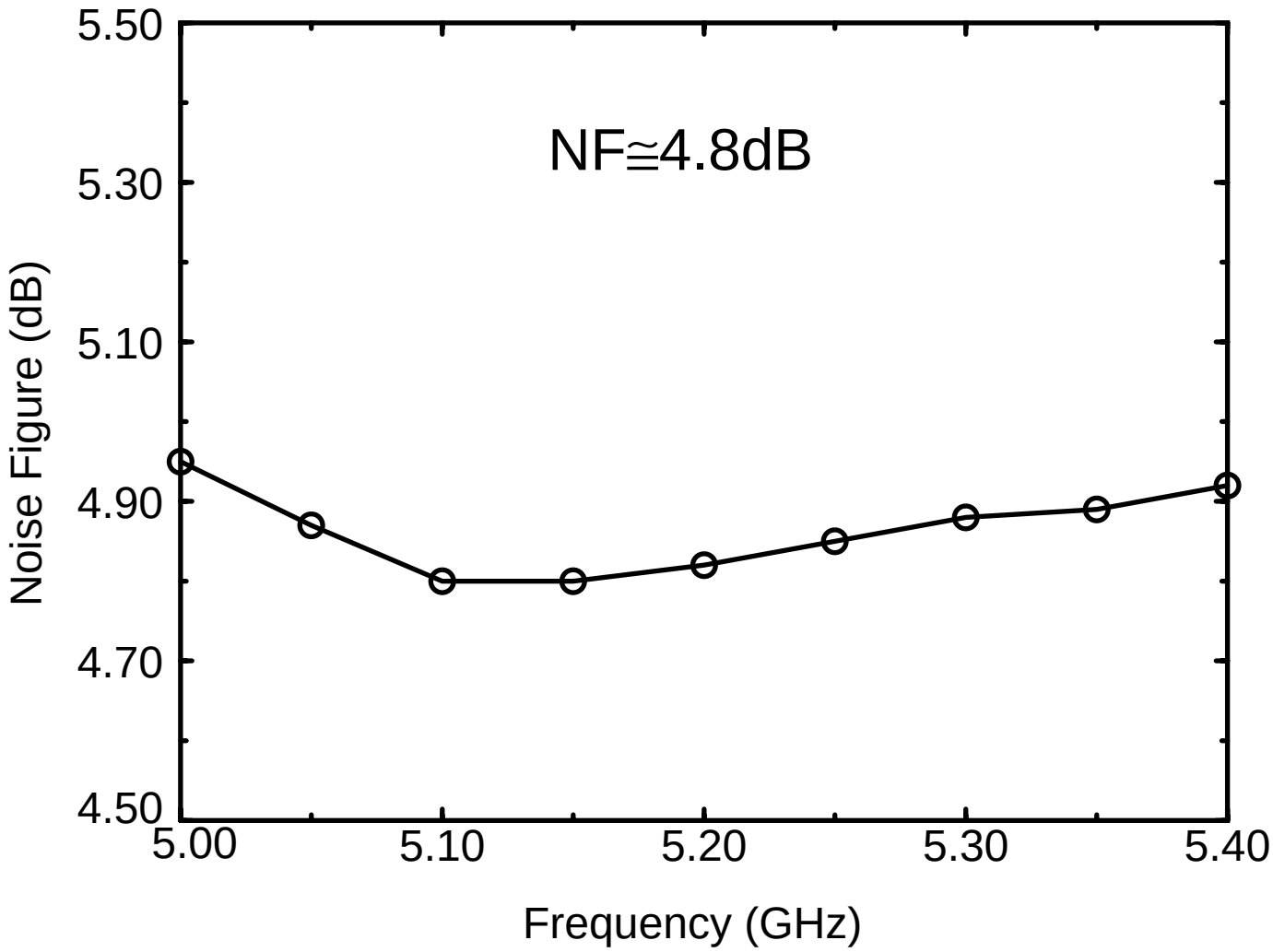
Circuit Implementation: VCO and Mixer



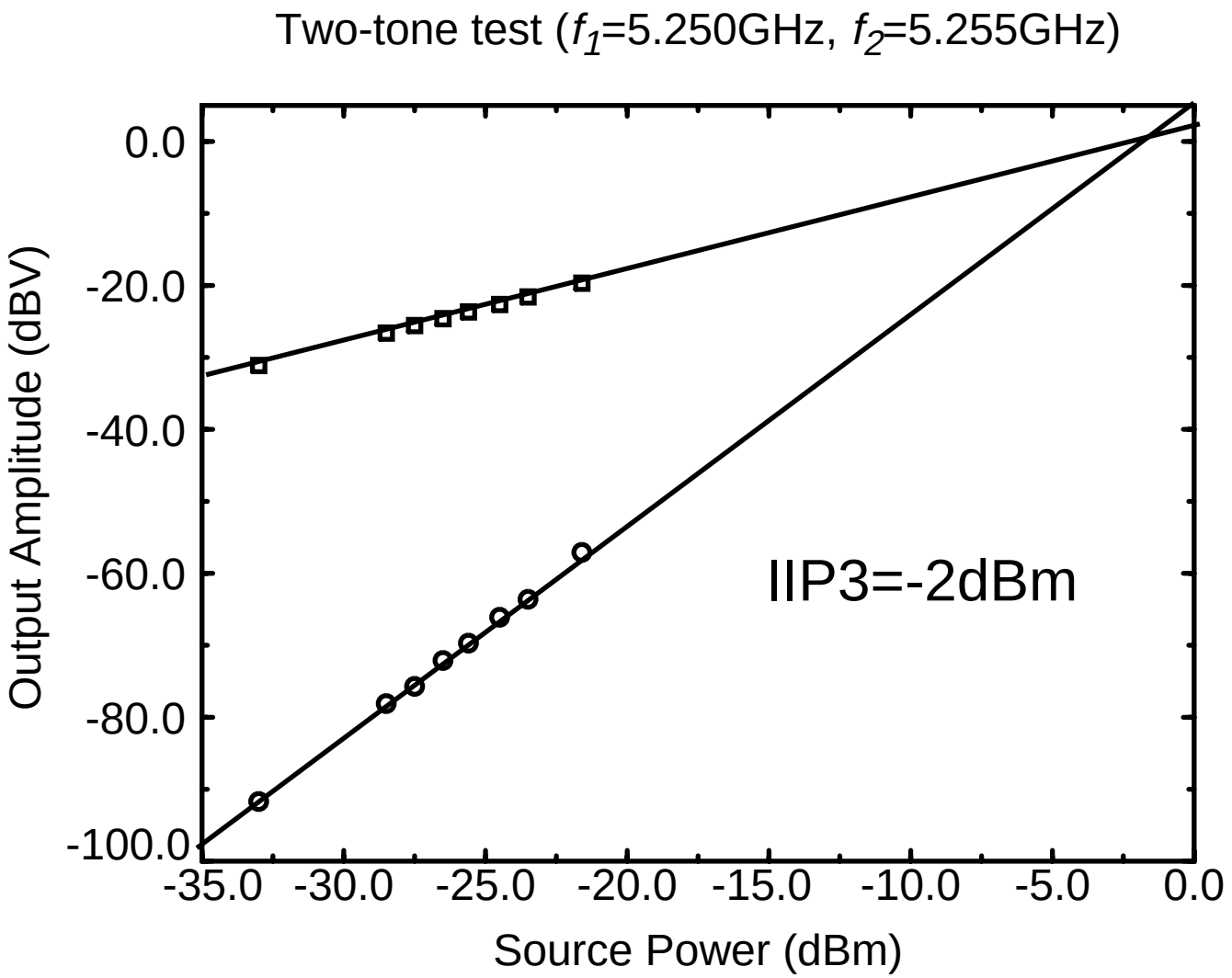
Die Micrograph



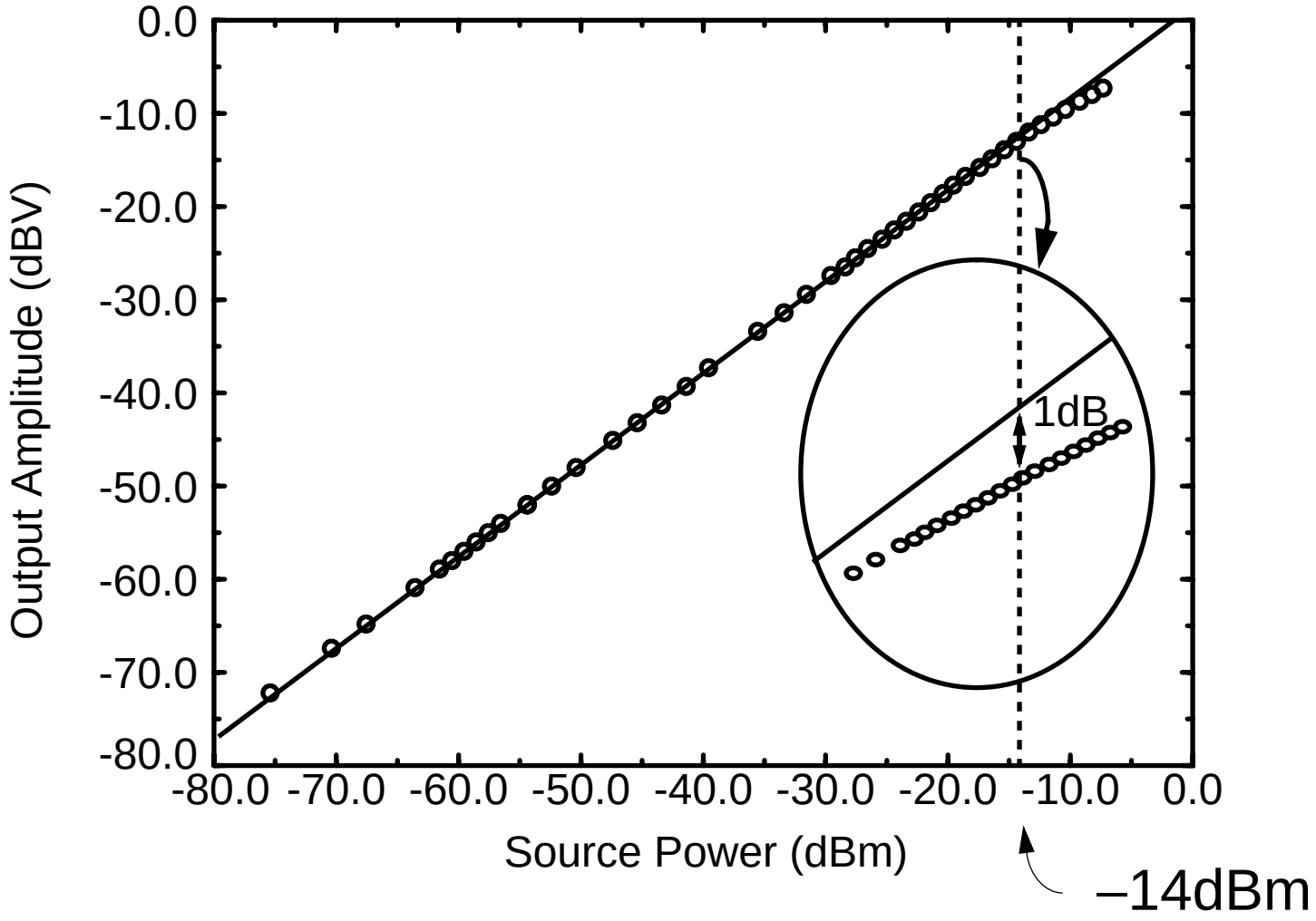
Measured LNA Noise Figure



IP3 Measurement for the RF Front-End



1-dB Compression-Point Measurement



Measured Signal-Path Performance

LNA performance	
Noise figure	4.8dB
Voltage gain	18dB
S_{11}	-12dB
Image-rejection (filter only)	12dB
Receive path (LNA+mixers) performance	
Total noise figure	5.2dB
Total voltage gain	12dB
Input-referred IP3	-2dBm
1-dB compression point	-14dBm
Power dissipation	
LNA	7.2mW
Image-reject filter	1.0mW
Image-reject PLL/VCO	3.2mW
Bias circuitry	1.0mW
Total power @ 2V	12.4mW
Implementation	
Die area	$1mm^2$
Technology	0.24-mm CMOS

Conclusions

- CMOS is suitable for multi-GHz WLAN applications.
- Filtering at RF can be used for
  - →Image rejection.
  - →Improved noise performance.
- Automatic tuning is feasible at RF frequencies.
  - →Image-reject PLL structure consumes little power.
- The proposed front-end architecture is highly linear and tolerates large blockers.

Acknowledgments

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