A 5GHz, 32mW CMOS Frequency Synthesizer with an Injection–Locked Frequency Divider

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OUTLINE

- motivation
- introduction
- synthesizer architecture
- synthesizer building blocks
  - injection–locked frequency divider (ILFD)
  - voltage–controlled oscillator (VCO)
  - prescaler
  - charge pump and loop–filter
- summary
- conclusion

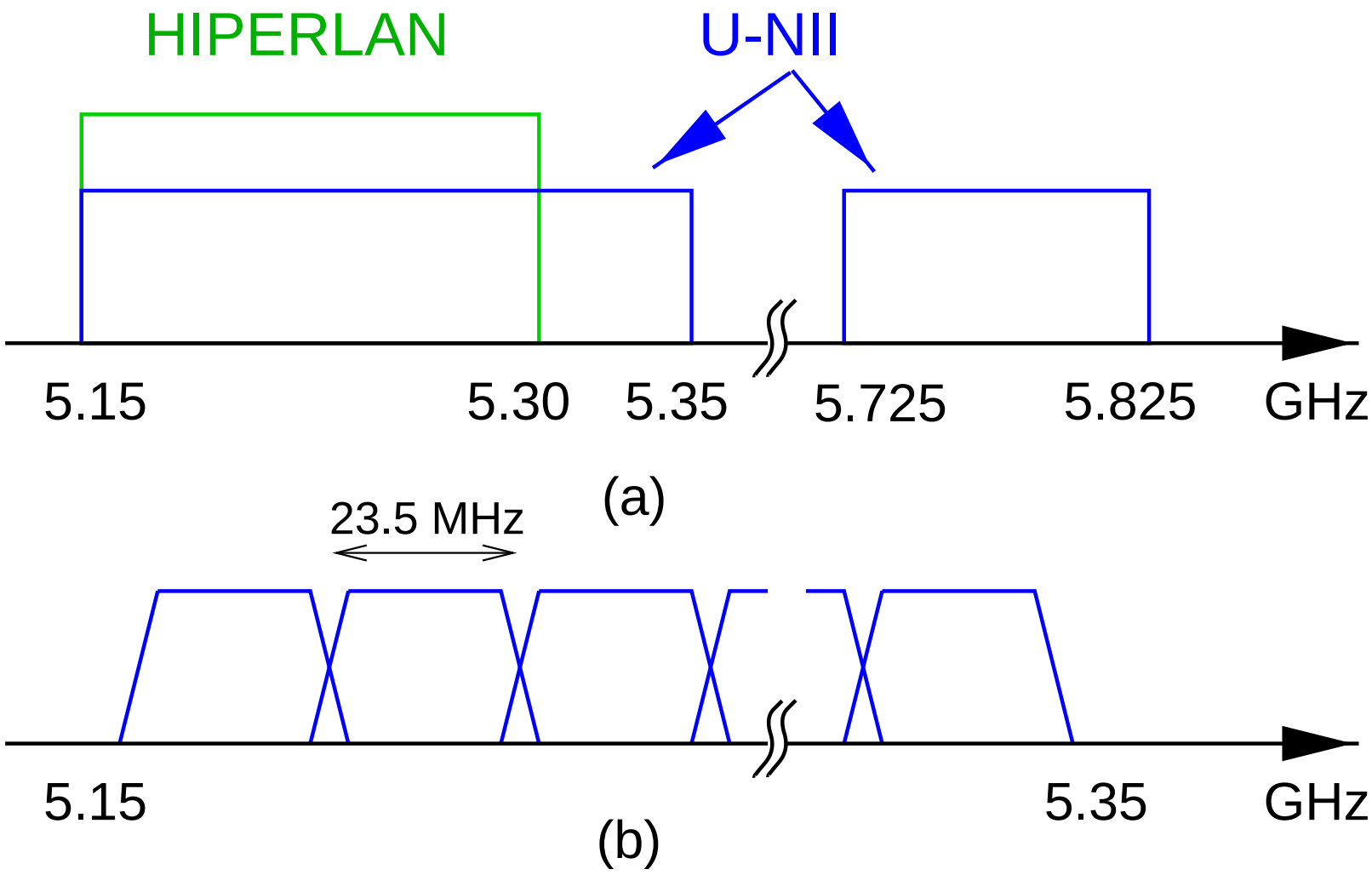
MOTIVATION

- large demand on wideband wireless LAN systems
  - 20+Mb/s data rate
  - low cost
  - low power
- new released frequency band
  - unlicensed national information infrastructure (U–NII) band

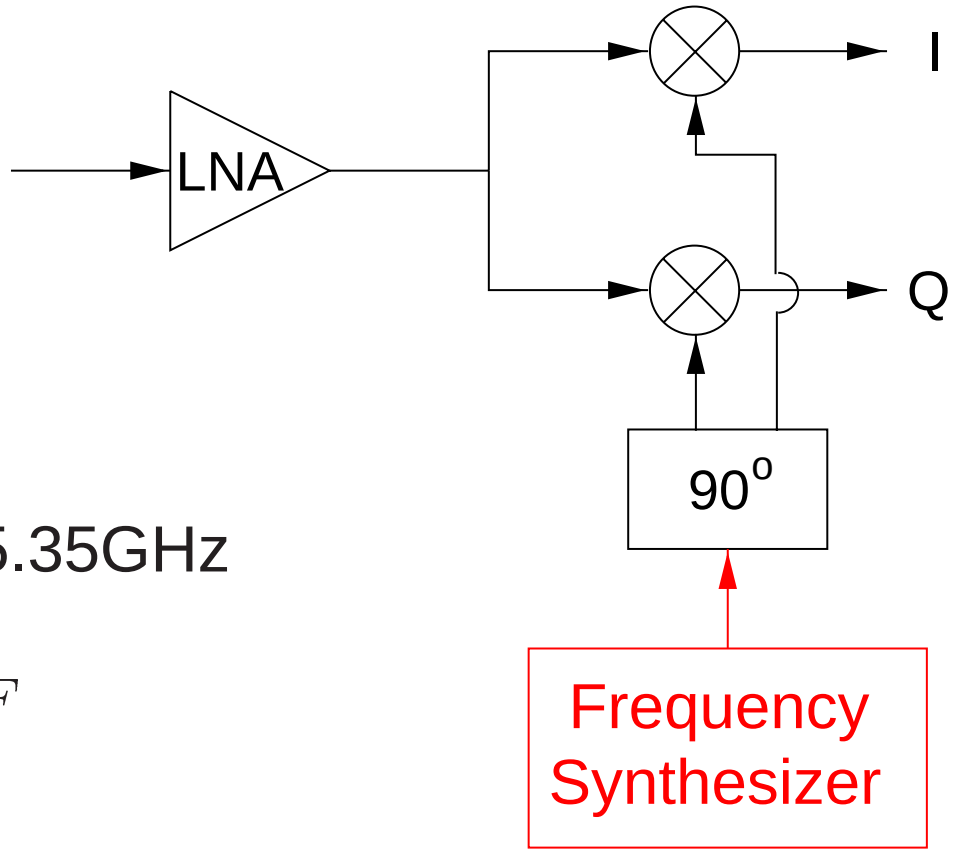
GOAL

- design a 5GHz frequency synthesizer for a U–NII band wireless–LAN receiver (HIPERLAN compatible)
- implement in CMOS
- minimize power consumption

FREQUENCY OF OPERATION



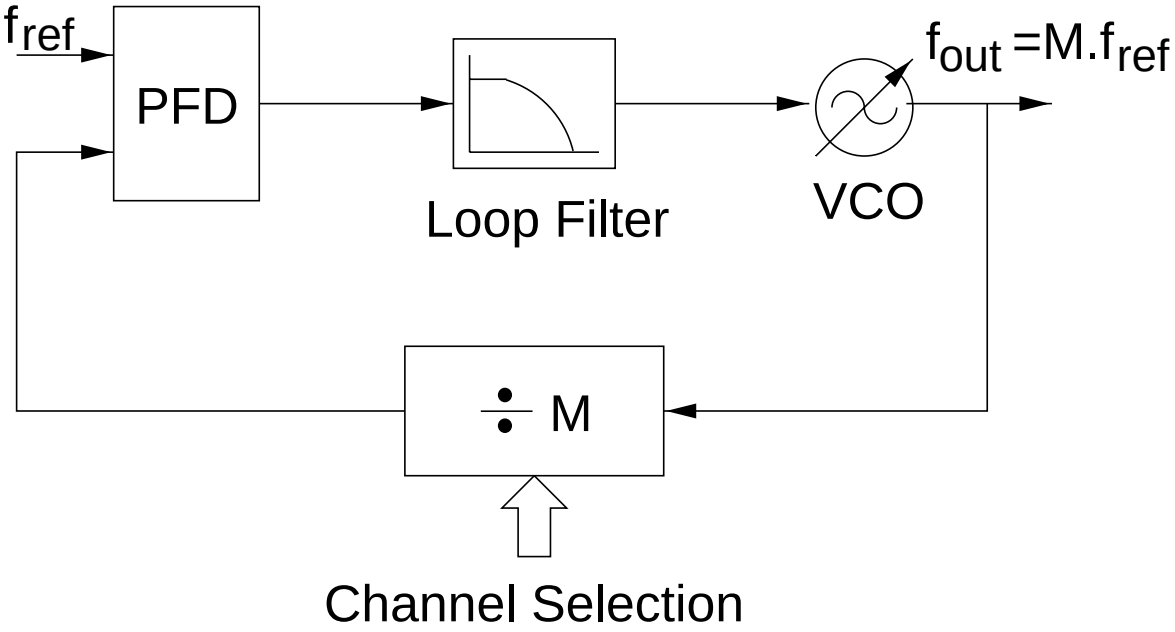
RECEIVER ARCHITECTURE



- f_{RF} =5.15–5.35GHz
- $f_{LO} = \frac{16}{17} f_{RF}$

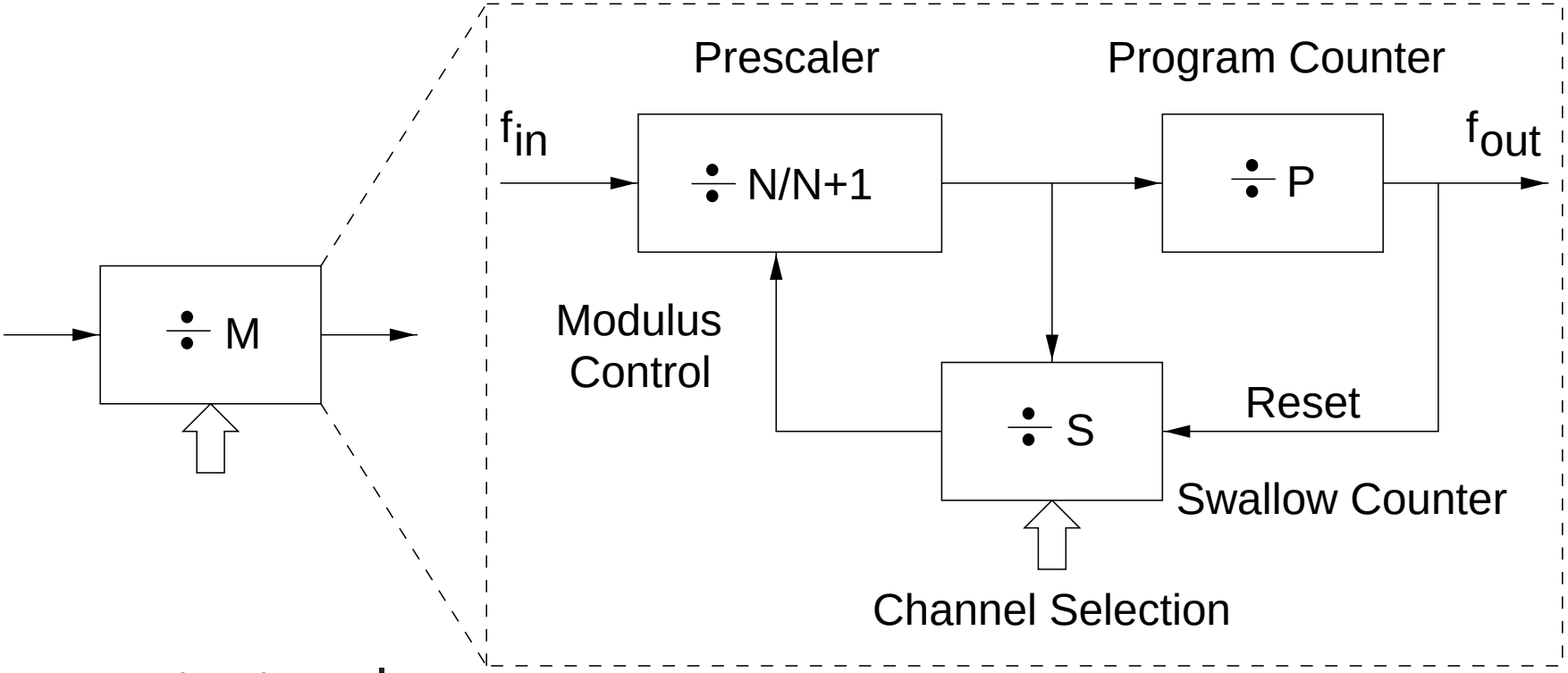
∗ H. Samavati et al., “A 12.4mW CMOS Front–End for a 5GHz Wireless–LAN Receiver”, 1999 Symposium of VLSI Circuits, Session 9.2.

INTEGER–N FREQUENCY SYNTHESIZER



- $f_{out} = \mathrm{M} \times f_{ref}$
- $\mathrm{M} = \mathrm{M_o} + \mathrm{S}$
  $\mathrm{S} = 0, 1, 2, ..., 7$

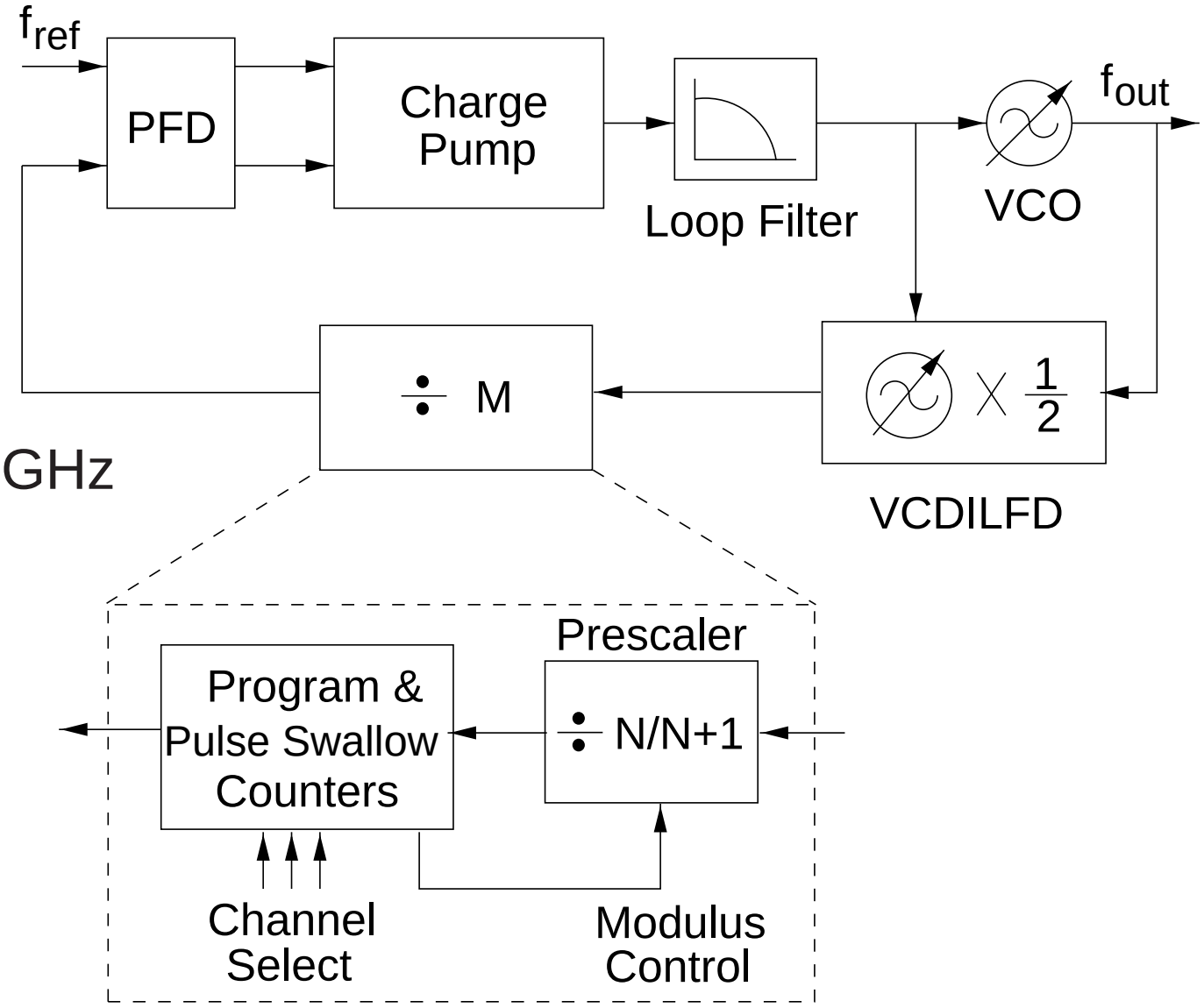
PULSE SWALLOW FREQUENCY DIVIDER



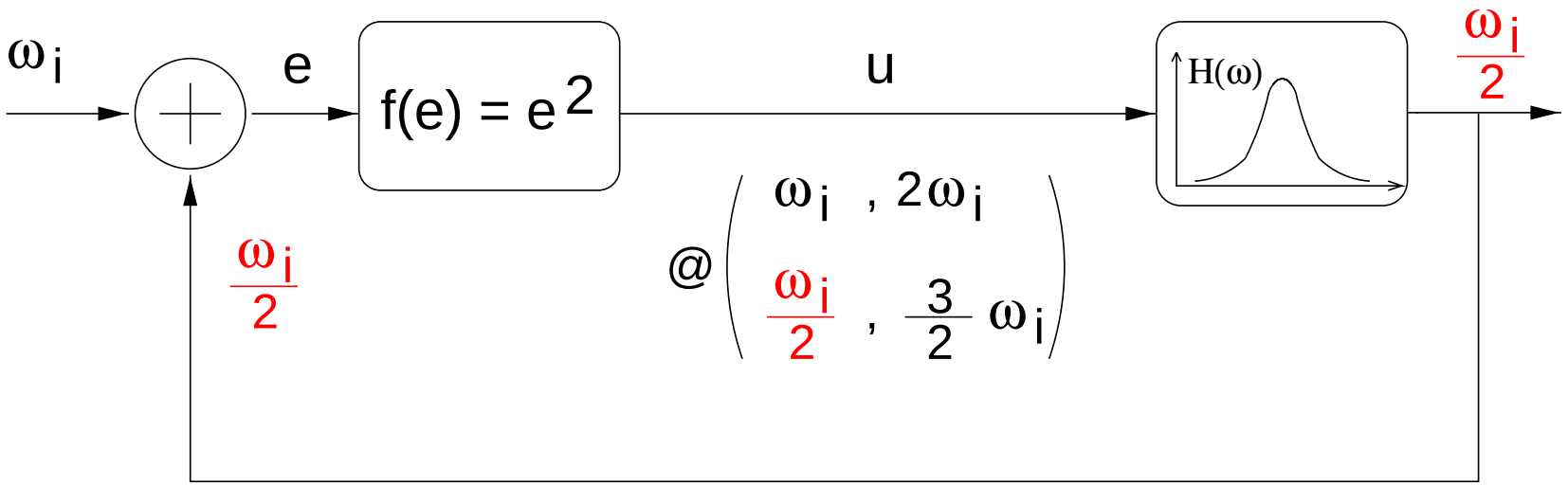
- one output cycle = $(\mathrm{N}+1)\mathrm{S}+(\mathrm{P}-\mathrm{S})\mathrm{N}=\mathrm{PN}+\mathrm{S}$ input cycles.
- $\mathrm{f_{in}}=(\mathrm{PN}+\mathrm{S})\times\mathrm{f_{out}}$
- $\mathrm{M}=\mathrm{PN}+\mathrm{S}=\mathrm{M_o}+\mathrm{S}$

PROPOSED ARCHITECTURE

- f_{ref}=11MHz
- f_o=4.840–4.994GHz
- 8 channels
- M=220–227
- N=22



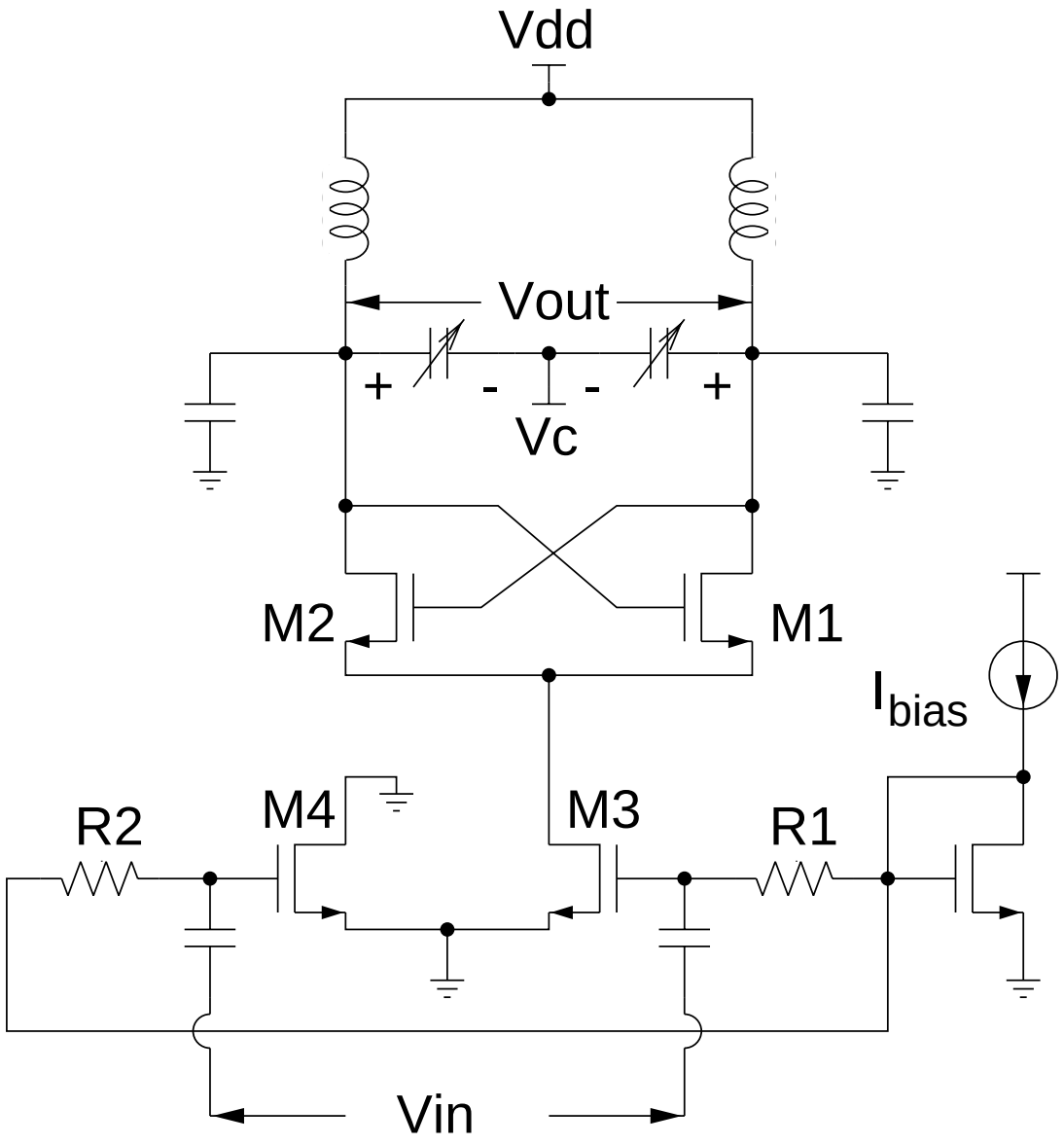
ILFD SIMPLIFIED PICTURE



- oscillator feedback model with perturbation
- oscillation conditions should be satisfied in the presence of the incident signal

VOLTAGE–CONTROLLED DIFFERENTIAL ILFD

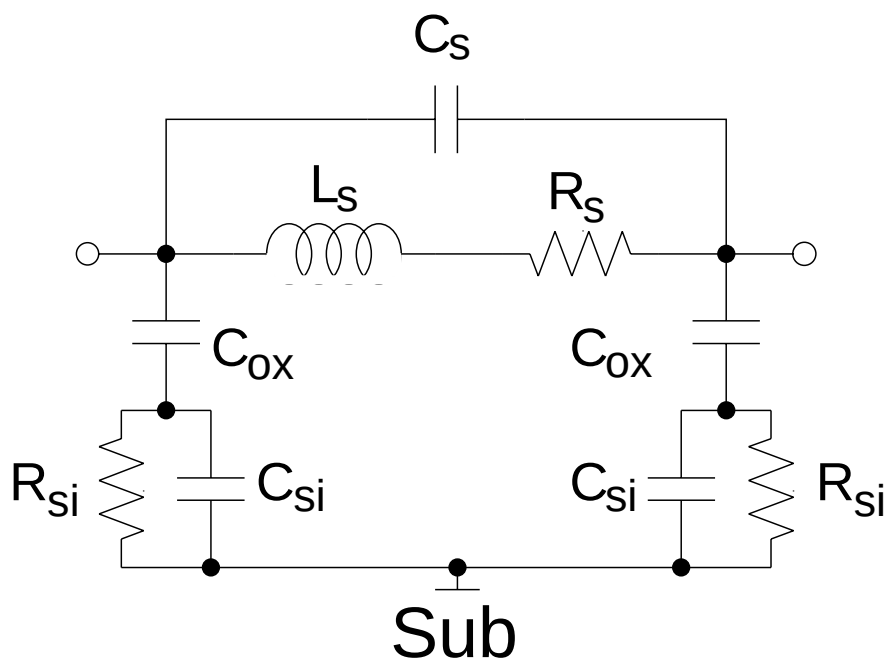
- 0.24μm CMOS
- Vdd=1.5V
- $\mathrm{I_{bias}}$=300μA
- f_o=2.25GHz
- f_i=4.5GHz

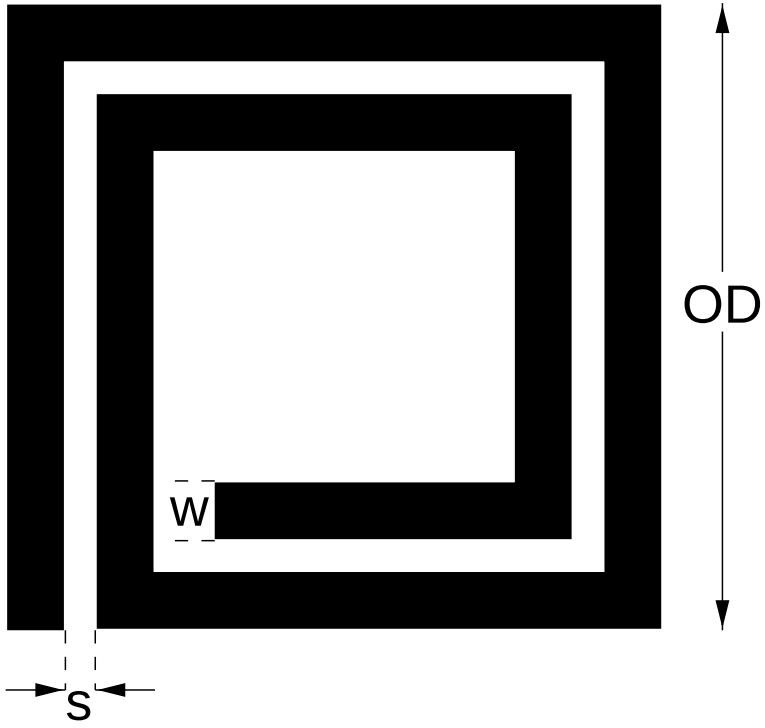


INDUCTOR DESIGN (ILFD)

- maximum locking range $\Rightarrow$ maximize L
- minimum power consumption $\Rightarrow$ maximize LQ

INDUCTOR DESIGN





- design parameters:
  - w: metal width
  - s: metal spacing
  - OD: outer dimension
  - n: number of turns

INDUCTOR DESIGN (ILFD)

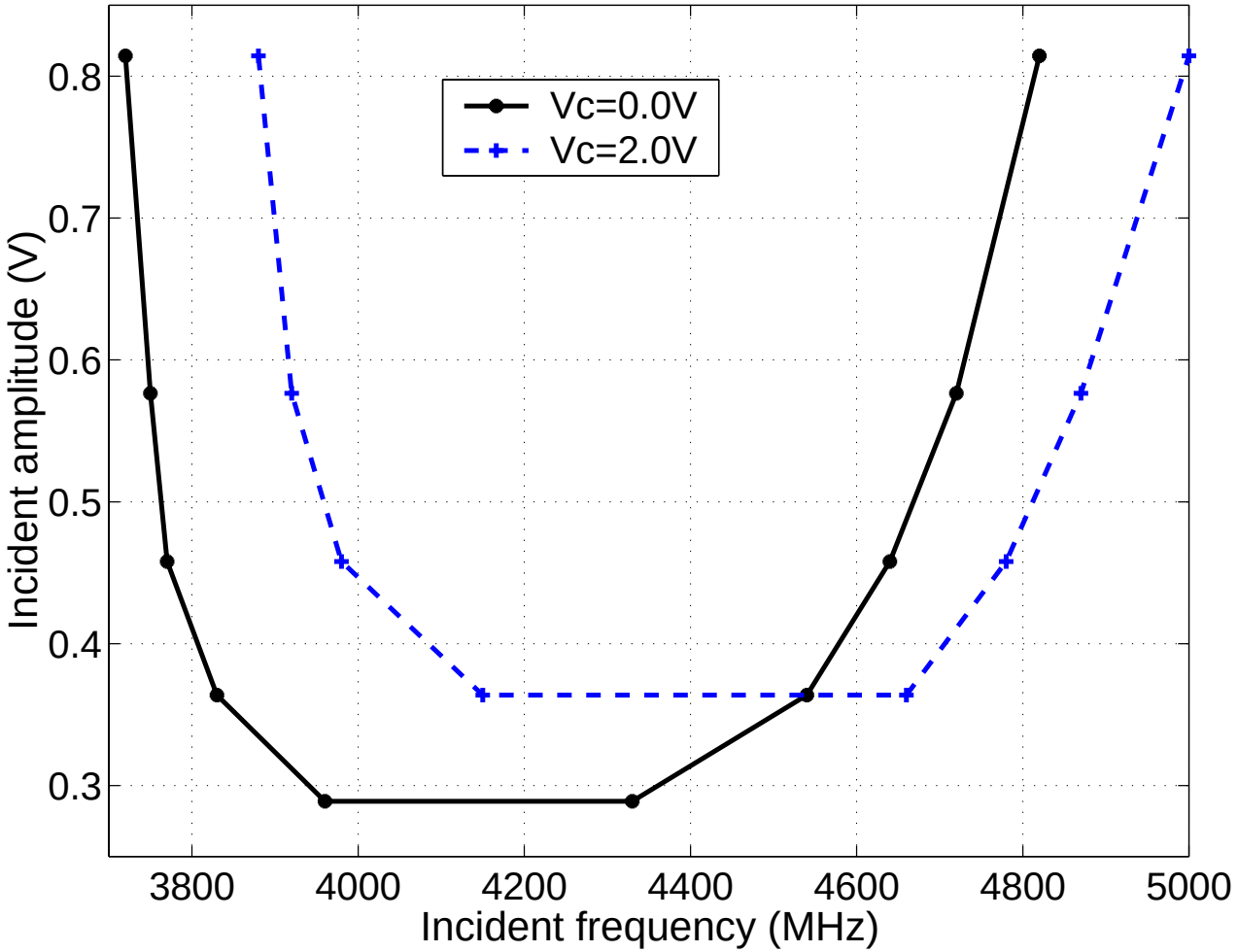
- in planar spiral inductors maximizing L does not maximize LQ

$$\Downarrow$$

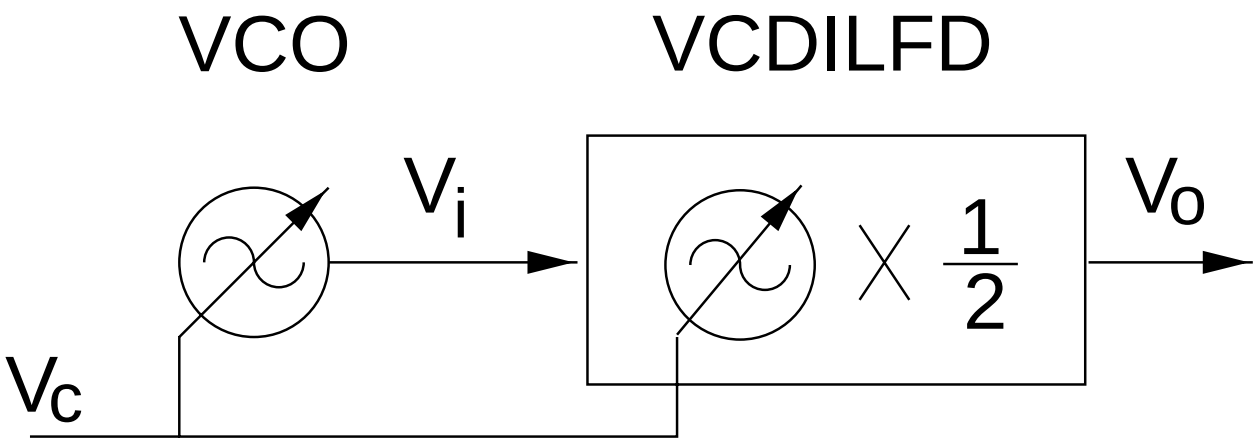
maximize L for a given LQ

VCDILFD FREQUENCY RANGE

- 0.24μm CMOS
- Vdd=1.5V
- I_{bias}=300μA



TRACKING ILFD



- locking range extension

ILFD SUMMARY

maximum frequency of operation	5GHz
output frequency tuning	110MHz $\approx$ 5%
input–referred locking range	450MHz $\approx$ 10% @ 0.7mW
	900MHz $\approx$ 20% @ 1.0mW
technology	0.24μm CMOS
die area	0.186mm^2

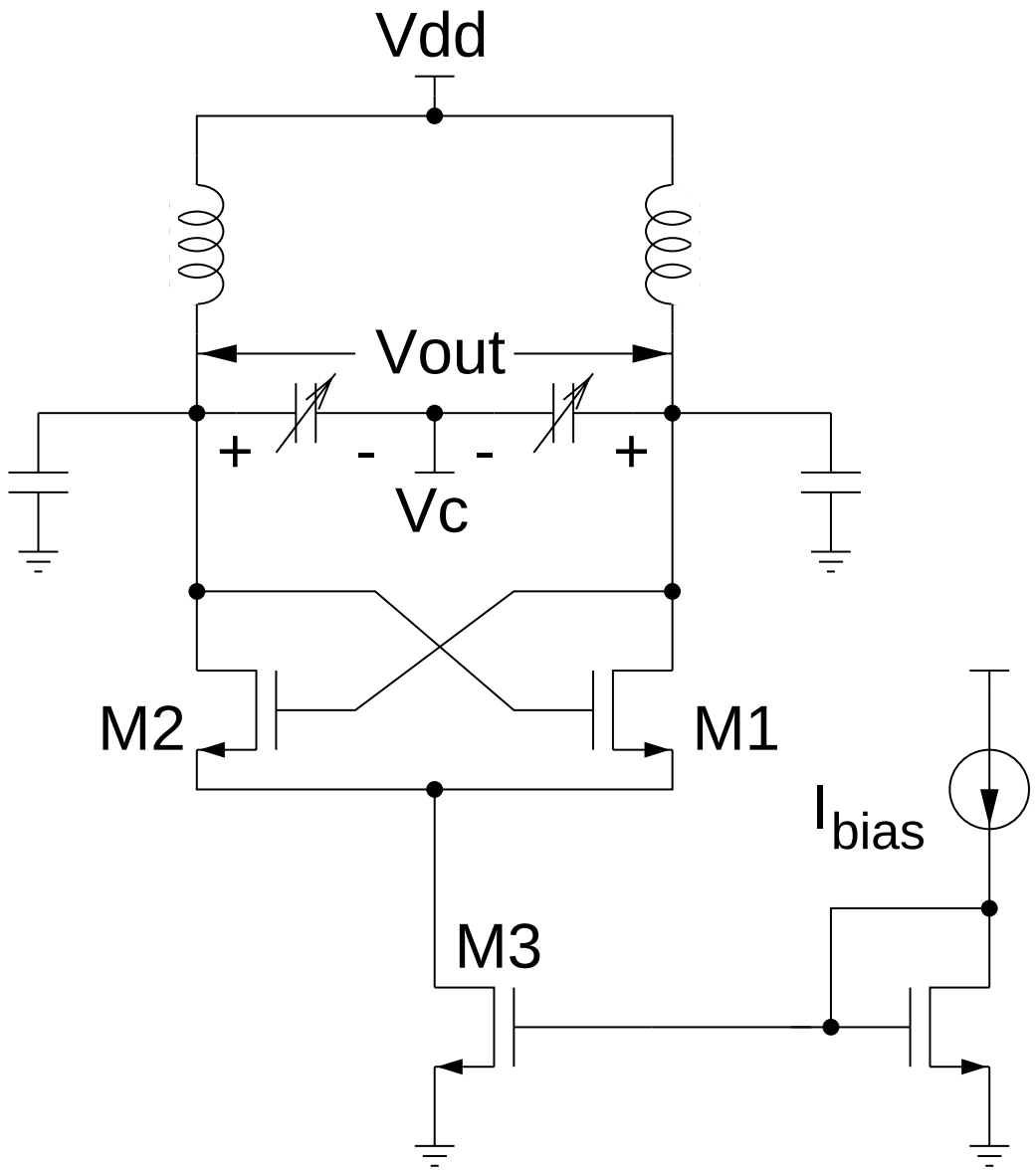
flip–flop–based divider

0.24μm CMOS (simulation)	7mW @ 5GHz
0.1μm CMOS	2.6mW @ 5GHz

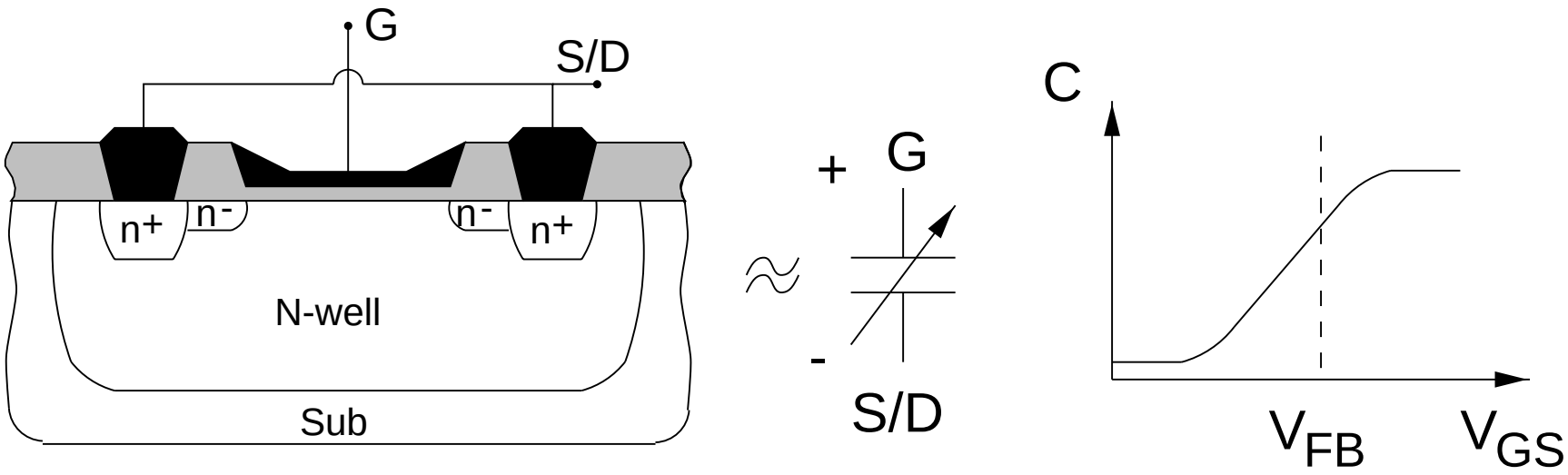
(Razavi *et al.*, JSSC Vol. 30, No.2, pp 101–109, Feb. 1995)

VOLTAGE–CONTROLLED OSCILLATOR

- 0.24μm CMOS
- Vdd=1.5V
- $\mathrm{I_{bias}}$=2.0mA
- f_o=4.85GHz



VARACTOR



- accumulation mode MOS capacitor
  - large quality factor ($>$ 60 @ 5GHz)
  - flat–band voltage $\approx$ zero

∗ A. S. Porret et al., CICC Digest, pp 641-644, 1999.

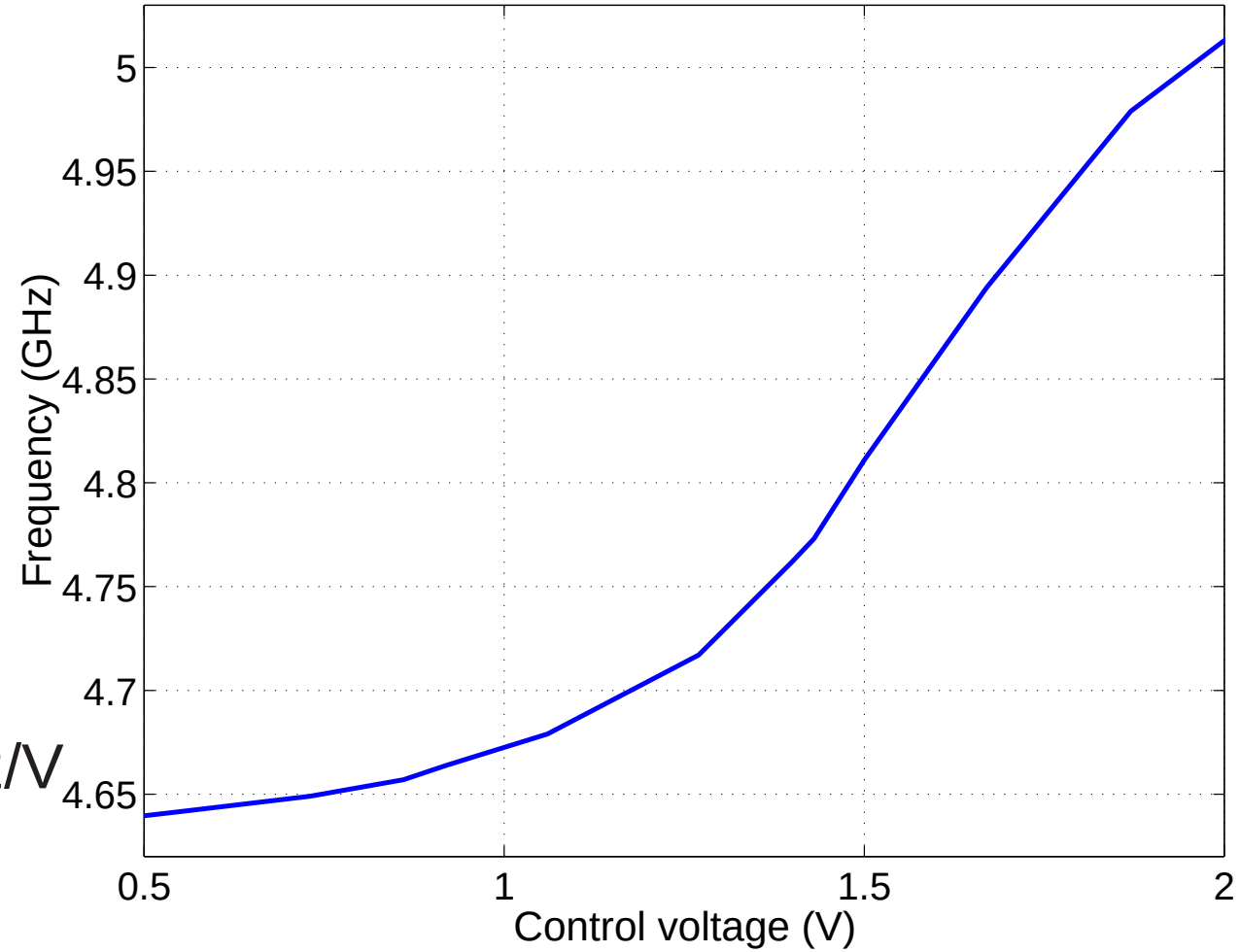
∗ T. Soorapanth et al., Symposium on VLSI Circuits Digest, pp 32–33, 1998.

INDUCTOR DESIGN (VCO)

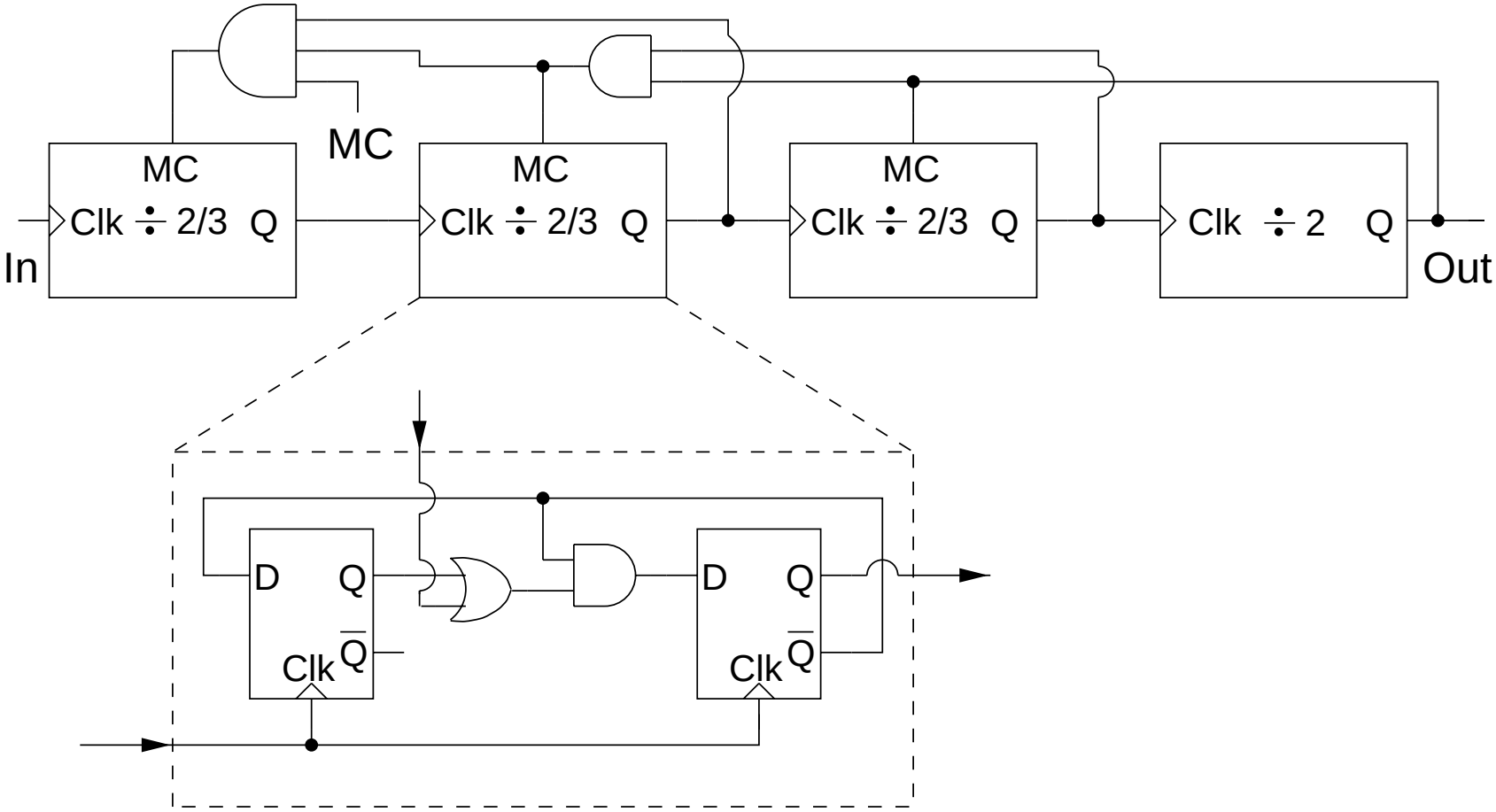
- maximum $Q \Rightarrow$ minimum inductor noise
- if inductors are not the main source of noise, maximum $LQ \Rightarrow$
  - maximum oscillation amplitude for a given bias current
  - minimum phase noise

VCO FREQUENCY TUNING

- 0.24μm CMOS
- Vdd $=$ 1.5V
- $\mathrm{I_{bias}} =$ 2.0mA
- $\Delta f =$ 370MHz
  $\approx$ 7.7%
- $\Delta V_c =$1.5V
- $(\frac{df}{dv})_{\max} =$500MHz/V

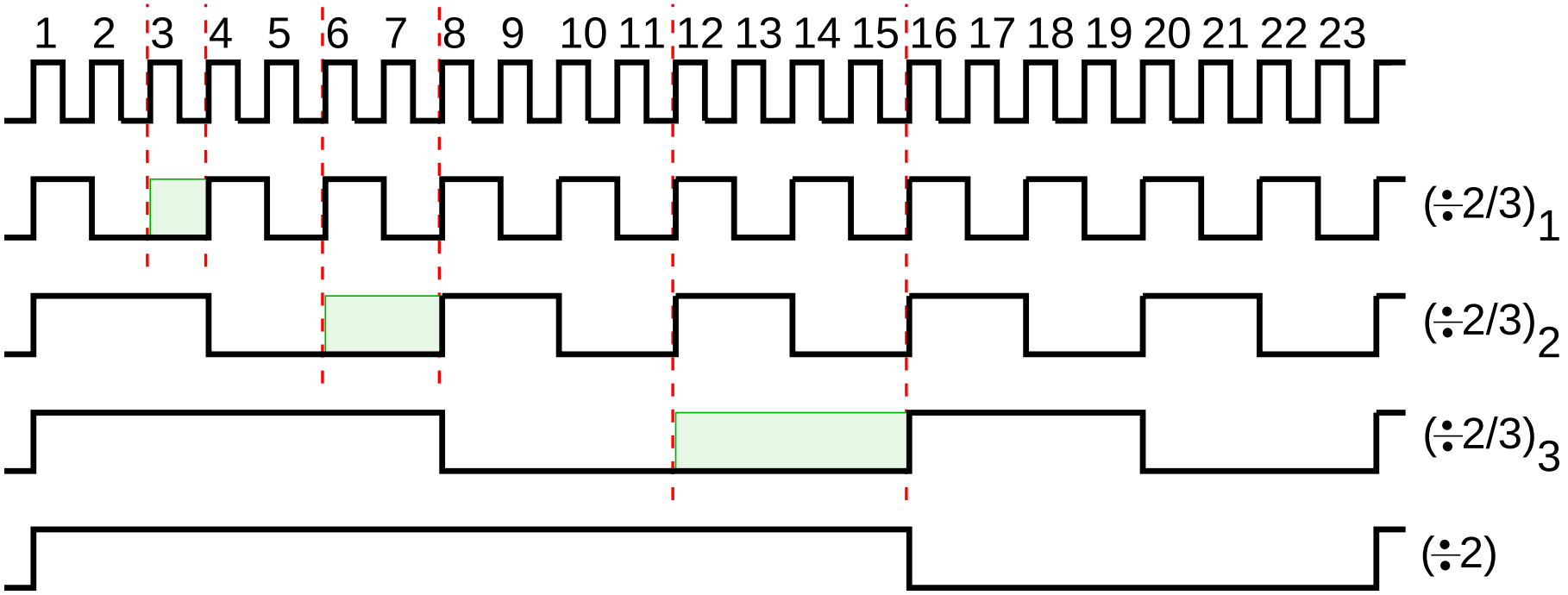


PRESCALER



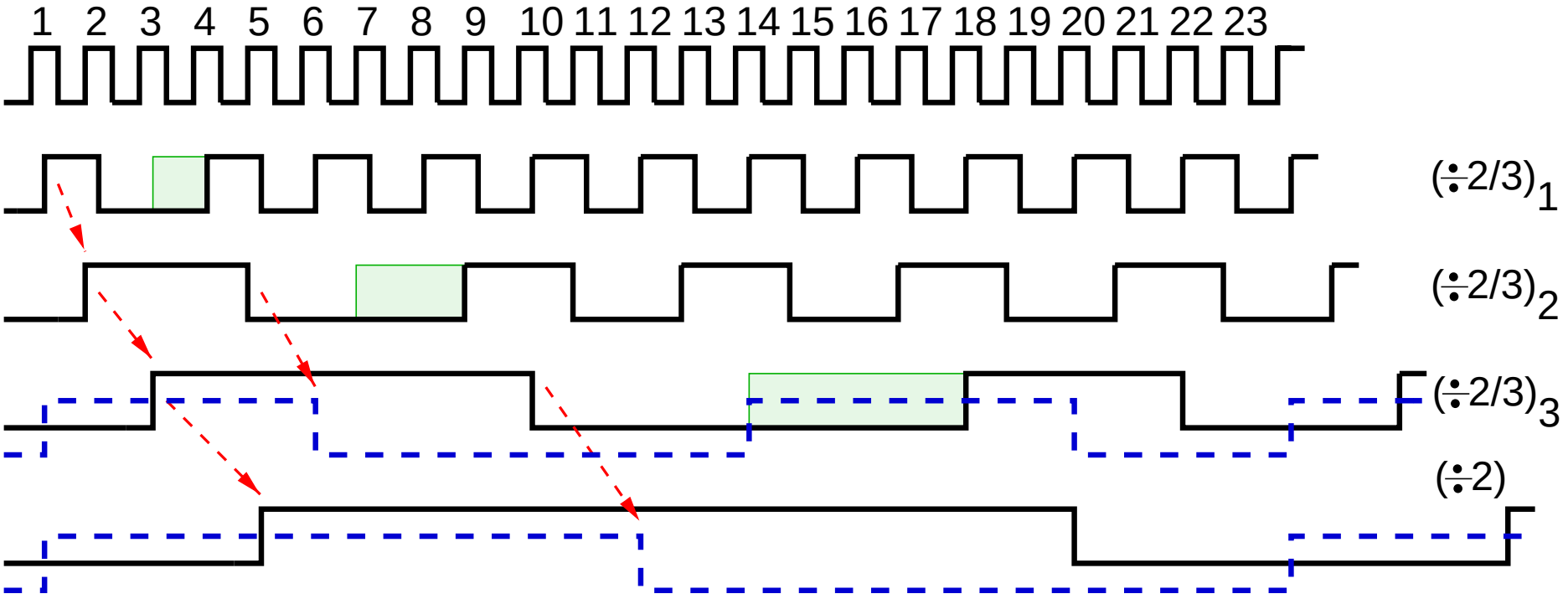
- divide by 22/23
- $N = 2^4 + \mathrm{S}_1.2^0 + \mathrm{S}_2.2^1 + \mathrm{S}_3.2^2$

PRESCALER (ZERO GATE DELAY)



- $N = 2^4 + \mathrm{S}_1.2^0 + \mathrm{S}_2.2^1 + \mathrm{S}_3.2^2$
- $\mathrm{T}_{\mathrm{clk}} =$ 400ps
- $\mathrm{D}_{\mathrm{FO4}} =$ 160ps (Slow process + high temperature)

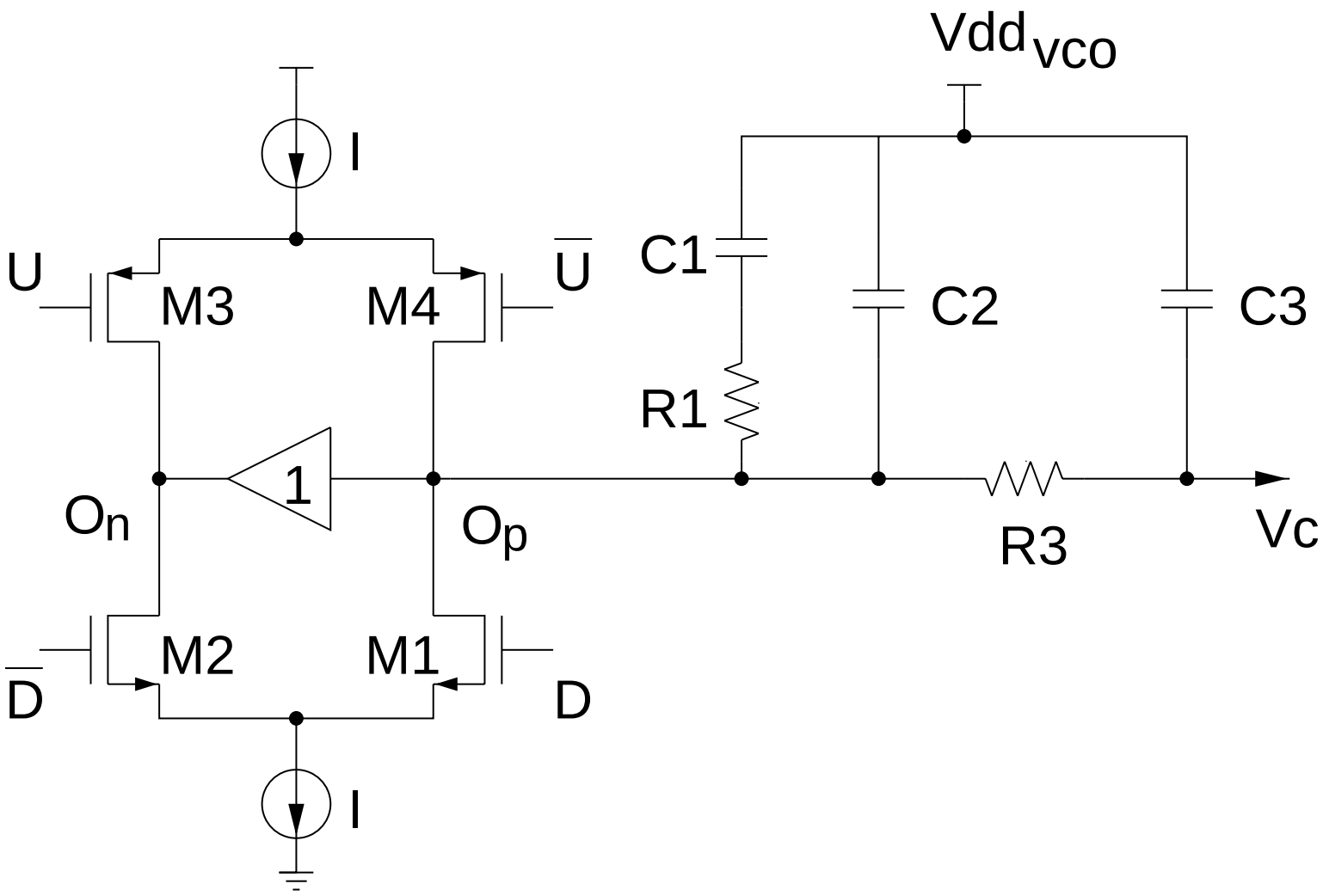
PRESCALER (NON ZERO GATE DELAY)



- problem: gate delays add
- solution:
  - make gates faster $\Rightarrow$ burn more power
  - use quadrature outputs to generate swallow commands

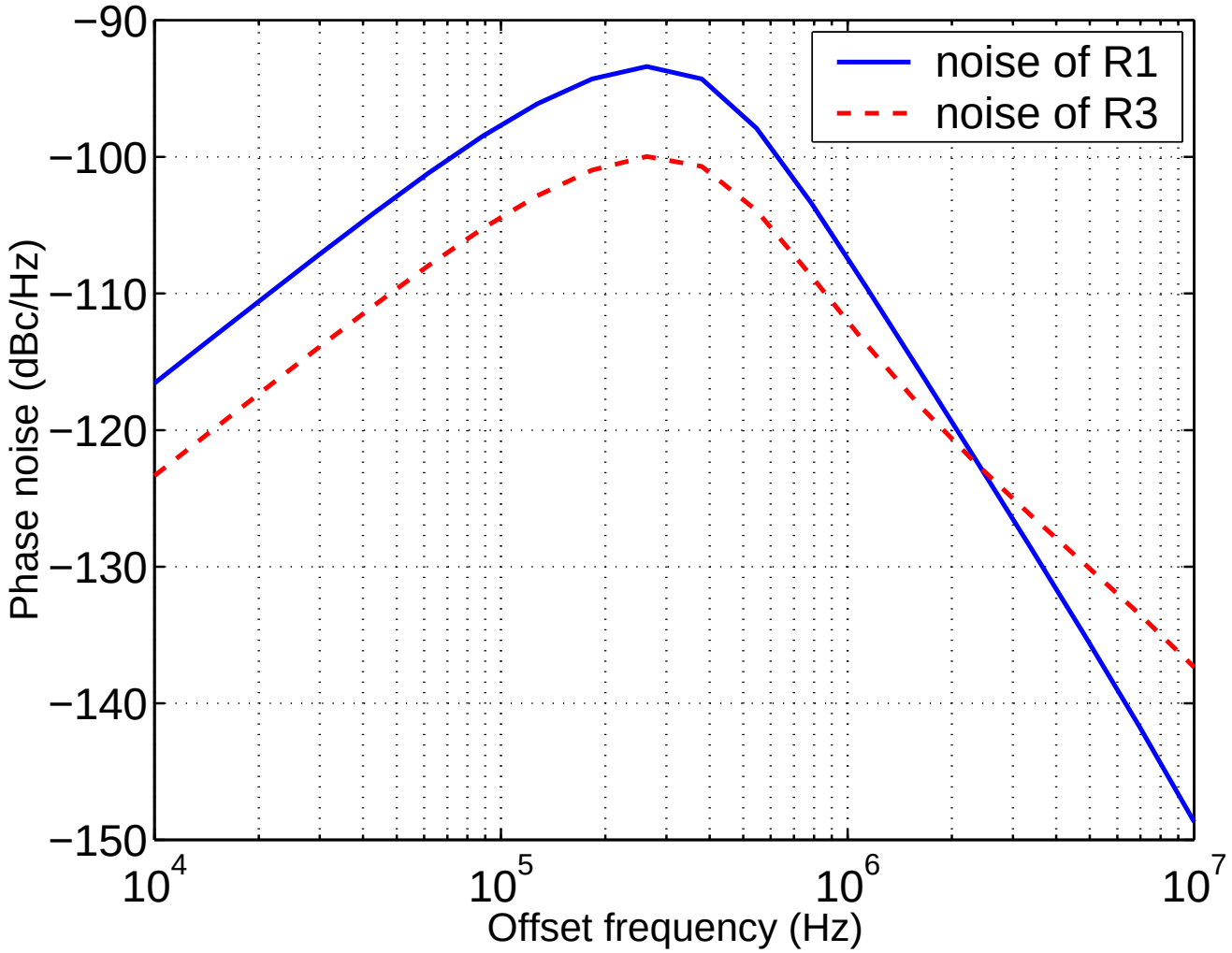
CHARGE PUMP AND LOOP–FILTER

- I=50μA
- R1=47kΩ
- R3=8kΩ
- C1=30pF
- C2=3.3pF
- C3=2pF



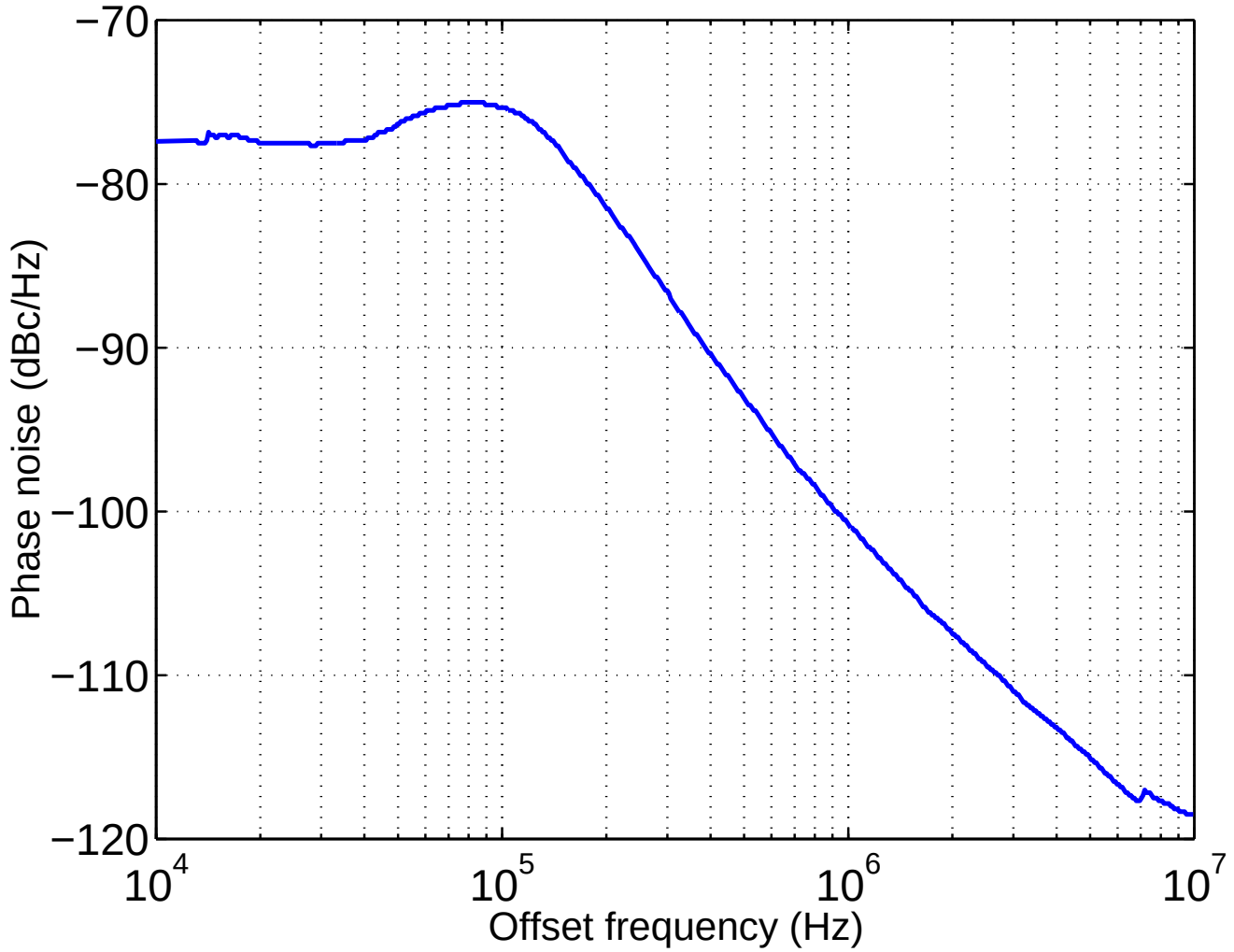
LOOP–FILTER NOISE

- L=-107dBc/Hz @ 1MHz
- L=-137dBc/Hz @ 10MHz
- L=-145dBc/Hz @ 22MHz



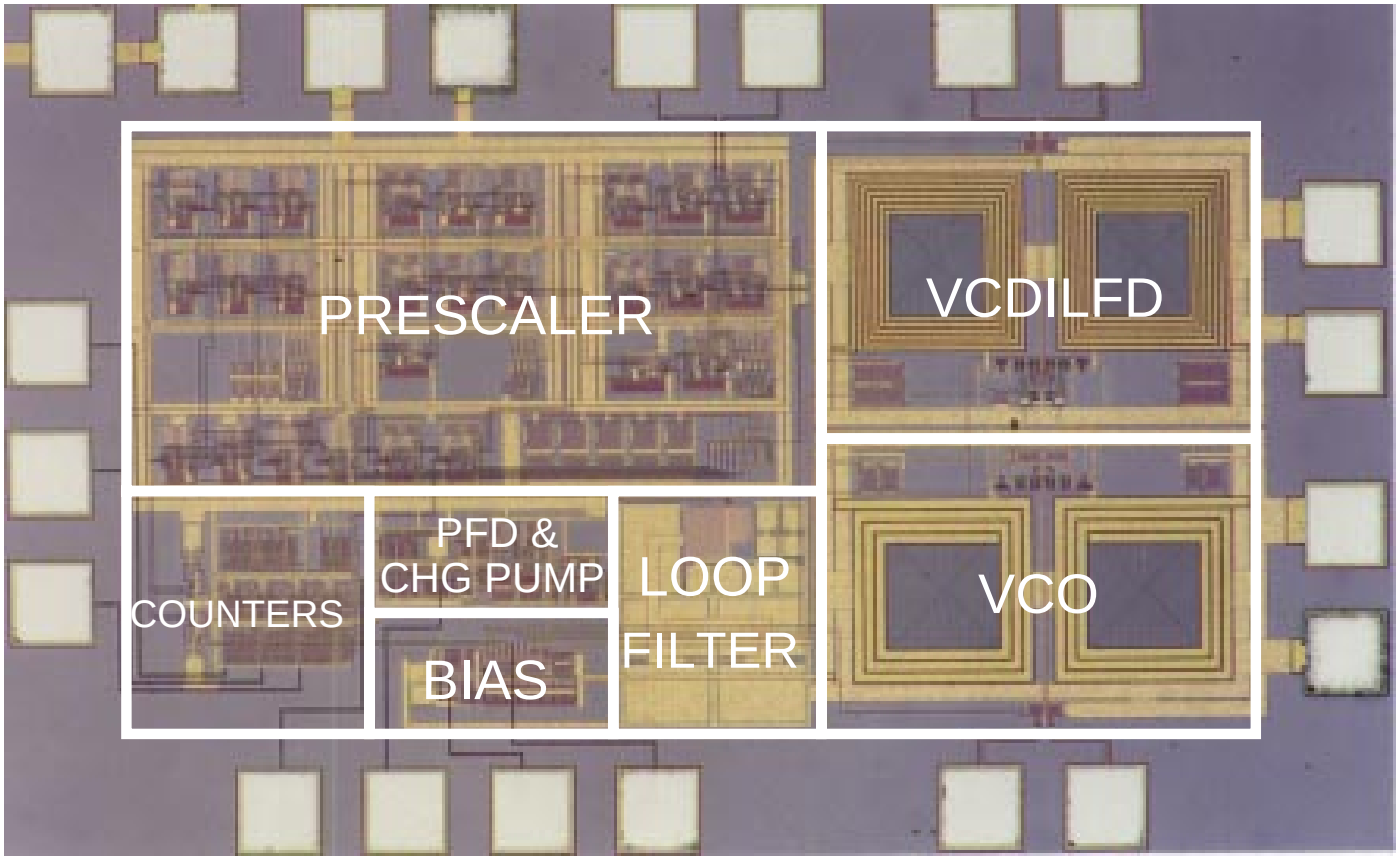
PLL PHASE NOISE

- L=-101dBc/Hz @ 1MHz
- L=-127.5dBc/Hz @ 22MHz



SYNTHESIZER CHIP MICROGRAPH

- 0.24μm CMOS
- area=1.6mm^2 (1mm$\times$ 1.6mm)



SUMMARY

Synthesized frequencies	4.840–4.994GHz
Reference frequency	11MHz
LO spacing	22MHz
Spurs	$\leq$ -45dBc @ f_{ref} , $\leq$ -54dBc @ 2 $\times f_{ref}$
Phase noise	-101dBc/Hz @ 1MHz
VCO power	3.0mW
VCDILFD power	1.2mW
Prescaler power	25.4mW
Total power	32mW
Supply voltage	2.0V (1.5V for VCO & VCDILFD)
Die area	$1.6\mathrm{mm}^2$
Technology	$0.24\mu\mathrm{m}$ CMOS

COMPARISON

reference	f (GHz)	power	L	FM	comment
Parker, JSSC 98	1.6	90mW	0.6μm	10.6	integer–N
Craninckx, ISSCC 98	1.8	51mW	0.4μm	14.1	fractional–N
Shahani, JSSC 98	1.6	36mW	0.5μm	22.2	dividerless
This work	5.0	32mW	0.24μm	37.5	integer–N

- FM=$\frac{f \times \mathrm{L}}{\mathrm{power}}$

CONCLUSION

- A 5GHz frequency synthesizer is fully integrated in 0.24μm CMOS
- power consumption is reduced by
  - employing a voltage–controlled ILFD
  - optimizing spiral inductors for the VCO and ILFD
  - taking advantage of quadrature outputs in the prescaler
- loop–filter noise is kept small by using reasonably small resistors
- low spurious side bands are achieved by
  - using a semi–differential charge pump
  - designing a fourth–order loop

ACKNOWLEDGMENTS

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