Superharmonic Injection Locked Oscillators as Low Power Frequency Dividers

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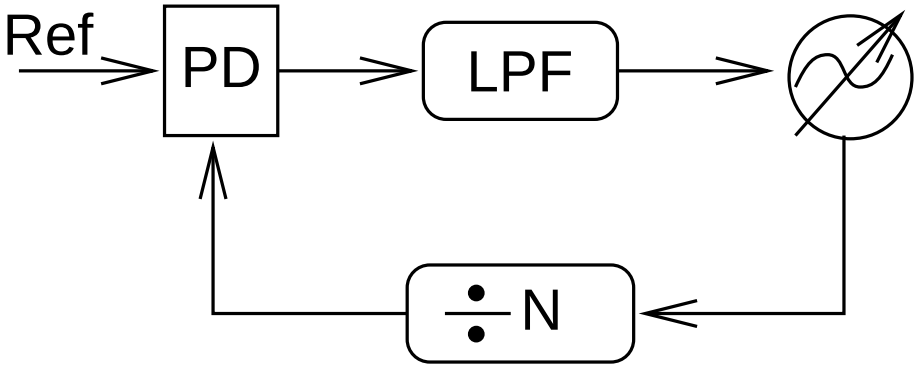
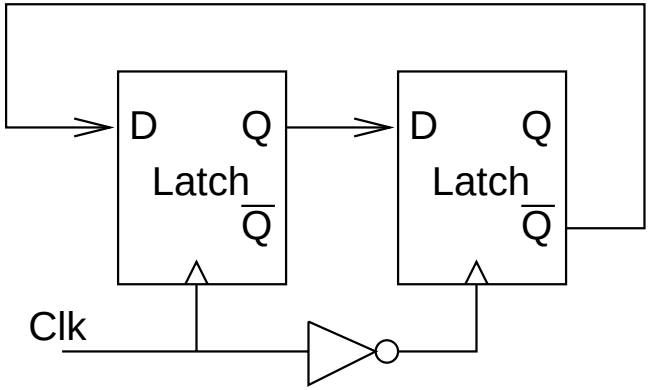
OUTLINE:

- Frequency dividers
  - Applications
  - Power and frequency issues (limitations/relations)
- Injection locked oscillators
  - Review of definitions
  - Mathematical model
  - Application as injection locked frequency dividers
- Simulation and measurement results
- Conclusion

FREQUENCY DIVIDERS

- Frequency dividers are widely used in the feedback path of phase locked loops.

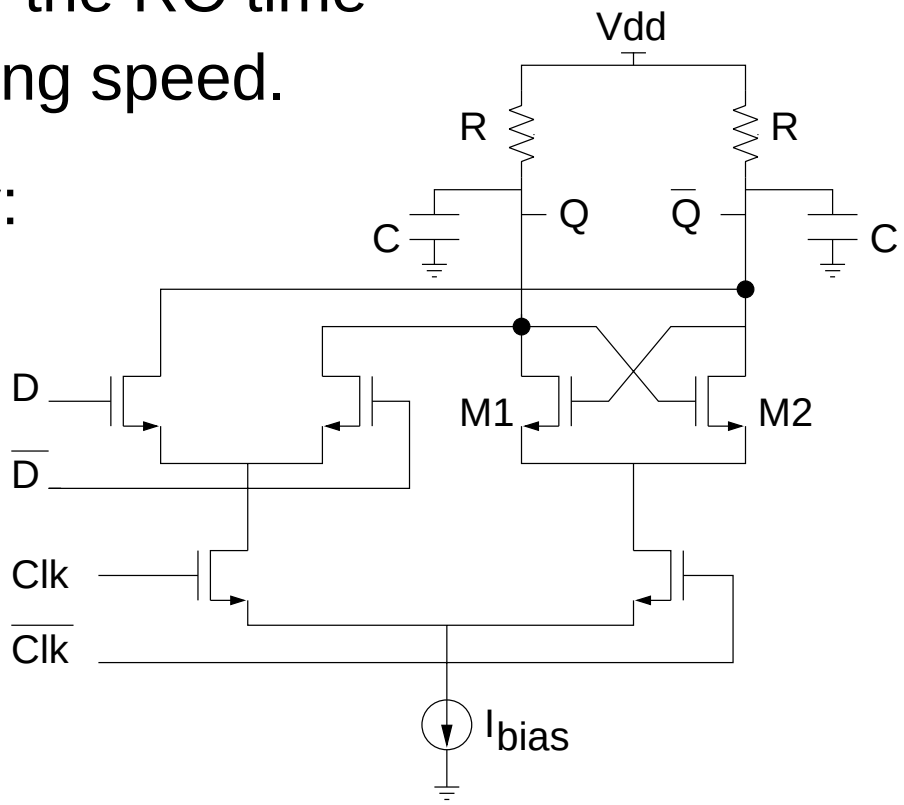




- Conventional frequency dividers:
  - Flip-flops are used to divide frequency.
  - Flip-flop based dividers are wide band.
  - Power consumption increases with the frequency of operation.

CONVENTIONAL FREQUENCY DIVIDERS

- Maximum frequency is limited by the RC time constant as well as M1/M2 latching speed.
- To operate at a higher frequency:
  - Reduce R $\Rightarrow$
    - $*$ Reduce RC time constant.
    - $*$ Increase M1/M2 latch time.
  - Increase I_{bias} $\Rightarrow$
    - $*$ M1 and M2 can latch.
    - $*$ Enough swing.
  - Increase power consumption.
- In CMOS logics, dynamic power $\propto CV^2 f$.



SOLUTION

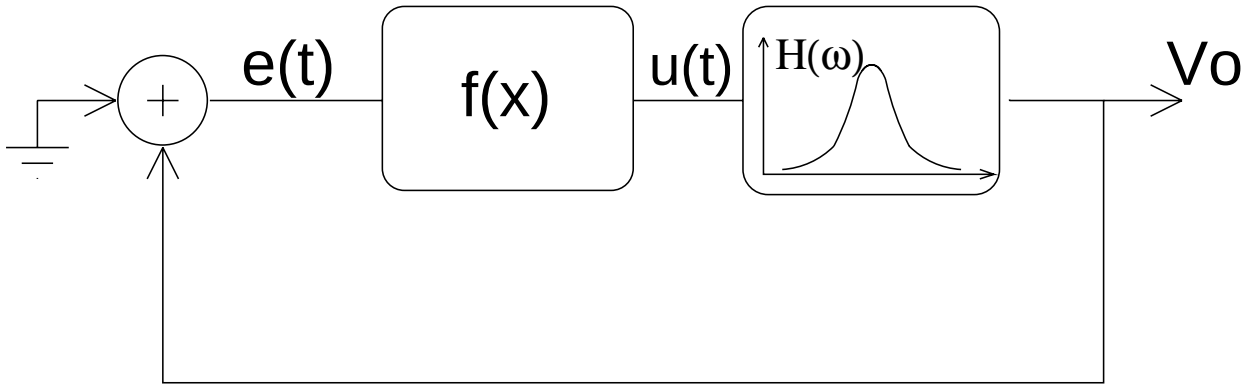
- Observation: Most wireless systems are narrow band.
- In order to increase speed and reduce power consumptions of frequency dividers:

Use resonators to trade off bandwidth for power and maximum frequency of operation.

INJECTION LOCKED OSCILLATORS

- By impressing an oscillator with an external (incident) signal, frequency locking can be achieved.
  - First-harmonic injection locked oscillators ($f_i = f_o$).
  - Subharmonic injection locked oscillators ($f_i = \frac{1}{N} f_o$).
  - Superharmonic injection locked oscillators ($f_i = N \times f_o$).

MODEL FOR LC OSCILLATORS

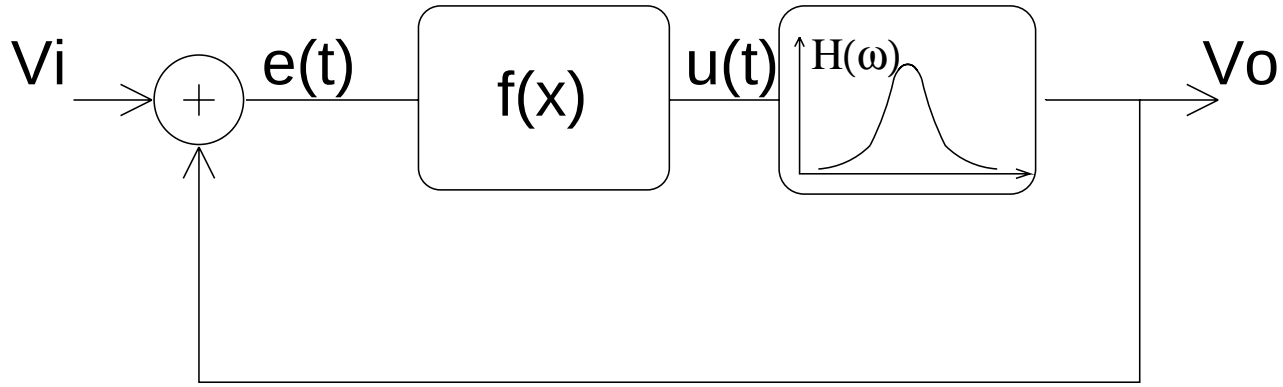


$f(x)$: A nonlinear function.

$$H(\omega) = \frac{H_0}{1 + j2Q\frac{\Delta\omega}{\omega_r}}$$

- Oscillation condition:
  - loop gain of unity
    - Gain condition: $|gain|$=1
    - Phase condition: $\Delta\varphi = 0$

MODEL FOR INJECTION LOCKED LC OSCILLATORS



$$\nu_o(t) = V_o cos(\omega_o t)$$

$$\nu_i(t) = V_i cos(\omega_i t + \phi)$$

$$u(t) = f[e(t)] = f[\nu_o(t) + \nu_i(t)]$$

- Oscillation condition should be satisfied in the presence of the incident signal.

Mathematical Model (Fundamental Equations)

- Satisfying the oscillation conditions $\Rightarrow$

$$V_o = H_o[K_{0,1} + \frac{1}{2}\sum_{m=1}^{\infty} K_{m,Nm\pm1} cos(m\phi)]$$

$$2V_oQ\frac{\Delta\omega}{\omega_r} = \frac{H_0}{2}\sum_{m=1}^{\infty} K_{m,Nm\pm1} sin(m\phi)$$

Special Case (Divide By Two)

$$f(x) = a_0 + a_1 x + a_2 x^2 + a_3 x^3$$

- Phase condition:

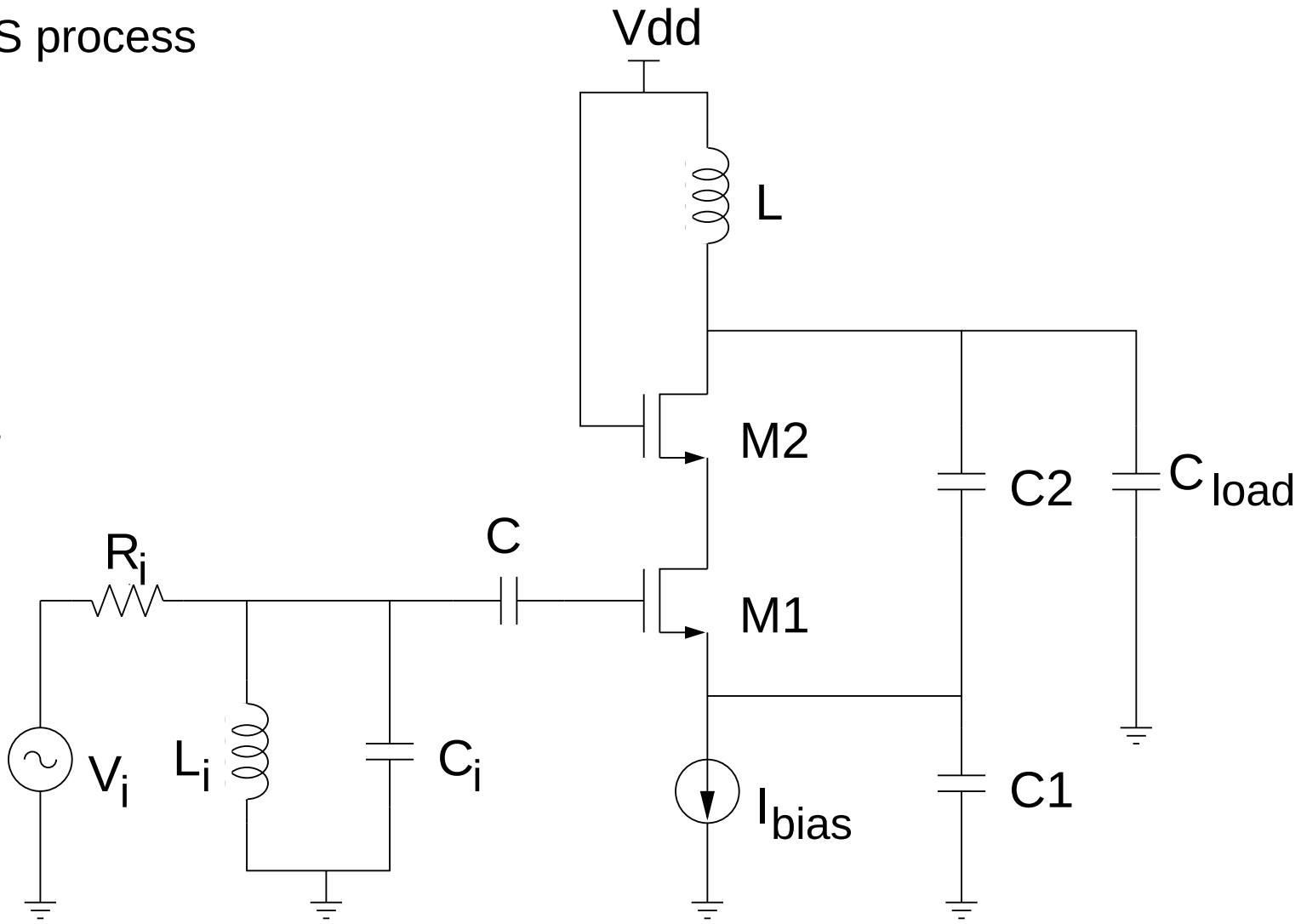
$$\left|\frac{\Delta\omega}{\omega_r}\right| < \left|\frac{H_0 a_2 V_i}{2Q}\right| \qquad , \qquad \frac{H_0}{Q} = \frac{LQ\omega_r}{Q} = L\omega_r$$

- Gain condition:

$$V_o = \sqrt{\frac{4}{3}\frac{1}{a_3 H_0}[1 - H_0(a_1 + \frac{3}{2}a_3 V_i^2 + a_2 V_i cos(\phi))]}$$

SINGLE ENDED ILFD

- 0.5μm CMOS process
- Vdd=2.5V
- I_{bias}=1.2mA
- f_o=920MHz
- f_i=1840MHz



SIMULATIONS (SINGLE ENDED ILFD)

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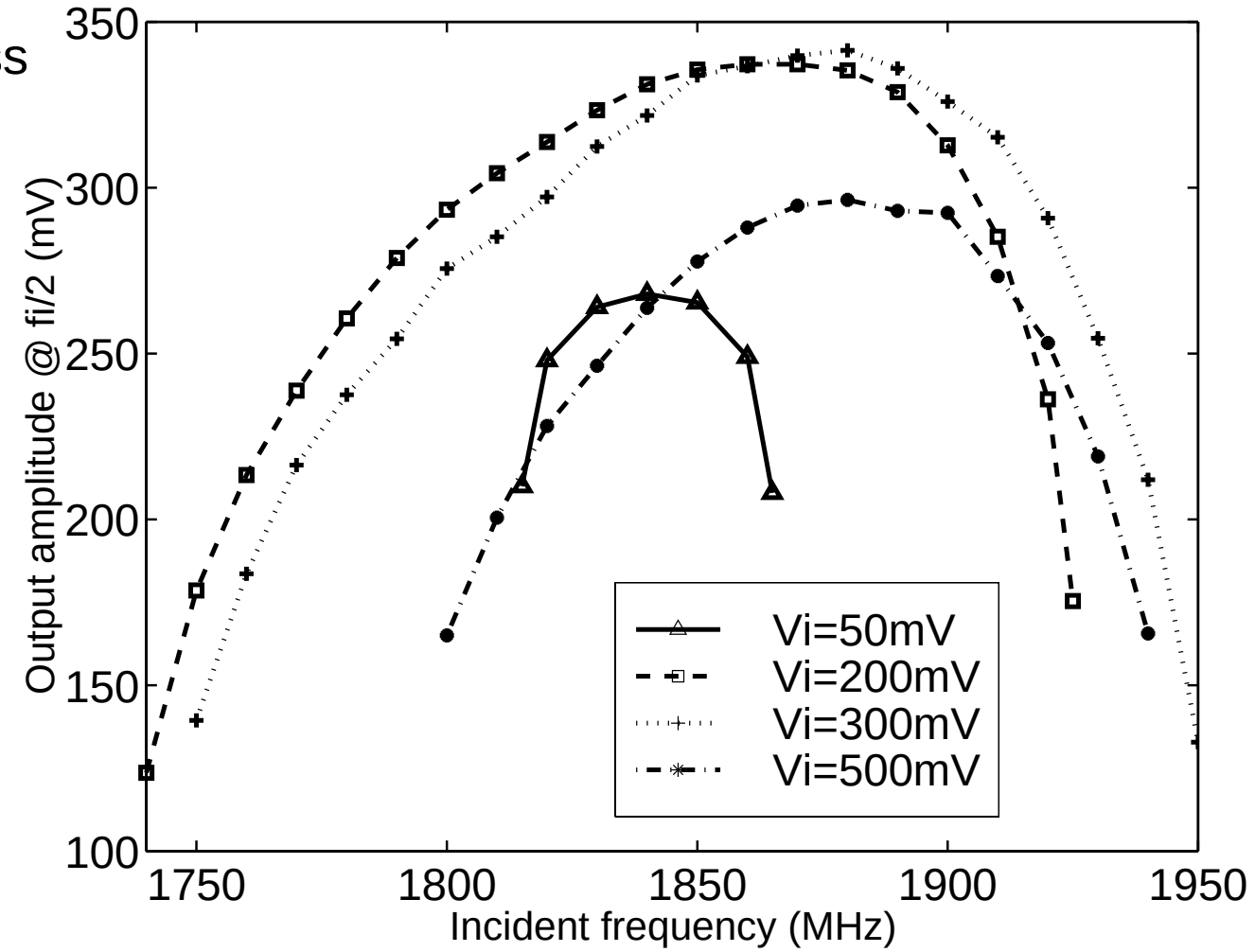
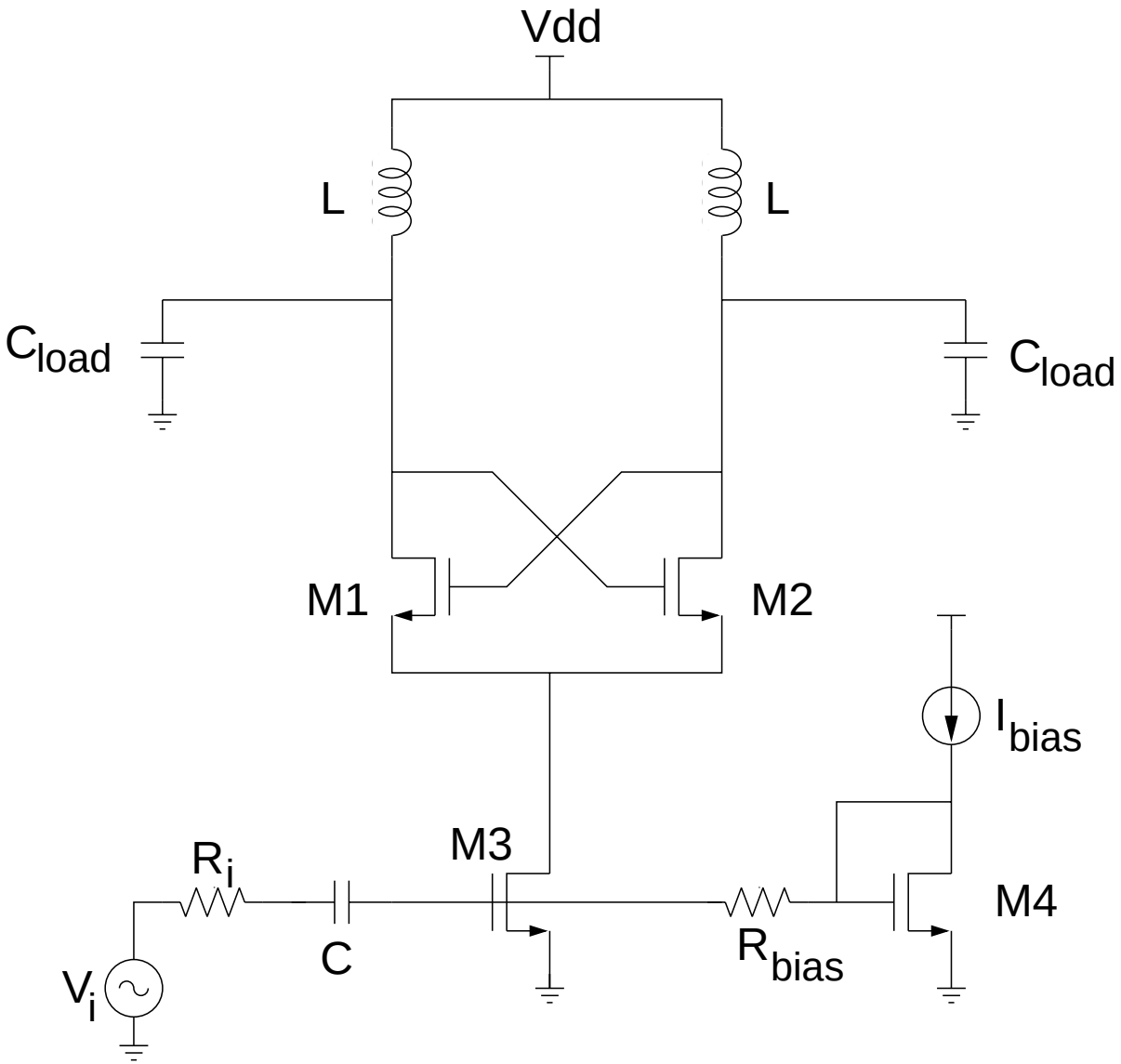


DIFFERENTIAL ILFD

- 0.5μm CMOS process
- Vdd=1.5V
- I_{bias}=300μA
- f_o=1.6GHz
- f_i=3.2GHz



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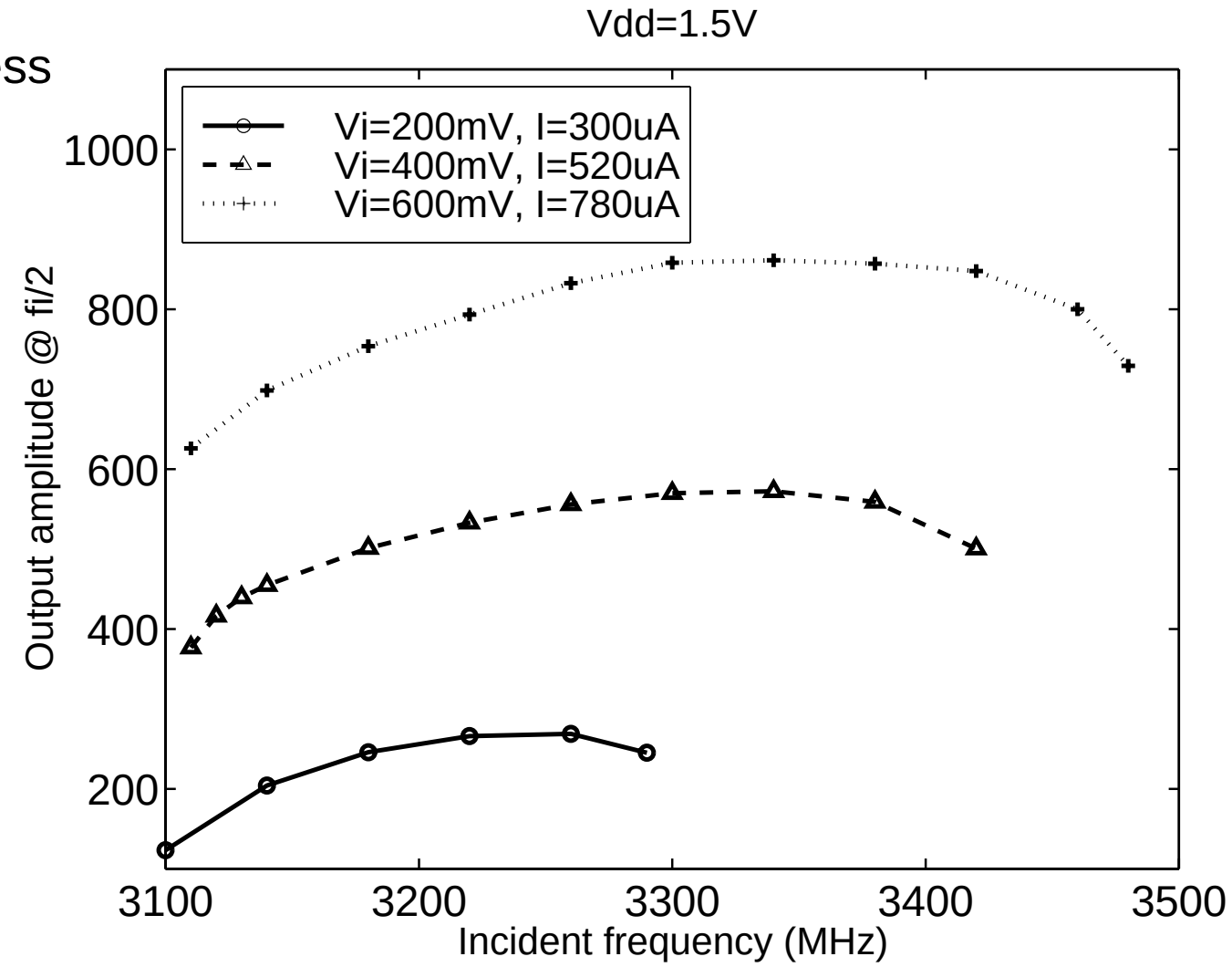

MEASUREMENTS (SINGLE ENDED ILFD)

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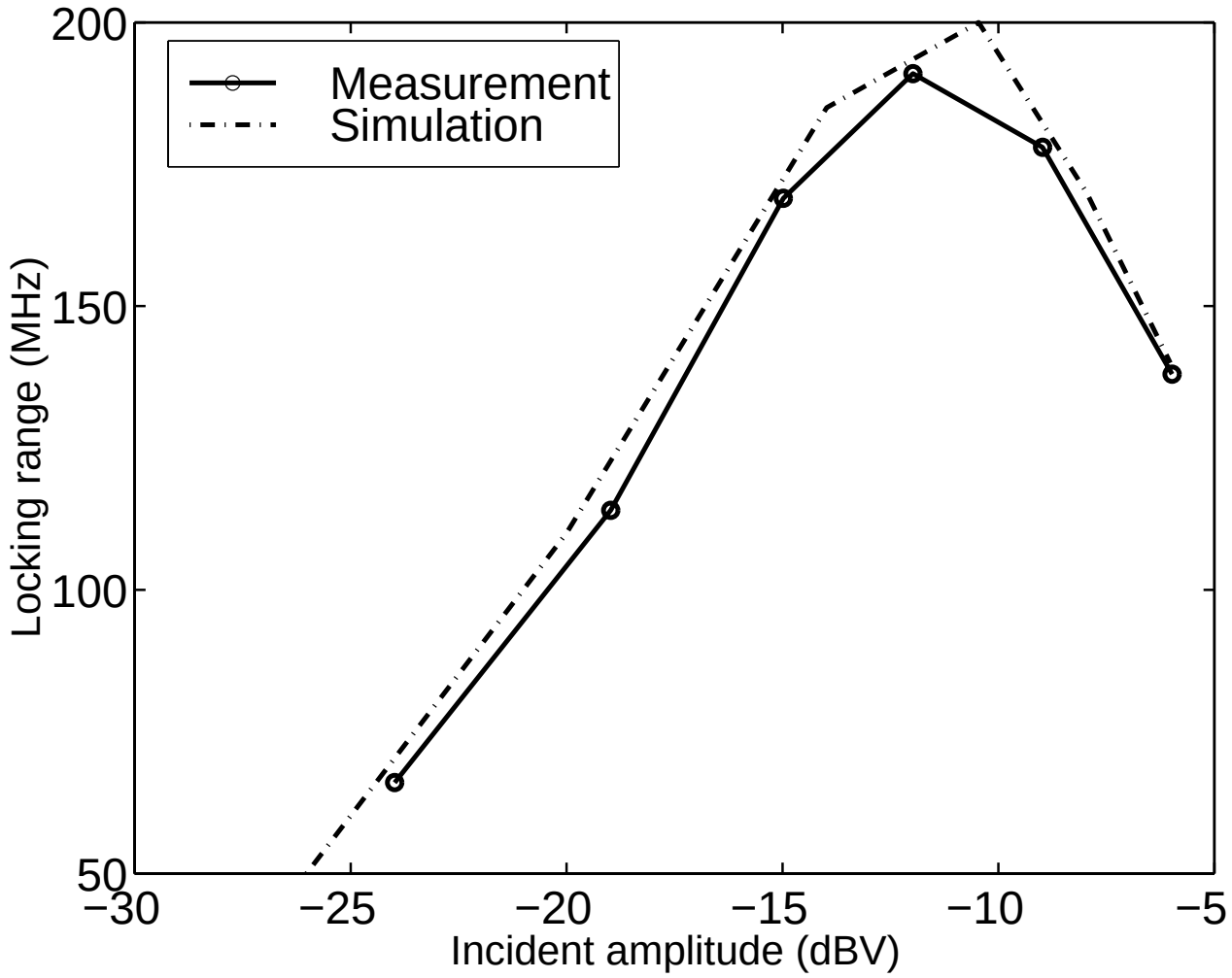

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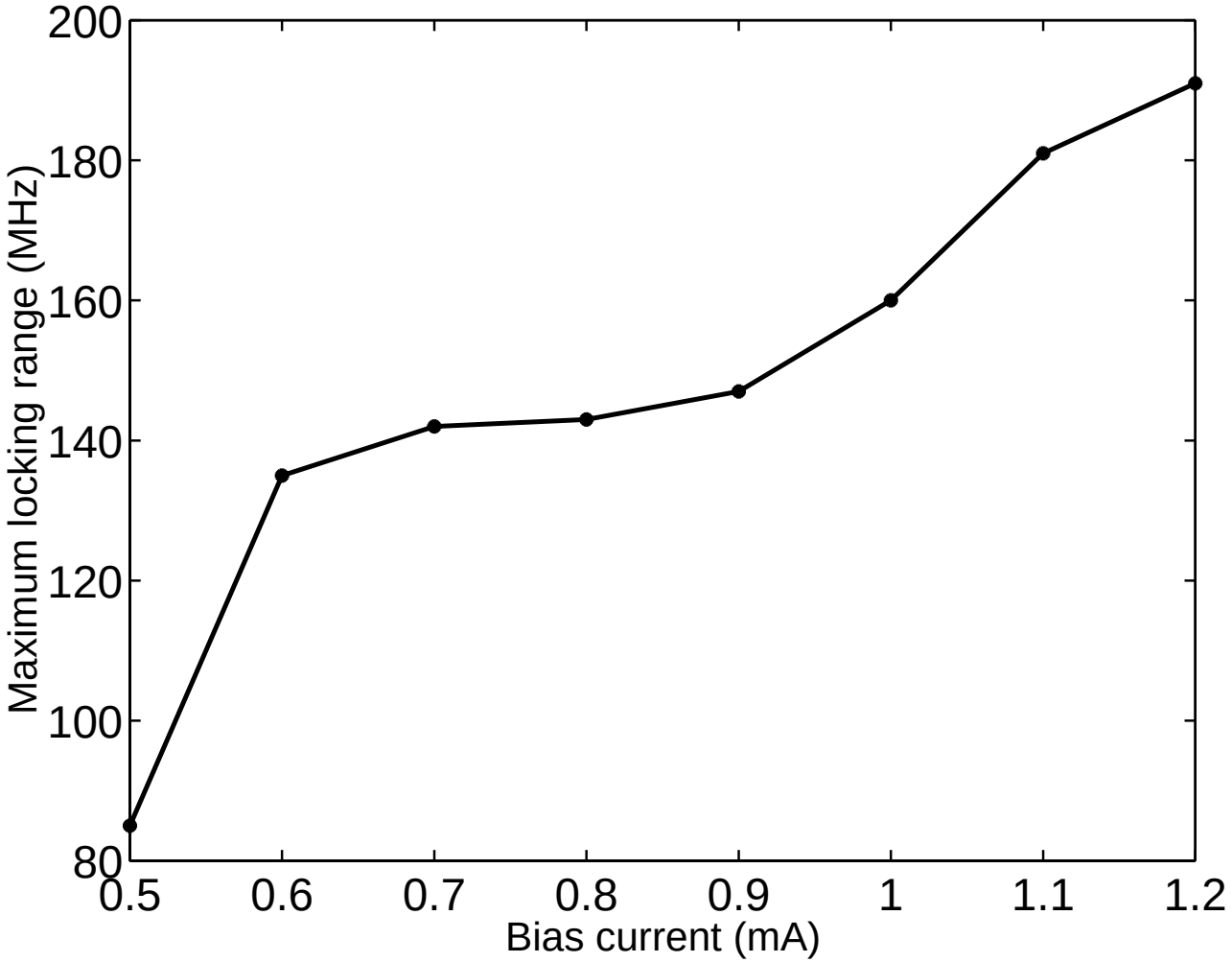

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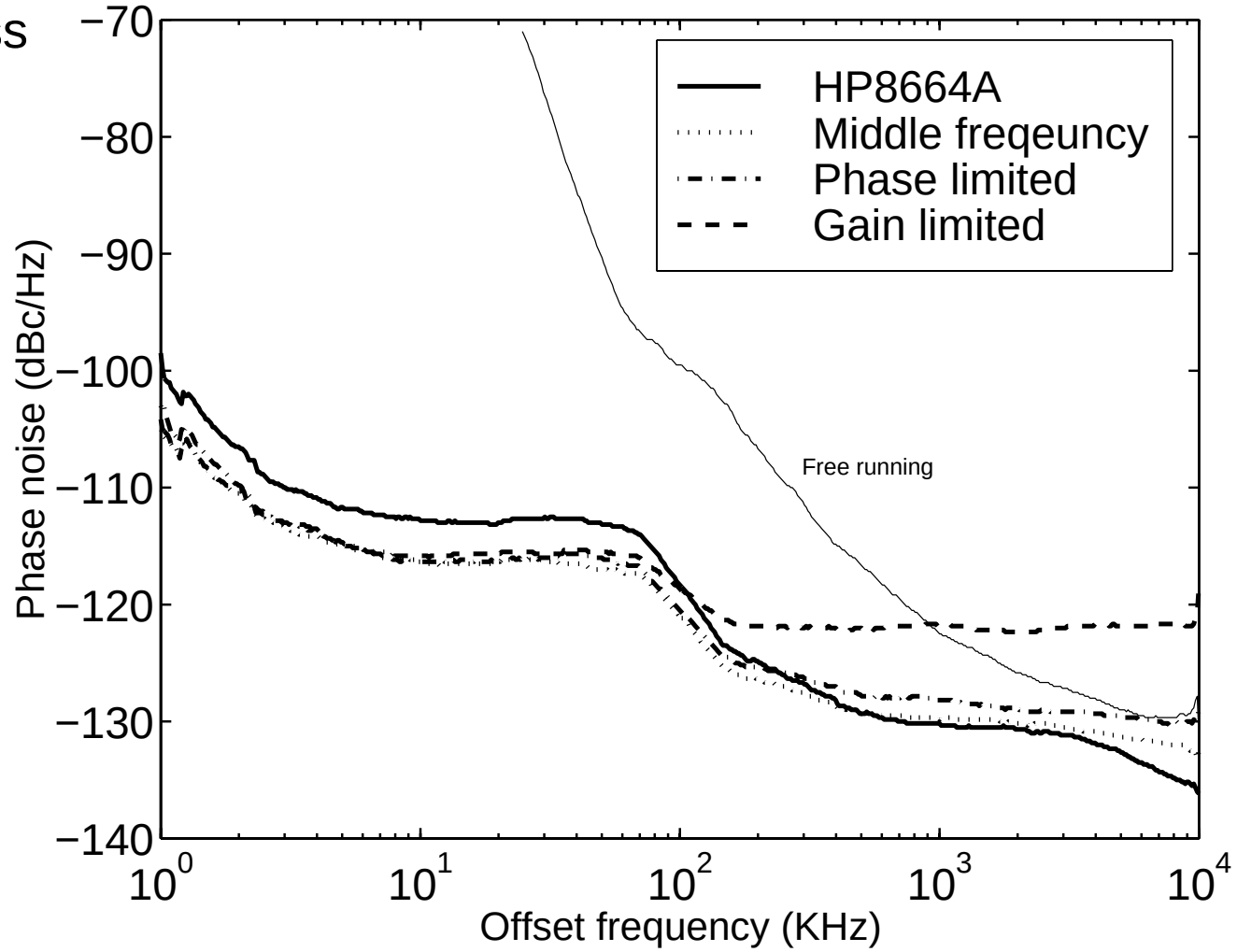
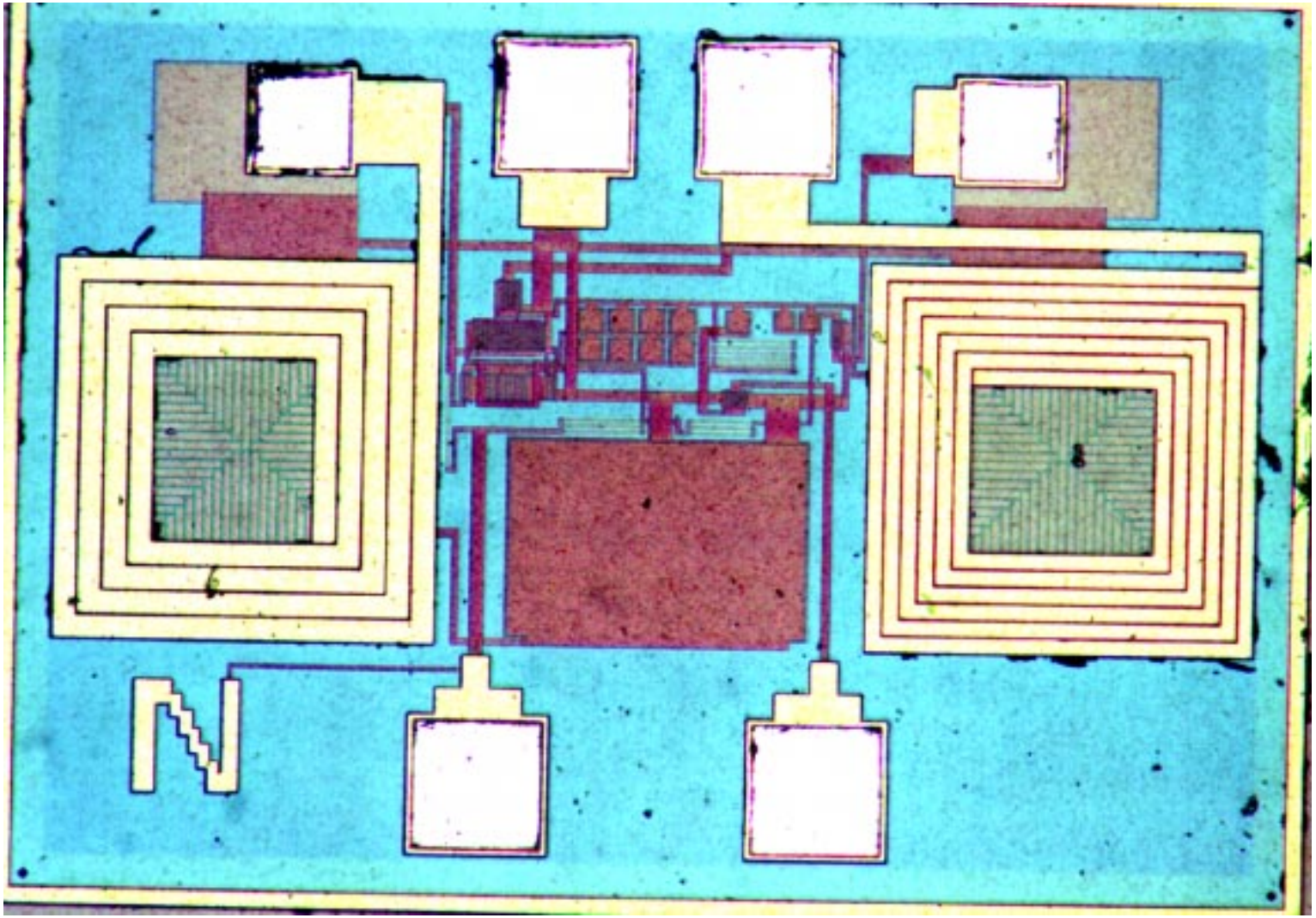


Chip Micrograph



PERFORMANCE SUMMARY

- $0.5\mu m$ CMOS process.

Divider	f(GHz)	Vdd(V)	$I_{bias}(\mu A)$	Power(mW)	Δf(MHz)
SiLFD (Measured)	1.8	2.5	600	1.5	135
			1200	3.0	191
DiLFD (Simulated)	3.5	1.5	300	0.45	190
			400	0.60	260
			780	1.17	370
SCL Flip-flop (Simulated)	1.8	2.0	1000	2.0	1800
	3.0	Failed			

CONCLUSION

- A new model for injection locked oscillators is developed which:
  - Predicts the locking range.
  - Describes two different mechanism through which injection locking fails.
- Superharmonic injection locked oscillators are designed as very high frequency and low power frequency dividers.
- Unlike conventional frequency dividers, the power consumption of an ILFD does not necessarily increase with frequency of operation.
- Using injection locking techniques, one can design frequency dividers at frequencies where conventional architectures fail.

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