Analysis and Optimization of Accumulation-Mode Varactor for RF ICs

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Abstract— **This paper presents a novel RF IC varactor implemented in standard CMOS process. This device has shown a remarkable tuning range of 150%, sensitivity of 300%/V, and quality factor of 23 at 1 GHz. A physical model of the varactor is presented and confirmed with measured data. Using the model derived, optimization has shown that a Q as high as 200 can be achieved.**

I. Introduction

High quality on-chip varactors are essential to monolithic integration of voltage-controlled oscillators in a Si-based RF ICs. Conventionally, on-chip varactors have been implemented with pn junctions under reverse bias or MOS capacitors in depletion-inversion regime. PN-junction varactors have been reported with quality factor (Q) of less than 7 for capacitance of 1–10 pF at 0.9–2.4 GHz. Typical MOS capacitors can achieve higher Q (14/GHz/pF) with larger capacitance per area [1]. In this paper, we present a novel varactor based on an NMOS-like structure biased in accumulation-depletion regime. A physical model is presented and verified with measured data. Based on the derived model, device optimization is performed.

II. Physical Models

A cross-sectional view of the accumulation-mode varactor is shown in Fig. 1. The structure is similar to an n-channel MOSFET with the exception of being fabricated in an n-well instead of the normal p-substrate. This choice was made to eliminate the parasitic pn-junction capacitances at source and drain that would otherwise limit the tuning range. An alternative structure using a p-channel MOSFET in a p-well/substrate has inferior quality due to lower carrier mobility. The basic operation of this device is similar to a standard MOS structure [2]. When the applied voltage (V_g) is far above the flatband voltage ($V_{\rm FB}$), the silicon surface is accumulated with electrons provided by the n^+ regions and the capacitance seen from the gate is simply the oxide capacitance. As V_g is decreased towards $V_{\rm FB}$, the silicon surface is less accumulated and eventually becomes charge-free at flatband, beyond which the surface undergoes depletion. From deep accumulation to strong depletion, the capacitance varies from a maximum to a minimum value. The region of interest where capacitance changes involves both accumulation and depletion operations. The models under these operating conditions are shown in Fig. 2.

In accumulation, the overall capacitance is mainly the series combination of the oxide capacitance $C_{\rm ox}$ and semiconductor capacitance $C_{\rm Si}$. Loss is represented by a combination of gate resistance R_g, accumulation-layer resistance $R_{\rm acc}$, S/D resistance R_d, and well resistance R_w. In depletion, the silicon surface consists of fixed donor charges only and lacks conducting majority carriers. The depletion model is similar to the accumulation model with additional depletion capacitance C_d at the channel-to-S/D interface. By performing network transformation on the models, equivalent series resistance R_s and capacitance C_s can be derived and Q can then be computed as $1/(\omega R_s C_s)$.

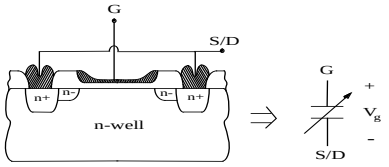

Fig. 1. Cross-section of accumulation-mode varactor

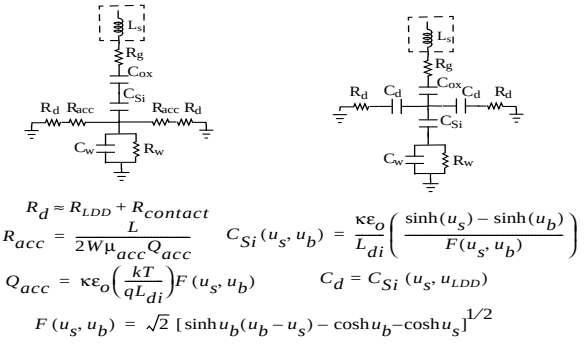

Fig. 2. (a) Accumulation model. (b) Depletion model.

III. Experimental Results and Discussion

A varactor shown in Fig. 3 was fabricated in a standard 0.5-μm CMOS process with effective channel length of 1.95 μm. S_{11} was measured using an HP8720B Network Analyzer and Cascade Microtech coplanar ground-signal-ground probes. R_s and C_s are extracted and plotted in Fig. 4 and 5, respectively. The measured C_s exhibits a normal high-frequency C-V characteristic and remains relatively independent of frequency up to 3 GHz beyond which the parasitic series inductance L_s causes C_s to appear increasing with frequency. The effective series capacitance $C_{\rm s,eff}$ can be described by $C_s/(1-\omega^2 L_s C_s)$. According to this expression, $C_{\rm s,eff}$ deviates noticeably from C_s at high frequencies under accumulation condition as observed in

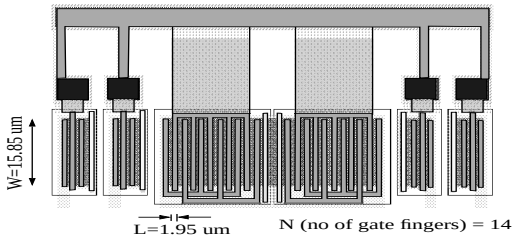

Fig. 3. Layout of the varactor tested

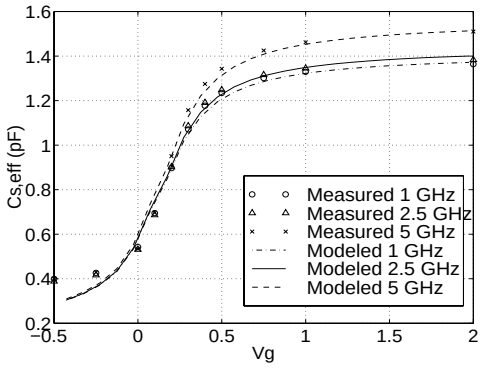

Fig. 4. Measured and Modeled effective series capacitance $C_{\mathrm{s,eff}}$

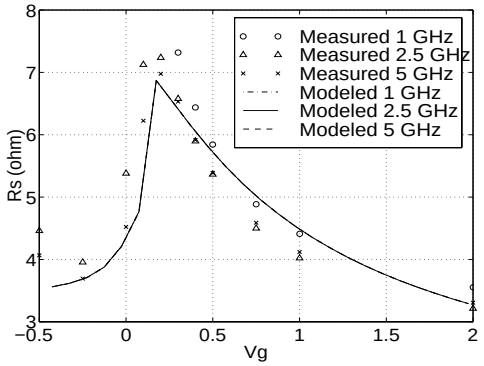

Fig. 5. Measured and Modeled series resistance R_s

Fig. 4.

The series resistance R_s in accumulation increases as V_g is swept from deep accumulation towards flatband. This is due to an increase in accumulation-layer resistance R_{acc} as majority carriers are extracted out through the n^+ regions. Below flatband, surface dopants are depleted leaving behind fixed donor charges. In depletion, loss is dominated by the well resistance R_w. R_s decreases below flatband because the semiconductor capacitance C_{Si} decreases, which reduces the effect of R_w. The measured R_s shows a slight frequency dependence which is unnoticeable in the model. This minor discrepancy can be attributed to the distributed nature of the well parasitics which is not adequately modeled by a single lumped RC element. Measured and modeled varactor Q are shown in Fig. 6.

In general, the modeled and measured results show excellent agreement. In accumulation, R_{acc} dominates the loss behavior. In depletion, the loss mechanism is dependent on the distributed well parasitics. Q reaches a minimum value around the flatband voltage where C_s variation is large and R_s is near maximum. This indicates a direct trade-off between Q and sensitivity, which can be specified as a constraint in device optimization.

IV. Device Optimization

Based on the derived model, optimization can be performed to determine the design parameters for achieving maximum Q in a given area. The device parameters, effective width (W), effective length (L) and number of gate fingers (N) are as defined in Fig. 3. The device is chosen to operate in accumulation mode where substrate noise coupled through the well has less effect. The optimization is conducted for a nominal capacitance of 1 pF with ± 30%-tuning capability at 1 GHz. Fig. 7 shows the resulting optimal Q, W, L, and N as a function of allowed area. As a larger area is allocated, Q can be increased to a maximum of 200, beyond which further area increase yields no improvement. This limit is achieved when L reaches a minimum governed by process technology. The result is consistent with the fact that Q in accumulation is largely determined by R_{acc} which is proportional to L and inversely proportional to W and N. This plot serves as a design tool for high-quality varactors.

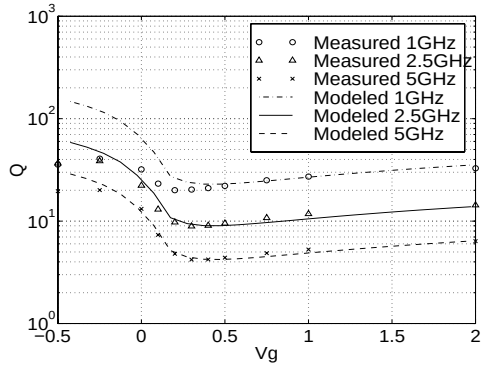

Fig. 6. Measured and Modeled Q

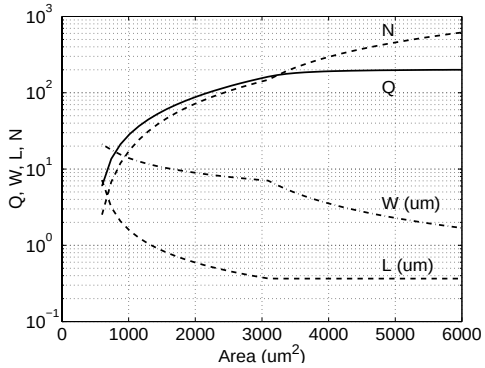

Fig. 7. Optimal Q, W, L, N vs allowed device area

V. Conclusions

A novel IC varactor is presented along with a physical model which has been verified with experimental data. Through optimization, design parameters for achieving Q as high as 200 have been determined.

Acknowledgments

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References

[1] J.N. Burghartz, M. Soyuer, K.A. Jenkins, "Integrated RF and Microwave Components in BiCMOS Technology," *IEEE Transactions on Electron Devices,* vol. 43, no. 9, Sept 1996.

[2] R.H. Kingston, S. F. Neustadter, "Calculation of the Space Charge, Electric Field, and Free Carrier Concentration at the Surface of a Semiconductor," *Journal of Applied Physics,* vol. 26, no. 6, June 1955.