A 1.5V, 1.5GHz CMOS Low Noise Amplifier

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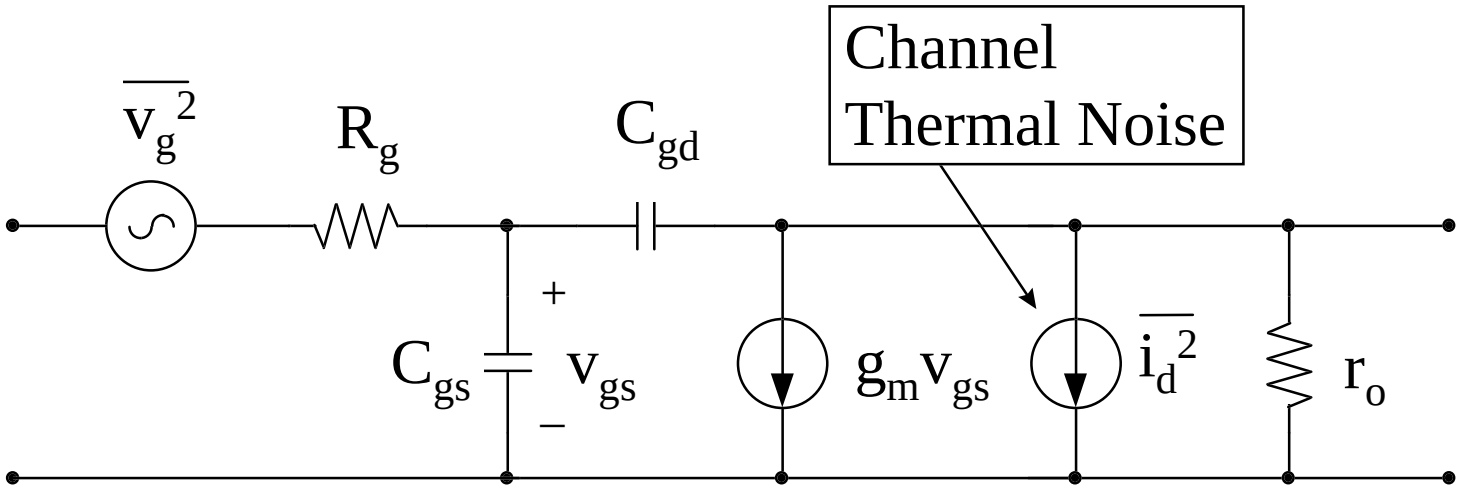
Outline

- *LNA Architecture / RF Noise*
- Experimental Results
- Summary and Conclusions

Simple CMOS Noise Model



- Channel thermal noise is dominant.

$$\overline{i_d^2} = 4kTB\gamma g_{d0}$$

- Gate resistance minimized by good layout.

Channel Thermal Noise

- Current HSPICE Implementation:

$$\overline{i_d^2} = \frac{8}{3} kTBg_m \qquad \text{(NLEV < 3)}$$

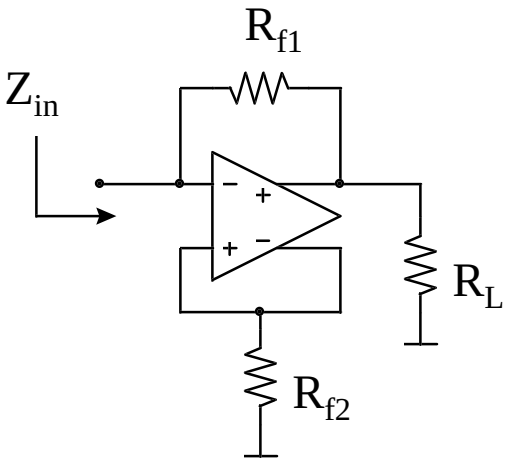
$$\overline{i_d^2} = \frac{8}{3} kTB \cdot K' \left(V_{gs} - V_T\right) \frac{1 + a + a^2}{1 + a} GDSNOI \qquad \text{(NLEV = 3)}$$

$$a = 1 - \frac{V_{ds}}{V_{dsat}}$$

- BSIM-3 Implementation:

$$\overline{i_d^2} = \frac{4kT\mu_{eff}}{L_{eff}^2} \left| Q_{inv} \right|$$

How To Get 50Ω

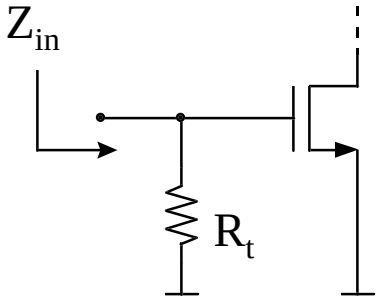


Dual Feedback

$$Z_{in} = \sqrt{R_{f1} R_{f2}}$$

Need high gain.

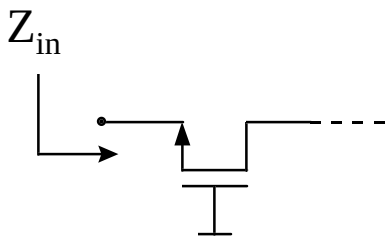
Stability problems.



Resistive Termination

$$Z_{in} = R_t$$

Poor NF.

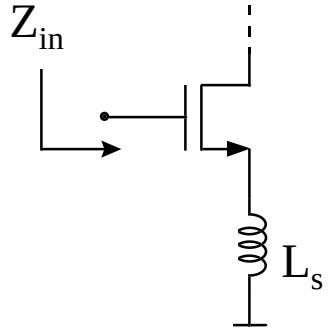


$1/g_m$ Termination

$$Z_{in} = \frac{1}{g_m}$$

NF > 3dB

($\gamma > 1$)



Inductive Degeneration

$$\mathrm{Re}\left[Z_{in}\right] = \frac{g_m}{C_{gs}} L_s$$

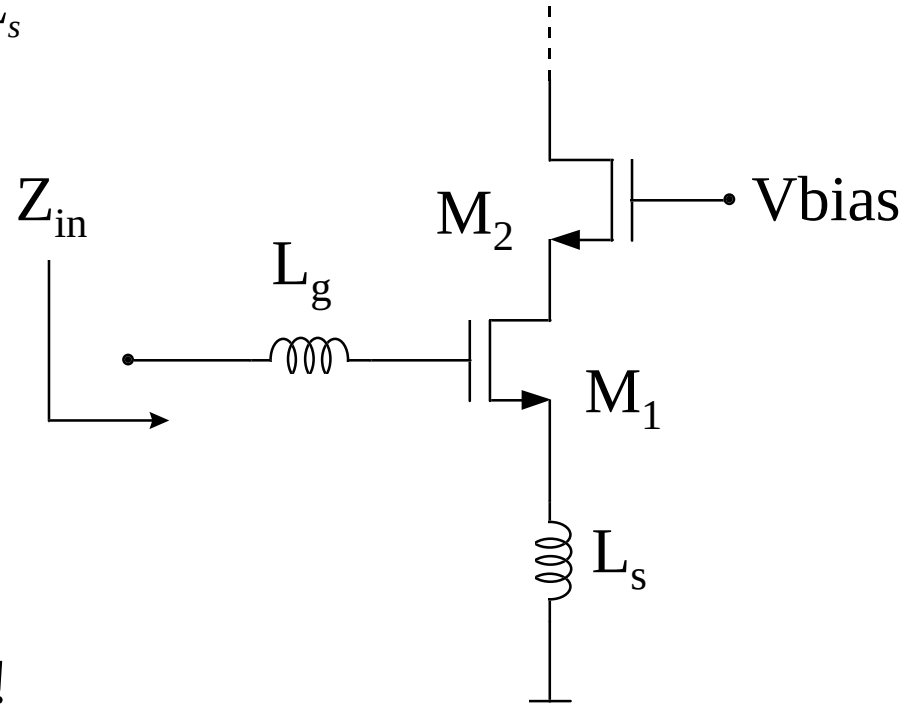
Narrowband.

LNA Input Stage

$$Z_{in} = s\left(L_s + L_g\right) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \approx \omega_T L_s$$

$$G_{m,eff} = g_{m1}Q_{in} = \frac{g_{m1}}{\omega C_{gs}\left(R_s + \omega_T L_s\right)}$$

$$= \frac{\omega_T}{\omega R_s\left(1 + \frac{\omega_T L_s}{R_s}\right)} = \frac{\omega_T}{2\omega R_s}$$



Note: $G_{m,eff}$ is <u>independent</u> of g_{m1}!

Noise Factor

A common form

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma g_{d0} R_s \omega^2 C_{gs}^2}{g_m^2}$$

A better form

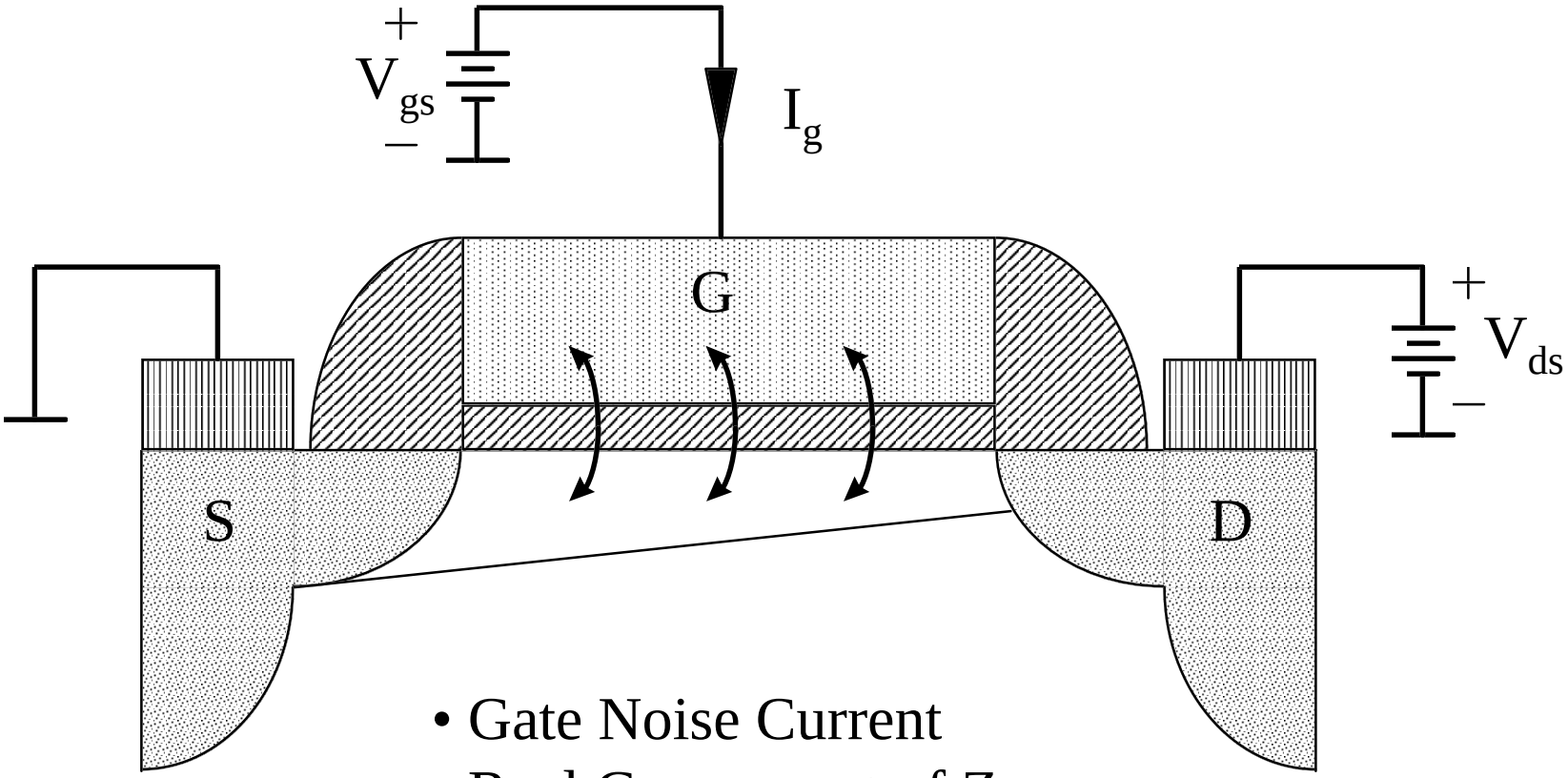
$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega}{\omega_T} \right)^2$$

- Reducing g_{d0}, Increasing Q_{in} lowers F!
- Achieving low F involves linearity tradeoff.

$$\left| V_{gs} \right| = Q_{in} \left| V_s \right|$$

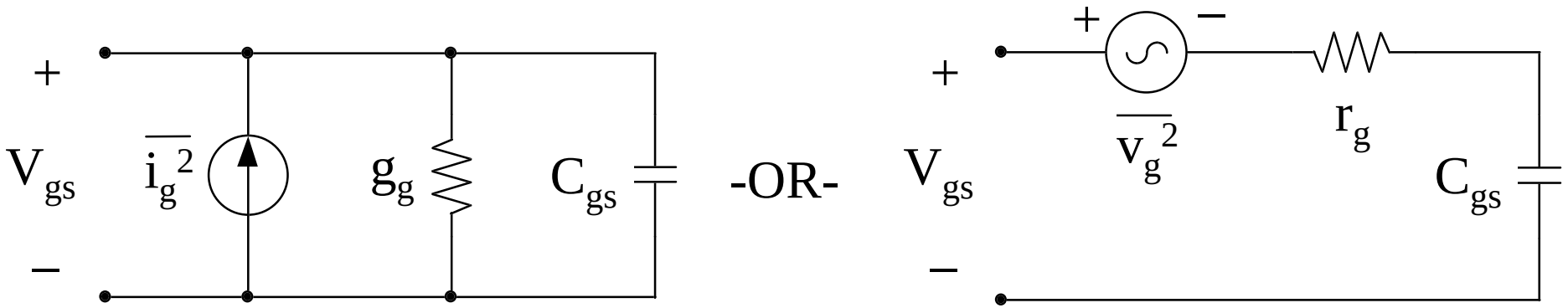
- Technology Scaling is Key.
- Problem : *The Free Lunch Principle*

Induced Gate Effects



- Gate Noise Current
- Real Component of Z_g

Equivalent Gate Circuit



$$\overline{i_g^2} = 4kTB\delta g_g \qquad g_g = \frac{1}{5}\frac{\omega^2 C_{gs}^2}{g_{d0}}$$

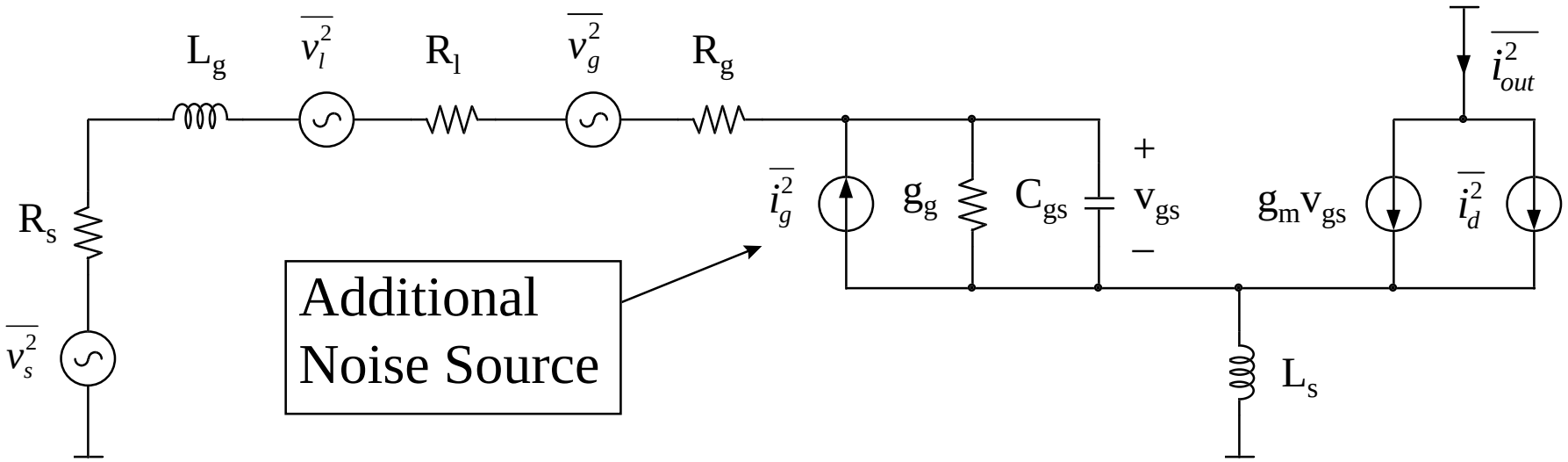
"Blue" Noise

$$\overline{v_g^2} = 4kTB\delta r_g \qquad r_g = \frac{1}{5g_{d0}}$$

"White" Noise

- δ (~ 4/3) modified by hot electron effects
- $\overline{i_g^2}$ partially correlated with $\overline{i_d^2}$ (c = 0.395j)
- $\overline{i_g^2}$ and g_g not modeled in HSPICE

Revised Noise Factor



$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega}{\omega_T} \right)^2 \left\{ 1 + 2\sqrt{\frac{\delta\alpha^2}{5\gamma}} Q_L |c| + \frac{\delta\alpha^2}{5\gamma} \left[1 + Q_L^2 \right] \right\}$$

(At Resonance)

Noise Factor Terms

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega}{\omega_T} \right)^2 \left\{ 1 + 2\sqrt{\frac{\delta\alpha^2}{5\gamma}} Q_L |c| + \frac{\delta\alpha^2}{5\gamma} \left[1 + Q_L^2 \right] \right\}$$

$$Q_L = \frac{\omega\left(L_s + L_g\right)}{R_s} = \frac{1}{\omega R_s C_{gs}} \approx 2 * Q_{in}$$

Q of the Input Circuit

$$\alpha = \frac{g_m}{g_{d0}} \leq 1$$

Decreases with shorter channels

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} = 0.395\,j$$

Gate / Drain Correlation Factor

Minimum Noise Factor

Take $\frac{\partial F}{\partial W_{M1}} = 0$ to find the condition for minimum F:

$$Q_{L,opt} = \sqrt{1 + \frac{5\gamma}{\delta\alpha^2}} \geq 1.87$$

← Long Channel Values

$$F_{\min} = 1 + \sqrt{\frac{4}{5}\delta\gamma}\left(\frac{\omega}{\omega_T}\right)\left\{|c| + \sqrt{1 + \frac{\delta\alpha^2}{5\gamma}}\right\} \geq 1 + 1.33\left(\frac{\omega}{\omega_T}\right)$$

Note: Worst-Case $F_{\min} = 4$ (6dB) when $g_m = g_g$.

Architecture / Noise Summary

- MOS Device has gate current noise in addition to drain current noise. ➡ Optimum Z_s exists.
- Optimum Q_{in} relatively large. ➡ Power savings *and* lower F by reducing W_{M1} for $Q_{in} < Q_{opt}$.
- HSPICE models of MOS noise are inadequate.
  - Induced gate effects are not modeled at all.
  - Hot Electron effects influence the noise power spectral density of channel-related noise sources.

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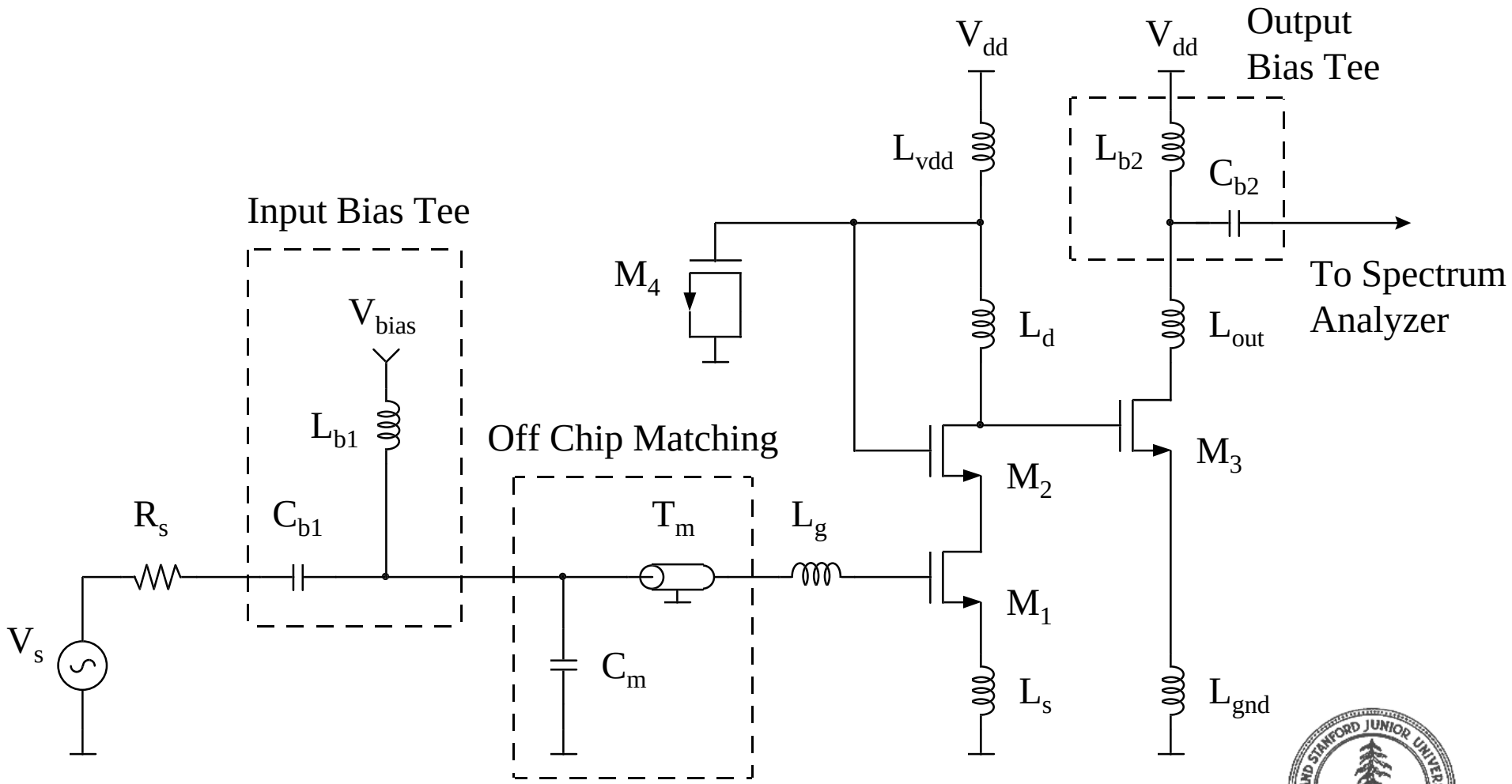
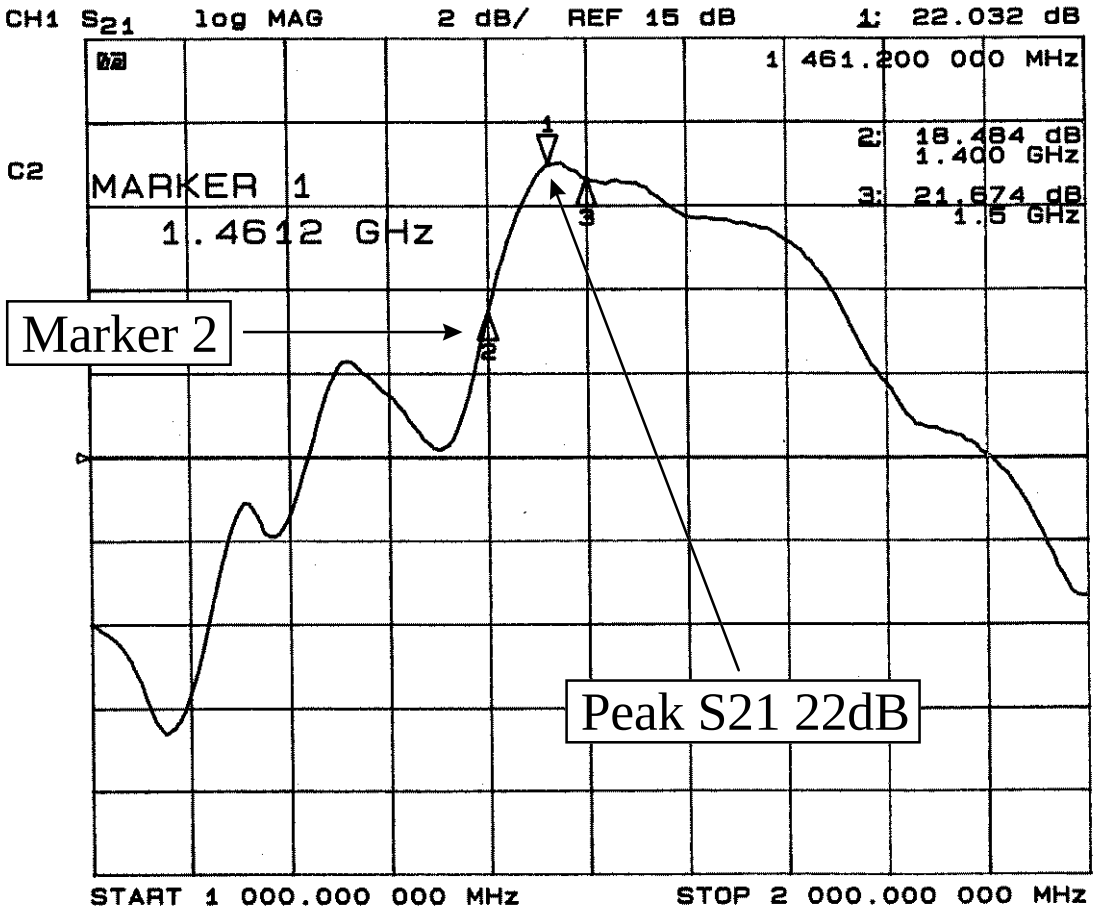
Complete LNA Schematic

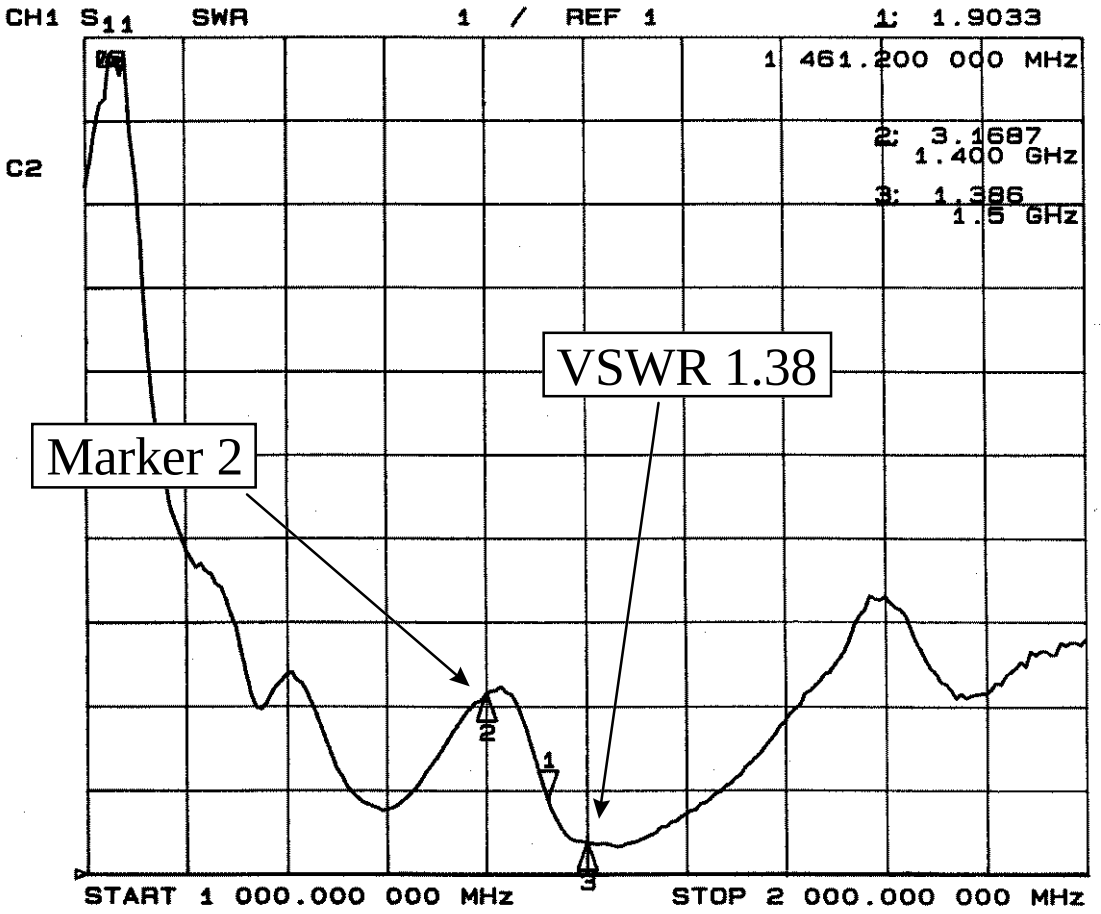


Die Photo

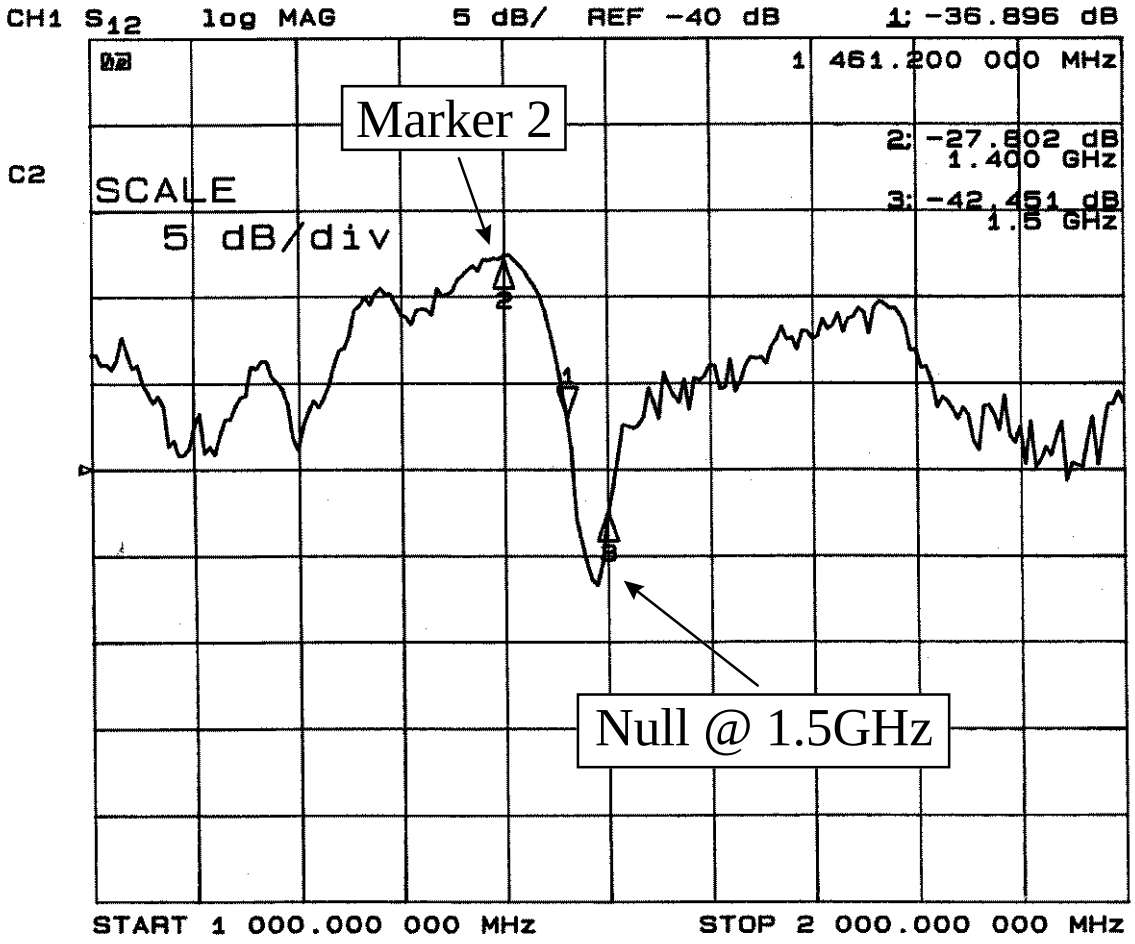
S21


CH1 S21 log MAG 2 dB/ REF 15 dB 1: 22.032 dB
1 461.200 000 MHz
2: 18.484 dB
1.400 GHz
3: 21.674 dB
1.5 GHz
C2
MARKER 1
1.4612 GHz
Marker 2
Peak S21 22dB
START 1 000.000 000 MHz
STOP 2 000.000 000 MHz

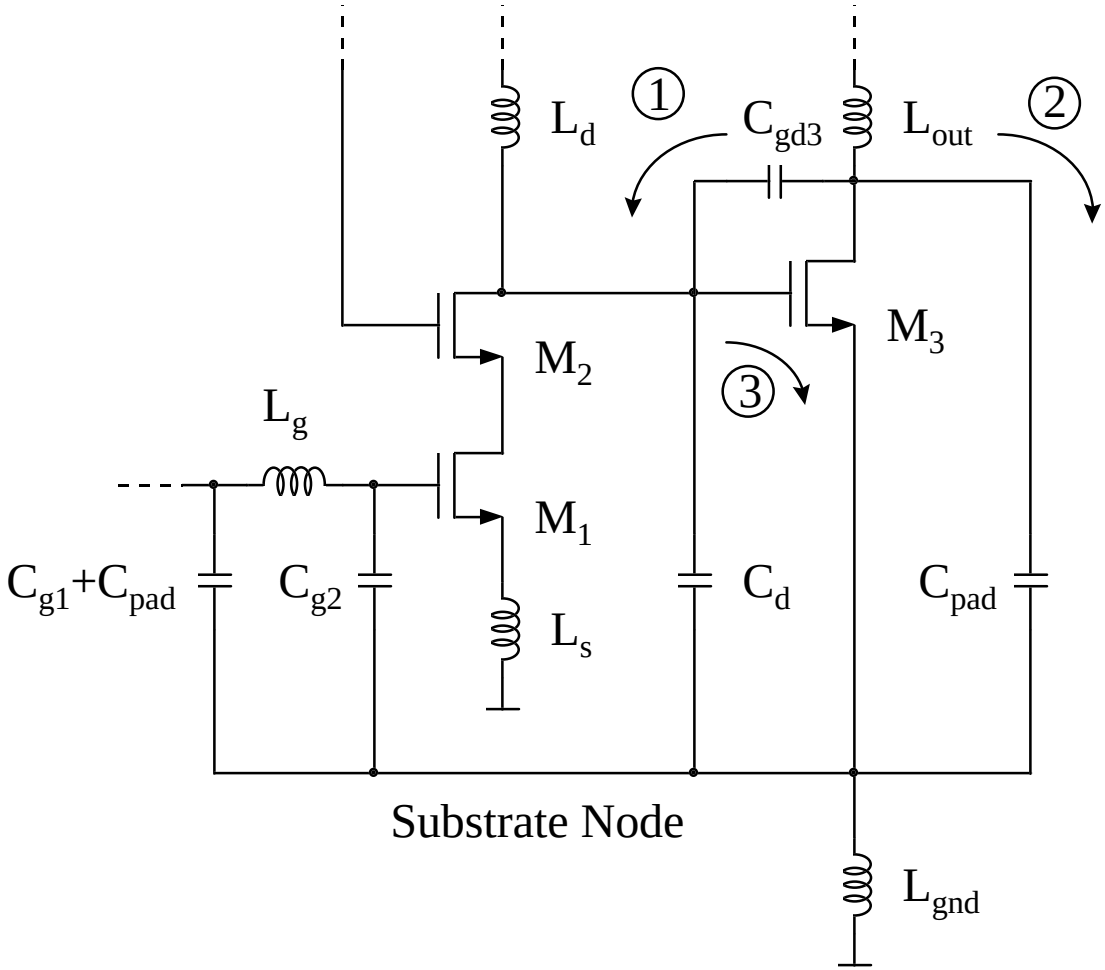
S11


CH1 S11 SWR
1 / REF 1
1: 1.9033
1 461.200 000 MHz
2: 3.1687
1.400 GHz
3: 1.386
1.5 GHz
C2
VSWR 1.38
Marker 2
START 1 000.000 000 MHz
STOP 2 000.000 000 MHz

S12

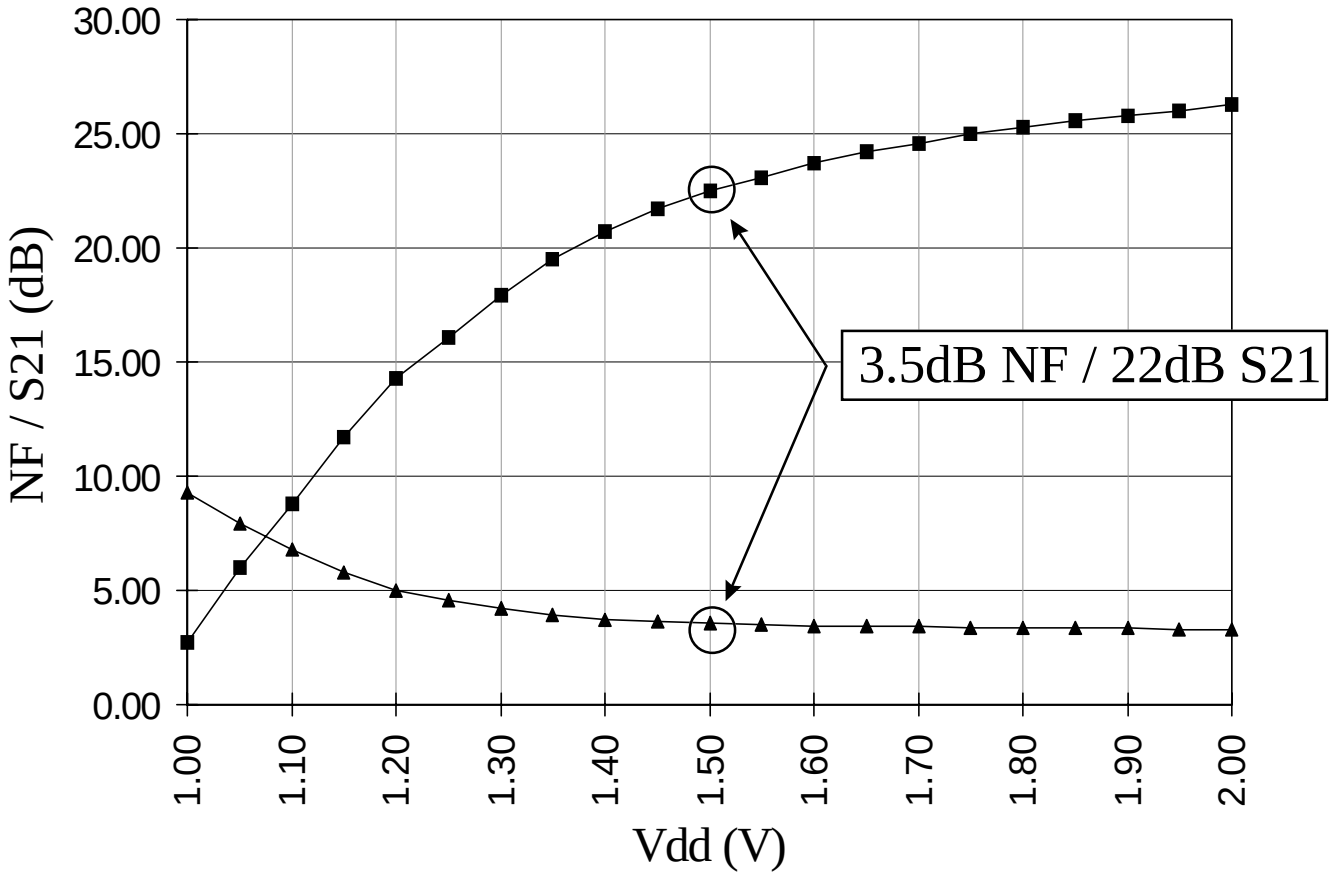

CH1 S12 log MAG 5 dB/ REF -40 dB 1: -36.896 dB
1 461.200 000 MHz
2: -27.602 dB
1.400 GHz
3: -42.451 dB
1.5 GHz
C2
SCALE
5 dB/div
Marker 2
Null @ 1.5GHz
START 1 000.000 000 MHz
STOP 2 000.000 000 MHz

Reverse Isolation

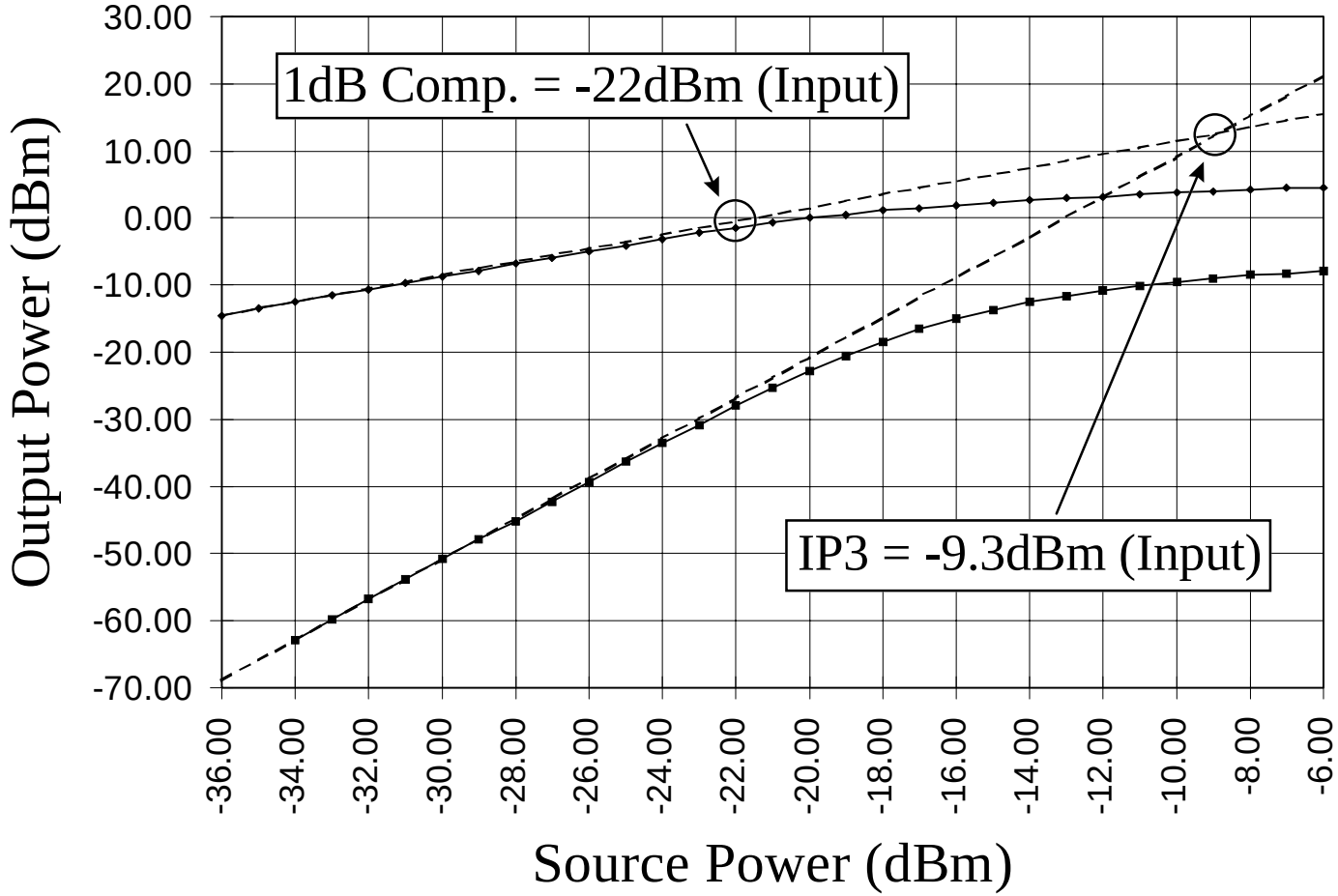


- Substrate tied to lowest inductance signal ground.
- Parasitic capacitances from spiral inductors and pads degrade reverse isolation.
- Simulation with parasitics shows null in S12 as seen in experimental data.

Noise Figure / S21 vs. Vdd



Linearity - IP3



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Performance Summary

Frequency	1.5GHz
Noise Figure	3.5dB
S21	22dB
IP3 (Input)	-9.3dBm
1dB Compression (Input)	-22dBm
Supply Voltage	1.5V
Power Dissipation	30mW
First Stage	7.5mW
Technology	0.6µm CMOS
Die Area	0.12 mm^2

Conclusions

- CMOS is suitable for low noise above 1GHz.
- 3.5dB NF is lowest to date for CMOS above 1GHz.
- 1dB NF can be expected with current generation.
- Current CMOS noise models, as in HSPICE, are inadequate for accurate simulation of RF noise.
  - Significant noise contributors are *absent* from the models.
  - Short channel effects have not been properly accounted for.
  - More research is required.

Acknowledgments

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for many helpful discussions on CMOS noise