A 1.5V, 1.5GHz CMOS Low Noise Amplifier

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Outline

• LNA Architecture / RF Noise
• Experimental Results
• Summary and Conclusions
Simple CMOS Noise Model

- Channel thermal noise is dominant.
  \[ \overline{i_d^2} = 4kTB\gamma g_{d0} \]
- Gate resistance minimized by good layout.
Channel Thermal Noise

• Current HSPICE Implementation:

\[ \overline{i_d^2} = \frac{8}{3} kTB g_m \]  
\[ \overline{i_d^2} = \frac{8}{3} kTB \cdot K' \left( V_{gs} - V_T \right) \frac{1 + a + a^2}{1 + a} GDSNOI \]  
\[ (NLEV < 3) \]

\[ a = 1 - \frac{V_{ds}}{V_{dsat}} \]

• BSIM-3 Implementation:

\[ \overline{i_d^2} = \frac{4kT\mu_{eff}}{L_{eff}^2} |Q_{inv}| \]
How To Get $50\Omega$

- **Dual Feedback**
  \[ Z_{in} = \sqrt{R_{f1}R_{f2}} \]
  Need high gain.
  Stability problems.

- **Resistive Termination**
  \[ Z_{in} = R_t \]
  Poor NF.

- **$1/g_m$ Termination**
  \[ Z_{in} = \frac{1}{g_m} \]
  NF $> 3$dB
  \((\gamma > 1)\)

- **Inductive Degeneration**
  \[ \text{Re}[Z_{in}] = \frac{g_m}{C_{gs}}L_s \]
  Narrowband.

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LNA Input Stage

\[ Z_{in} = s\left(L_s + L_g\right) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \approx \omega_T L_s \]

\[ G_{m,eff} = g_{m1} Q_{in} = \frac{g_{m1}}{\omega C_{gs} \left(R_s + \omega_T L_s\right)} \]

\[ = \frac{\omega_T}{\omega R_s \left(1 + \frac{\omega_T L_s}{R_s}\right)} = \frac{\omega_T}{2\omega R_s} \]

Note: \( G_{m,eff} \) is independent of \( g_{m1} \)!
Noise Factor

\[ F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \omega^2 C_{gs}^2 / g_m^2 \]

\[ F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left( \frac{\omega}{\omega_T} \right)^2 \]

- Reducing \( g_{d0} \), Increasing \( Q_{in} \) lowers F!
- Achieving low F involves linearity tradeoff.
- Technology Scaling is Key.
- Problem: The Free Lunch Principle

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Induced Gate Effects

- Gate Noise Current
- Real Component of $Z_g$

$V_{gs}$ $I_g$ $V_{ds}$
Equivalent Gate Circuit

\[ V_{gs} \quad i_g^2 \quad g_g \quad C_{gs} \quad -OR- \quad V_{gs} \quad \bar{v}_g^2 \quad r_g \quad C_{gs} \]

\[ \bar{i}_g^2 = 4kTB\delta g_g \quad g_g = \frac{1}{5} \frac{\omega^2 C_{gs}^2}{g_{d0}} \]

“Blue” Noise
- \( \delta \ (\sim 4/3) \) modified by hot electron effects
- \( \bar{i}_g^2 \) partially correlated with \( \bar{i}_d^2 \) (\( c = 0.395j \))
- \( \bar{i}_g^2 \) and \( g_g \) not modeled in HSPICE

“White” Noise

\[ \bar{v}_g^2 = 4kTB\delta r_g \quad r_g = \frac{1}{5g_{d0}} \]
Revised Noise Factor

\[ F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left( \frac{\omega}{\omega_T} \right)^2 \left\{ 1 + 2 \sqrt{\frac{\delta \alpha^2}{5 \gamma}} Q_L |c| + \frac{\delta \alpha^2}{5 \gamma} \left[ 1 + Q_L^2 \right] \right\} \]

(At Resonance)
Noise Factor Terms

\[ F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left( \frac{\omega}{\omega_T} \right)^2 \left\{ 1 + 2 \sqrt{\frac{\delta\alpha^2}{5\gamma}} Q_L |c| + \frac{\delta\alpha^2}{5\gamma} [1 + Q_L^2] \right\} \]

\[ Q_L = \frac{\omega (L_s + L_g)}{R_s} = \frac{1}{\omega R_s C_{gs}} \approx 2 \ast Q_{in} \]

Q of the Input Circuit

\[ \alpha = \frac{g_m}{g_{d0}} \leq 1 \]

Decreases with shorter channels

\[ c = \frac{i_g i_d^*}{\sqrt{i_g^2 i_d^2}} = 0.395 j \]

Gate / Drain Correlation Factor

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Minimum Noise Factor

Take $\frac{\partial F}{\partial W_{M1}} = 0$ to find the condition for minimum $F$: 

$$Q_{L,\text{opt}} = \sqrt{1 + \frac{5\gamma}{\delta\alpha^2}} \geq 1.87$$

Long Channel Values

$$F_{\text{min}} = 1 + \sqrt{\frac{4}{5}} \delta\gamma \left( \frac{\omega}{\omega_T} \right) \left| c \right| + \sqrt{1 + \frac{\delta\alpha^2}{5\gamma}} \geq 1 + 1.33 \left( \frac{\omega}{\omega_T} \right)$$

Note: Worst-Case $F_{\text{min}} = 4$ (6dB) when $g_m = g_g$. 

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Architecture / Noise Summary

- MOS Device has gate current noise in addition to drain current noise. \( \Rightarrow \) Optimum \( Z_s \) exists.

- Optimum \( Q_{in} \) relatively large. \( \Rightarrow \) Power savings and lower \( F \) by reducing \( W_{M1} \) for \( Q_{in} < Q_{opt} \).

- HSPICE models of MOS noise are inadequate.
  - Induced gate effects are not modeled at all.
  - Hot Electron effects influence the noise power spectral density of channel-related noise sources.
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Die Photo
S21

Marker 2

Peak S21 22dB

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S11

Marker 2

VSWR 1.38
S12

Marker 2

Null @ 1.5GHz

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Reverse Isolation

- Substrate tied to lowest inductance signal ground.
- Parasitic capacitances from spiral inductors and pads degrade reverse isolation.
- Simulation with parasitics shows null in S12 as seen in experimental data.
Noise Figure / S21 vs. Vdd

3.5dB NF / 22dB S21
Linearity - IP3

**Source Power (dBm)**

**Output Power (dBm)**

1dB Comp. = -22dBm (Input)

IP3 = -9.3dBm (Input)
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# Performance Summary

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<td>Noise Figure</td>
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<tr>
<td>S21</td>
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<tr>
<td>IP3 (Input)</td>
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<td>1dB Compression (Input)</td>
<td>-22dBm</td>
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<td>Supply Voltage</td>
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<td>Power Dissipation</td>
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<td>First Stage</td>
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<td>Technology</td>
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<tr>
<td>Die Area</td>
<td>0.12 mm²</td>
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</tbody>
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Conclusions

• CMOS is suitable for low noise above 1GHz.
• 3.5dB NF is lowest to date for CMOS above 1GHz.
• 1dB NF can be expected with current generation.
• Current CMOS noise models, as in HSPICE, are inadequate for accurate simulation of RF noise.
  • Significant noise contributors are absent from the models.
  • Short channel effects have not been properly accounted for.
  • More research is required.
Acknowledgments

Stanford Center for Integrated Systems

Air Force Office of Scientific Research

Howard Swain of Hewlett Packard

for many helpful discussions on CMOS noise