# Issues in High Frequency Noise Simulation for Deep Submicron MOSFETs

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**Abstract.** This paper proposes issues in highly accurate high frequency noise simulation for deep submicron MOSFETs. Unlike classical RF design, in which a given device with fixed characteristics is used, CMOS RF design permits selection of user specified device geometries as well as matching elements and bias conditions. Therefore, an exhaustive intrinsic noise modeling of MOSFETs across the entire operating condition is required. In order to capture the physics needed for accurate noise simulation of short-channel MOSFETs, a noise simulation tool needs the capability to exploit multi-dimensional device simulation in conjunction with process simulation. Further scaling of gate oxides introduces substantial gate leakage current due to the direct tunneling of electrons in the channel. It is expected that this current subsequently introduces shot noise current in the gate and the drain.

## INTRODUCTION

As CMOS continues to scale dramatically, it is now an attractive alternative to more exotic technologies for many RF applications in the low-GHz frequency range [1]. The combination of improved cutoff frequency and the promise of integrating whole systems on a single chip [2] are key motivators. In contrast to classical noise optimization techniques, recent developments in CMOS RF circuit [2] permit greater flexibility in selection of device geometries as well as matching elements and bias condition. Although accurate broadband noise modeling is indispensable for low noise design, the noise behavior in short channel MOSFETs is not well understood. This problem is particularly acute in state-of-art MOSFET technologies because of various second-order effects caused by process dependencies [3]. Further scaling of gate oxide thickness introduces substantial gate leakage current – so called the direct tunneling current. This leakage current changes not only the low frequency noise performance but also the high frequency modeling.

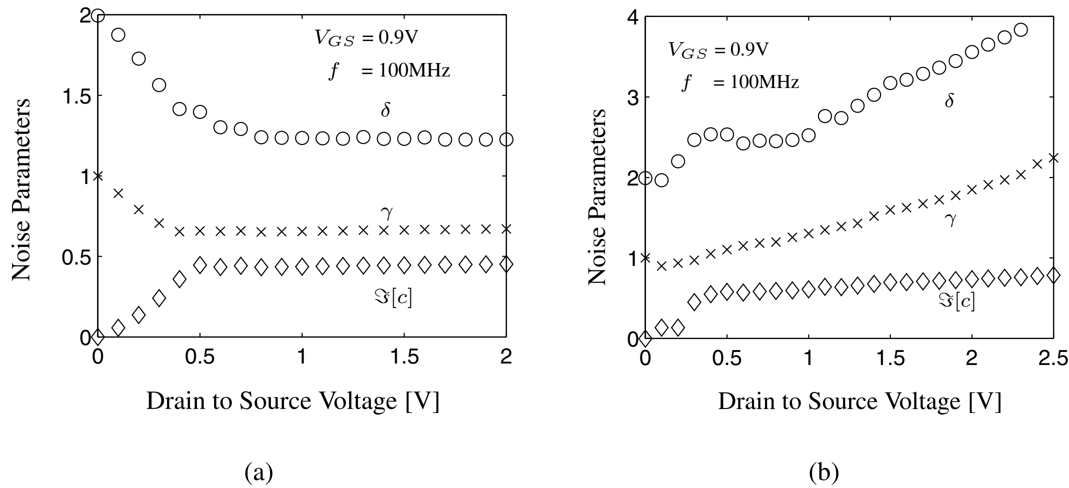


**FIGURE 1.** Drain bias evolution of three noise parameters ($\gamma$, $\delta$, and the imaginary part of $c$) comparing long channel characteristics with short channel. (a) 5 $\mu m$ nMOSFET. (b) 0.25 $\mu m$ nMOSFET.

# BIAS DEPENDENT INTRINSIC NOISE PERFORMANCE

In principle, one can obtain the minimum noise figure for a given device by using the optimum source impedance defined by the four noise parameters: $G_c$, $B_c$, $R_n$, and $G_u$. This classical approach has important shortcomings. For example, the source impedance that minimizes the noise figure generally differs, perhaps considerably, from that which maximizes power gain. Hence, it is possible for poor gain and a bad input match to accompany a good noise figure. Additionally, power consumption is an important consideration in many applications, but classical noise optimization simply ignores power consumption altogether. Finally, such an approach presumes that one is given a device with fixed characteristics, and thus offers no explicit guidance on how to best exercise the IC designer's freedom in tailoring device geometries [4].

Recently new noise figure optimization techniques for CMOS RF circuit have been proposed, permitting selection of device geometries to maximize noise performance for a specified gain or power dissipation [2]. Such approaches, however, have adopted assumptions regarding the intrinsic noise behavior of MOSFETs because detailed high-field behavior of noise was unknown at that time. In fact, the intrinsic noise behavior is the most critical information in noise figure optimization.

It has been known for quite some time that short-channel nMOSFETs in the saturation region exhibit considerably larger broadband RF noise than predicted by long channel theory [5]. This observation has led to speculation that poor, unacceptable noise performance might accompany scaling to smaller dimensions. The thermally noisy channel charge produces effects that are modeled by a drain and gate current noise generator [6]. These currents are partially correlated with each other because they share a common origin, and possess spectral densities given by the following equations:

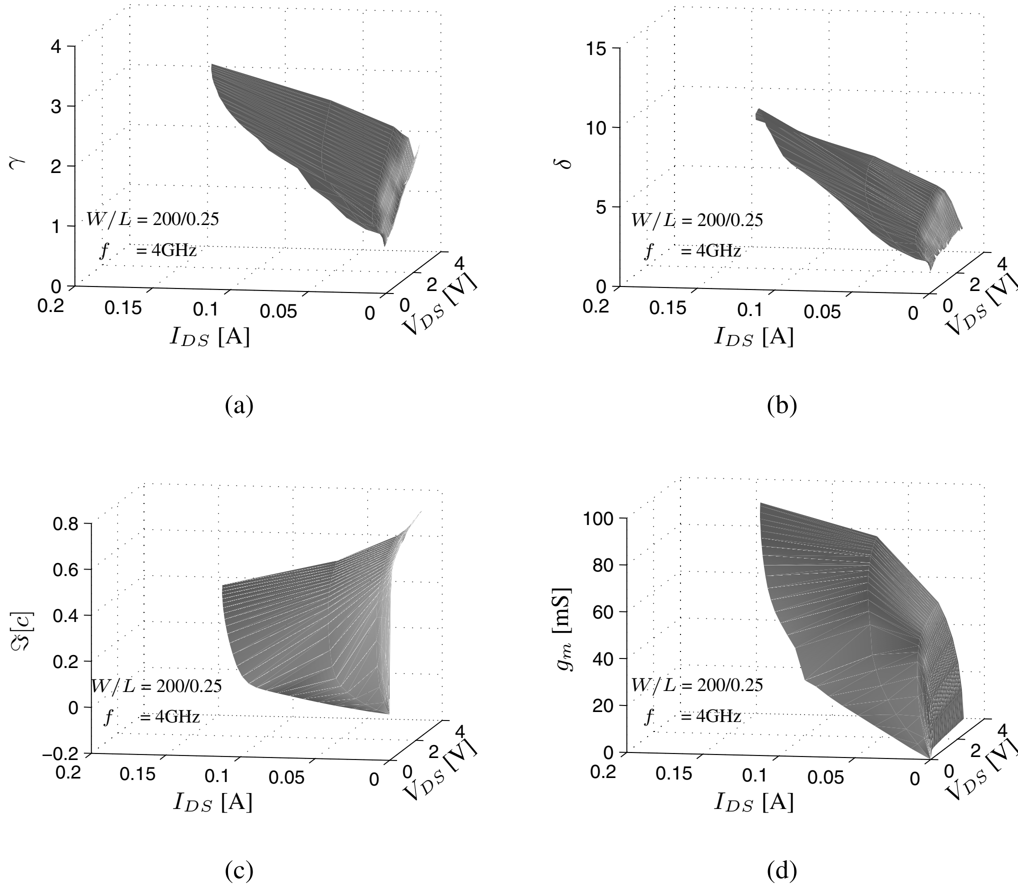


**FIGURE 2.** Intrinsic noise performance for the entire operating range of 0.25 $\mu m$ nMOSFET. (a) Drain noise parameter ($\gamma$). (b) Gate noise parameter ($\delta$). (c) Cross correlation between the drain and the gate noise (the imaginary part of $c$). (d) Transconductance ($g_m$).

$$S_{i_d} \triangleq 4\,k\,T\,\gamma\,g_{d0} \tag{1}$$

$$S_{i_g} \triangleq 4\,k\,T\,\delta\,g_g \tag{2}$$

$$c \triangleq \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \tag{3}$$

where $g_{d0}$ is the drain output conductance under zero drain bias and $g_g$ is the real part of input admittance. For long-channel MOSFETs, values for $\gamma$, $\delta$, and $c$ in saturation are 2/3, 4/3, and $j0.395$, respectively [2]. However, in short-channel MOSFETs, as the longitudinal field strength grows, carrier velocities begin to saturate, and further increases in the electric field cause carrier heating and increases in $\gamma$ and $\delta$.

To incorporate such carrier heating in short-channel MOSFETs, higher order moments such as captured by the Hydrodynamic (HD) formulation are needed in contrast to first order transport models such as that of Drift-Diffusion. Figure 1 shows HD simulation

results which illustrate increases in $\gamma$, $\delta$, and $c$ for a short-channel MOSFET (0.25 $\mu m$) in comparison to the long-channel case (5 $\mu m$). A mixed approach that combines a 1D active transmission line model with a 2D HD device simulation, which provides the Langevin stochastic source term as well as the local ac model parameters, was used in the simulation [3]. According to a recent study, the two-dimensional HD model combined with the Impedance Field Method (IFM) shows promise in capturing the physics needed for accurate noise simulation of short-channel MOSFETs down to 0.25 $\mu m$ [3]. However the extendability of the IFM for ultra-short channel devices beyond 0.1 $\mu m$ is a question so far.

State-of-art MOSFET technologies involve various second-order effects caused by complex processing such as new drain structures, gate overlap effects, nonuniform doping profiles in the substrate, etc. Future MOSFET technology is likely adopt still more advanced processing and materials, for example SiGe [7] and SiC [8]. Therefore, the capability to exploit multi-dimensional device simulation in conjunction with process simulation is an attractive alternative for extraction these physical dependencies of noise.

To utilize these new degrees of freedom in new noise figure optimization, an intrinsic noise modeling of MOSFET must be exhaustive across the range of fabrication and operating conditions. Providing detailed information on small signal parameters including second order parts in a distributed network is necessary as well. Figure 2 shows simulated intrinsic noise characteristics as a function of bias and current for the entire operating conditions of a 0.25 $\mu m$ MOSFET.

## DIRECT TUNNELING CURRENT

Traditionally, the gate oxide of a MOSFET has been considered as a perfect barrier for carriers allowing no current flow between the gate and silicon. In fact, there is tun-

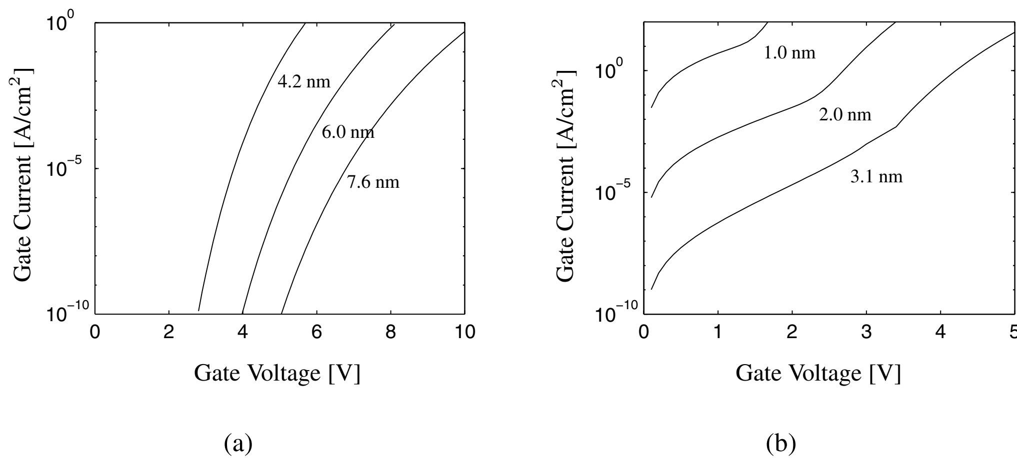


**FIGURE 3.** Gate oxide tunneling current in MOSFETs. (a) Fowler-Nordheim Tunneling current. (b) Direct Tunneling current.

neling of electrons from the vicinity of the electrode Fermi level through the forbidden energy gap into the conduction band of the oxide. Such a phenomenon is called Fowler-Nordheim Tunneling [9] and its current density can be expressed as

$$J = \frac{q^3 E^2}{8\pi h \Phi} \ \exp\left[ -\frac{4(2m)^{1/2}\Phi^{3/2}}{3\hbar q E} \right] \tag{4}$$

where $h$ is Planck's constant, $q$ is the electronic charge, $E$ is the electric field in the gate oxide, and $m$ is the free electron mass. The perfect barrier assumption has been valid in most practical situations because the Fowler-Nordheim Tunneling current has been negligibly small as shown in Figure 3 (a).

As demonstrated in Figure 3 (b), however, ultra-thin oxides below 4 nm exhibit drastic increase of leakage current, so called direct tunneling current [10]. In this regime, the gate oxide capacitor would introduce an extra noise current source, possibly a shot noise current source, besides two classical noise sources: drain and gate current noise. Fortunately, the $IR$ drop along the gate polysilicon due to the leakage current is negligible; also, the additional conductances ($1/r_{gs}$ and $1/r_{gd}$ in Figure 4) associated with this tunneling across the gate oxide are small compared with $\omega C_{gs}$ and $\omega C_{gd}$ in the range above the $1/f$ corner frequency, which is usually few MHz in MOSFETs.

By contrast, the impact of the direct tunneling current on high frequency noise performance is becoming critical. The gate shot noise current generated in each segment of the MOSFET flows along the channel and subsequently creates drain shot noise current as well, because it is uncorrelated with the origins of the drain and gate current noise [11]. Since the direct tunneling current can be substantial, the drain shot noise becomes comparable to the drain current noise in MOSFETs with oxides below 2 nm. While a rigorous modeling of the direct tunneling current is prerequisite to accounting

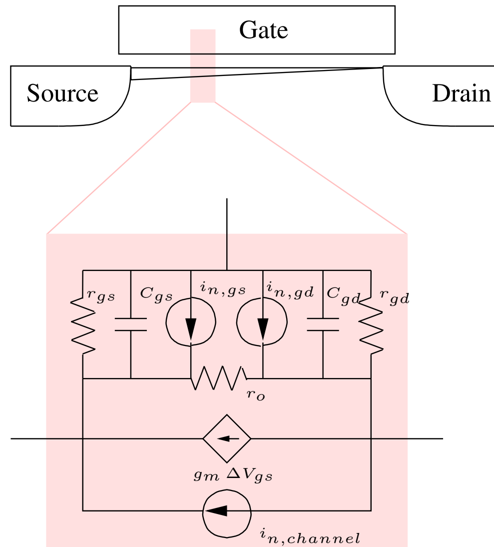


**FIGURE 4.** Local small-signal equivalent circuit for a segment of MOSFET in which the direct tunneling current is significant.

for this effect, accurate modeling of tunneling in MOSFETs involves evaluation of the multi-dimensional Schrödinger equation – an unsolved problem to date.

## CONCLUSIONS AND OPEN QUESTIONS

Noise figure optimization techniques for CMOS RF circuit now permit selection of device geometries to maximize noise performance for a specified gain or power dissipation. Unfortunately, exhaustive intrinsic noise modeling of MOSFETs for the entire operating condition is required. In order to capture the physics needed for accurate noise simulation of short-channel MOSFETs, which involves various second-order effects caused by complex processing, new noise simulation tools are needed with capabilities to exploit multi-dimensional device simulation in conjunction with process simulation. The extendability of the IFM for ultra-short channel devices beyond 0.1 $\mu m$ is open to question. Ultra-thin oxides below 4 nm exhibit a dramatic increase in leakage current due to the direct tunneling. This current introduces gate shot noise current which subsequently creates drain shot noise current. Accurate modeling of these effects must also reflect multi-dimensional Schrödinger equation analysis which is unsolved to date.

## ACKNOWLEDGMENTS

This study was supported by SRC under contract 98-SJ-116. The authors would like to thank Dr. Marek Mierzwinski of HP EEsof for promoting and mentoring this project.

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