A CMOS Multi-Gb/s 4-PAM Serial Link Transceiver*

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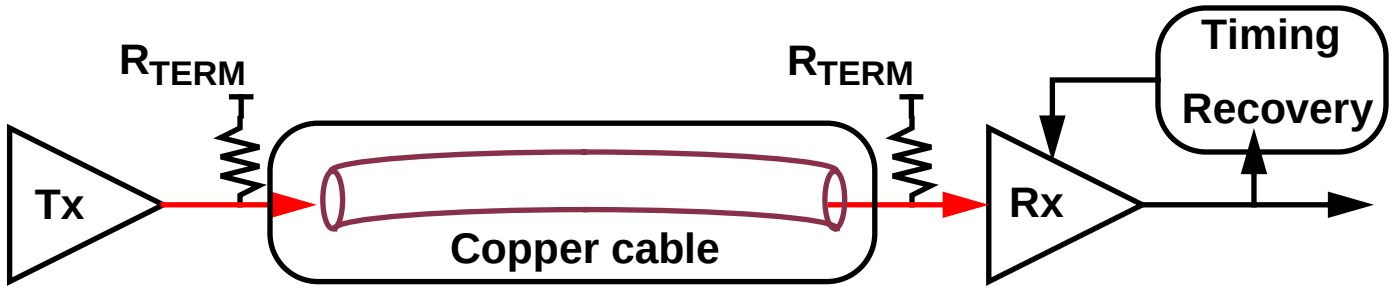
Goals



- Networking high-speed (5 -10Gbps) systems for ranges up to 10 meters at lower cost and complexity
  - → Parallel buses are costly for long distances.
  - → Optical fibers are not beneficial for such small ranges.
  - → Serial links on copper cables are an attractive solution for this kind of application.
- Push bandwidth limitations of CMOS serial links
  - → CMOS technology is getting cheaper, faster, and more available.
  - → Integrate more digital functions on-chip.

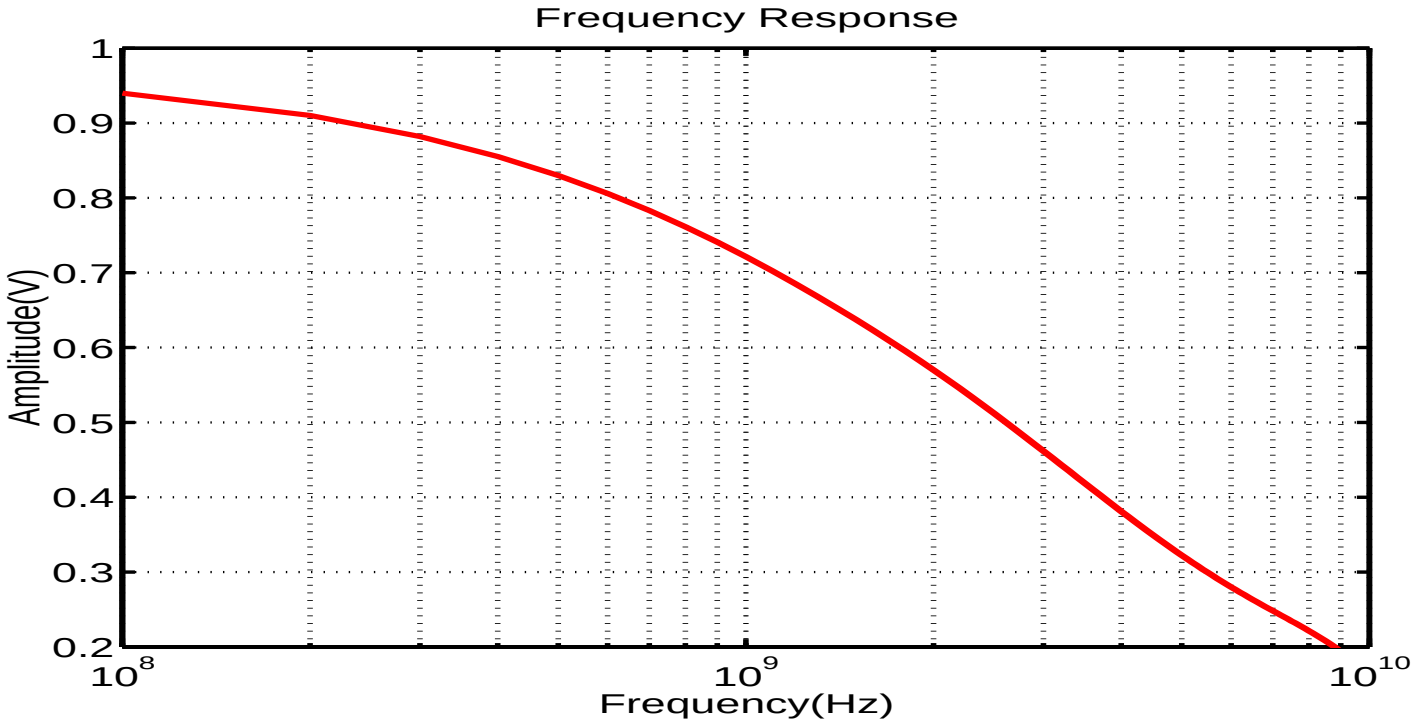
Outline

- ✔ *Challenges*
- ❑ System Architecture
- ❑ Circuit Implementation
- ❑ Test Results
- ❑ Conclusion

Challenges: Interconnection Bandwidth

- Frequency-dependent attenuation in electrical links due to skin effect resistance and dielectric loss.

  → The -3dB BW of 10-meter PE-142 coax is ~1.0GHz.



Challenges: Interconnection Bandwidth

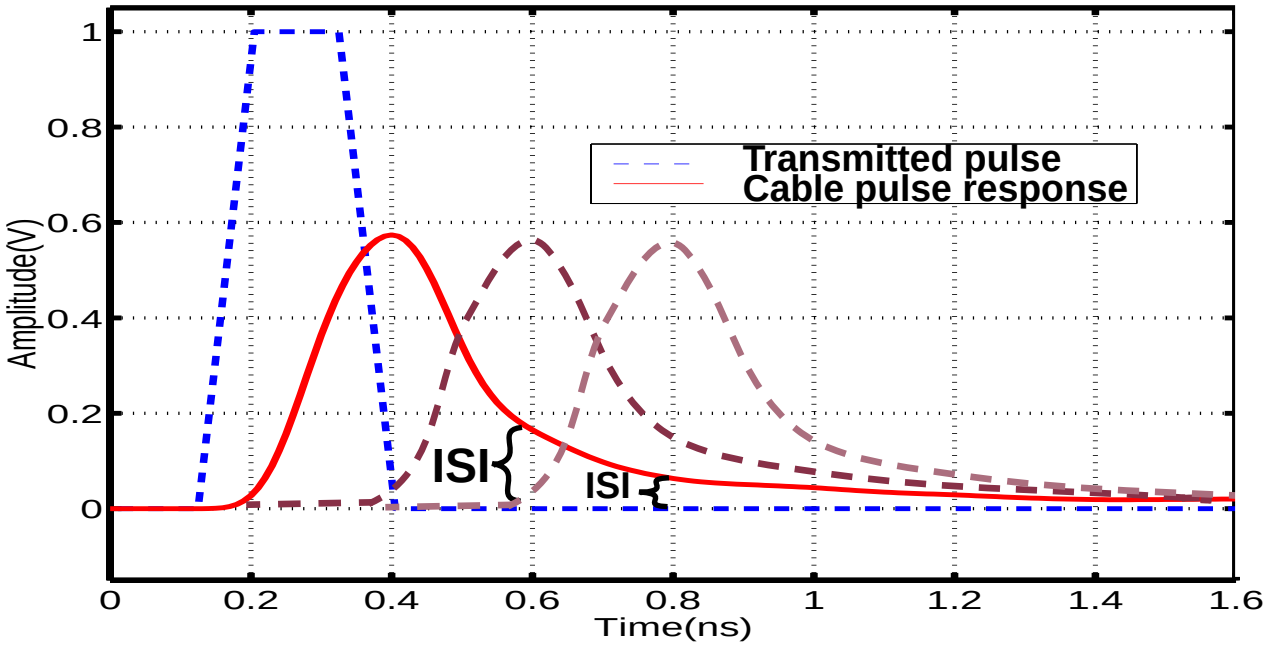
- Frequency-dependent attenuation causes ISI.

  → Only channel eigen-waveforms result in no ISI.

  → Generation and detection of true eigen-waveforms is not feasible due to circuit limitations at high frequencies.

  → Trapezoidal pulses are instead used as basis waveforms.

  → Higher symbol rate results in more ISI.

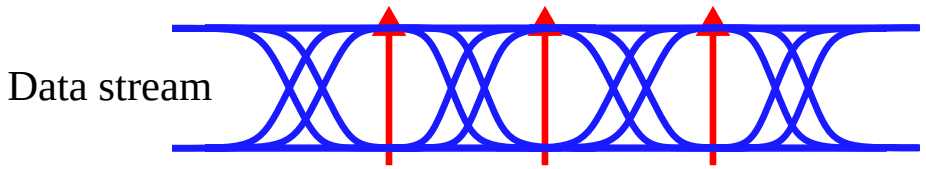


Challenges: Data Generation/Detection

- Hard to operate CMOS circuits at directly multi-GHz speeds

  → Better to reduce the on-chip frequency

- Recovering embedded timing information from the serial data



  → Large frequency variations of on-chip oscillators and small frequency capture range of phase detectors

- Data detection at high speeds

  → Input voltage offset, cross-talk, and signal reflection (reflection ISI) limits the minimum detectable signal.

Outline

- ❑ **Challenges**
- ✔ ***System Architecture***
- ❑ **Circuit Implementation**
- ❑ **Test Results**
- ❑ **Conclusion**

Reduction of On-Chip Frequency

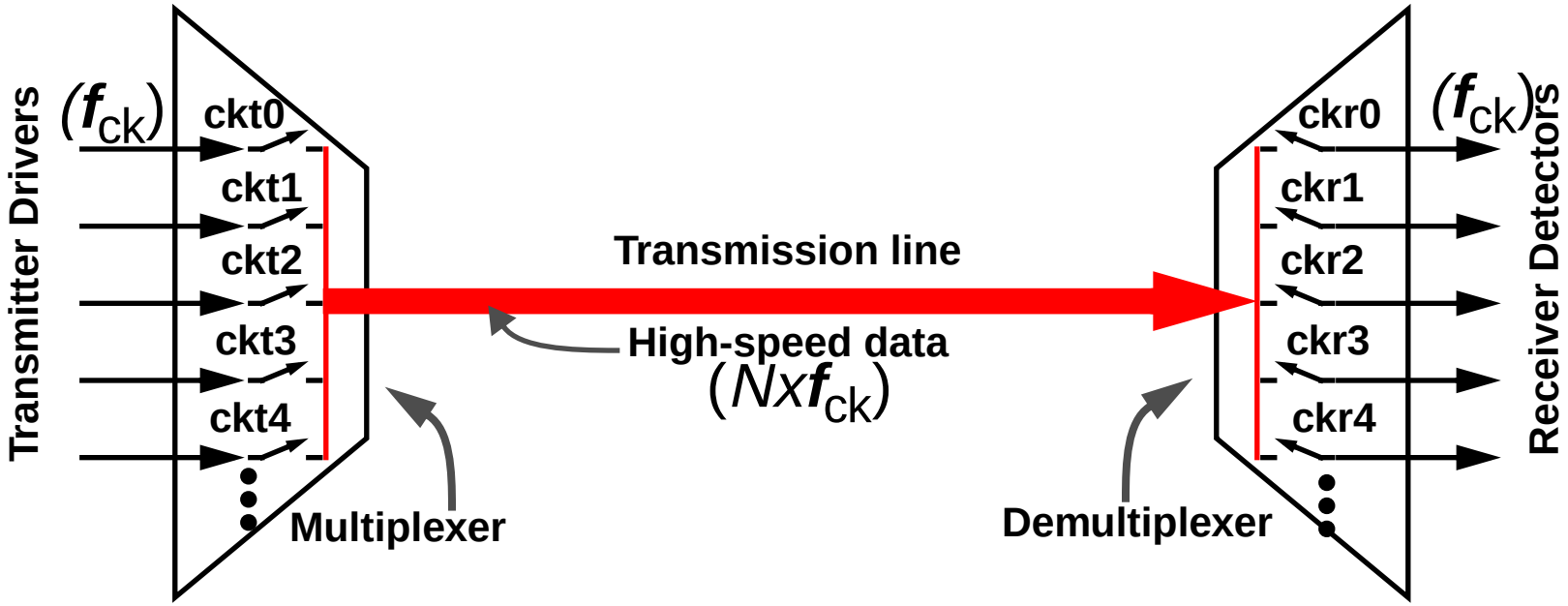
- Multiplexing (*N*:1) and demultiplexing (1:*N*) the high-speed data at the transmission line*

  → Reduces the on-chip frequency by a factor of *N*

  For example: $N = 5$ => (for 5Gsym/s) $f_{ck} = \frac{5G}{5}$ = 1GHz

  → Max switching speed of the process is the limit

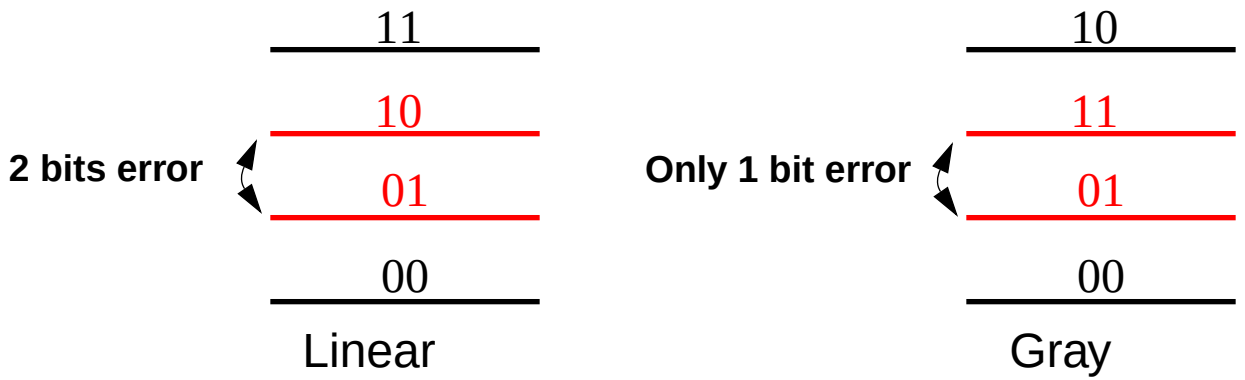
  CMOS provides high-speed transistor switches



*C-K. Yang, R. Farjad, M. Horowitz, VLSI Symp. 97

Proposed Modulation

- 4-PAM is used for data communication in the serial link
  - → Symbol rate reduces to half that of binary transmission.
  - → Lower symbol rate reduces ISI and on-chip clock frequency.
  - → Higher level PAM was not used because of:
    limited transmitter swing, minimum detectable signal
    and reflection ISI.
- 4Sym-->5Sym conversion guarantees clock recovery
- Gray code mapping of levels reduces BER by 25% vs. linear mapping



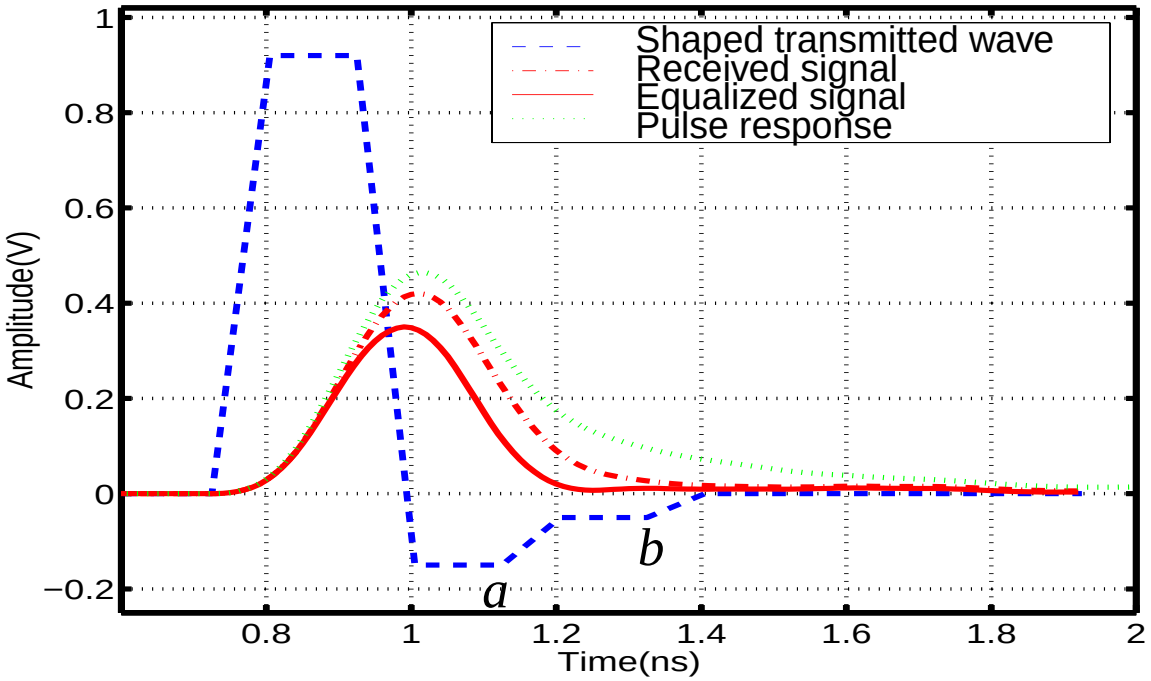
Proposed Architecture to Combat ISI

- To cancel the long tail of pulse response, a pre-emphasis symbol-spaced 2-tap FIR filter is implemented at the transmitter:

$$Vo(n) = Vi(n) - a \bullet Vi(n-1) - b \bullet Vi(n-2)$$

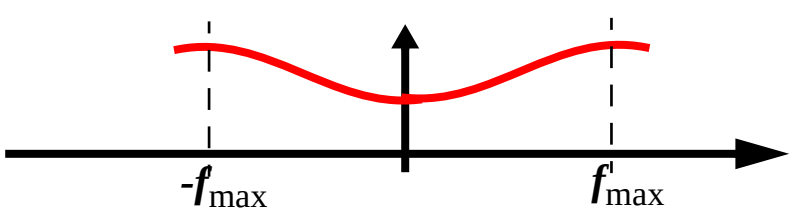
- To sharpen the signal transition edges, a half-symbol-spaced 1-tap high-pass equalizer is implemented at the receiver

$$Veq(n) = Vi(n) - \alpha \bullet Vi\left(n - \frac{1}{2}\right)$$



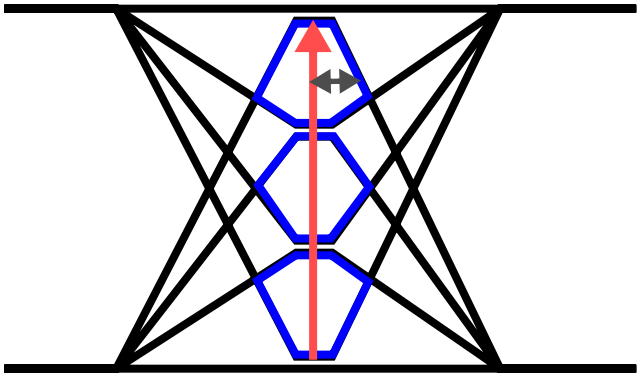
Receiver Equalizer

- The half-symbol-spaced filter boosts frequency components up to $f = \frac{1}{Ts}$

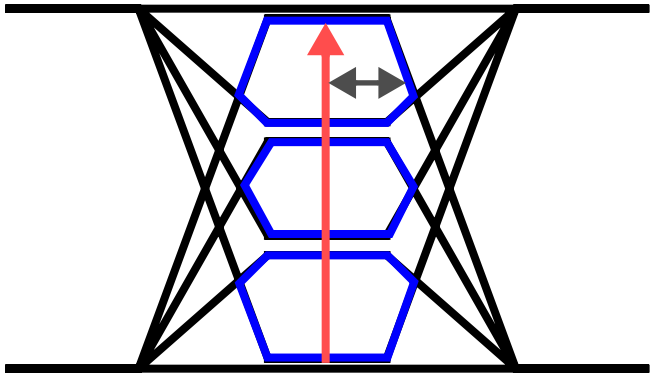


R=5Gsym/s
T_s=200ps
f_{max}=5GHz

- Sharpening the transitions increases the eye opening width.
  =>Less sensitive to sampling phase errors.



Slow transition



Sharp transition

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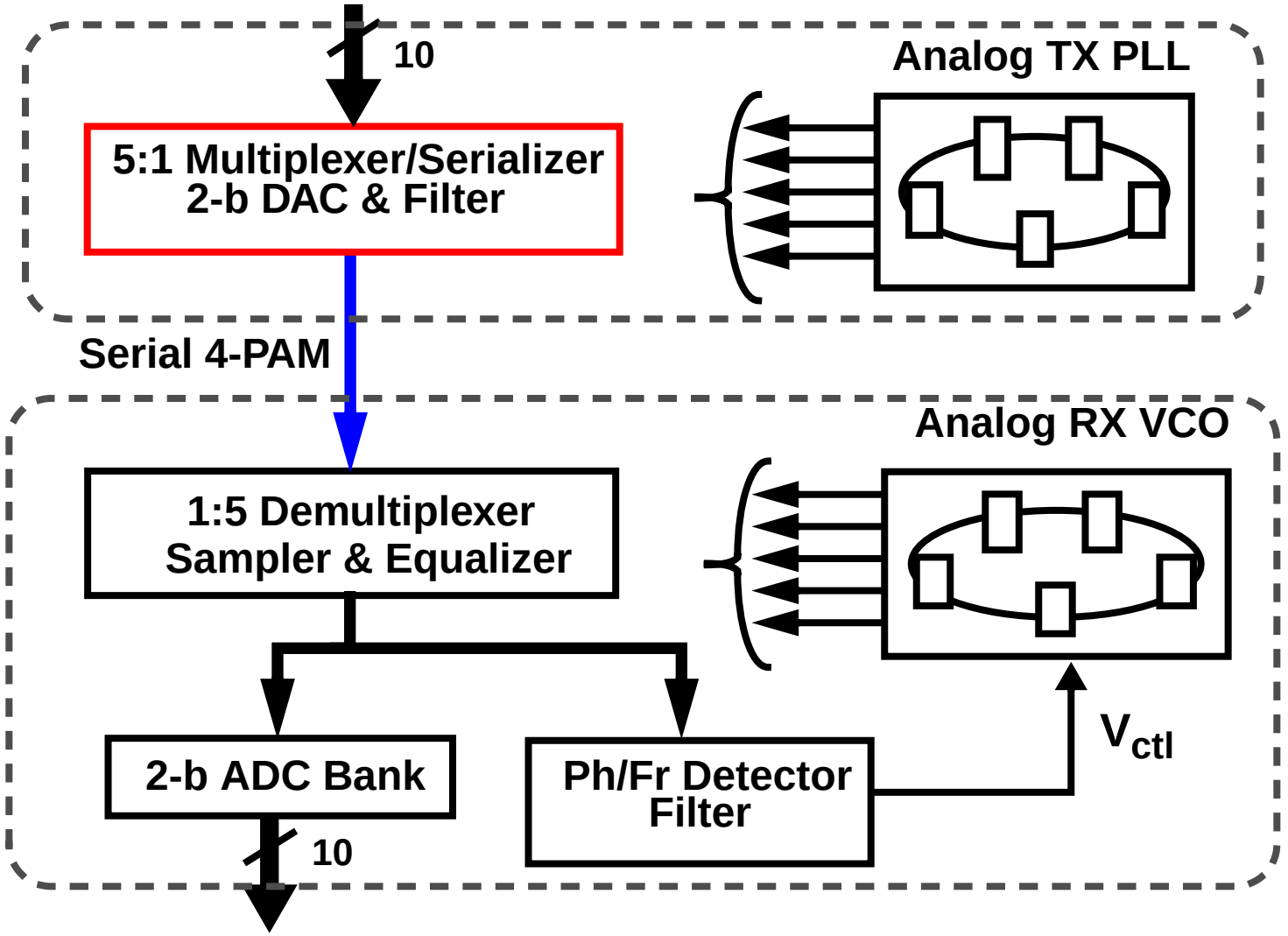
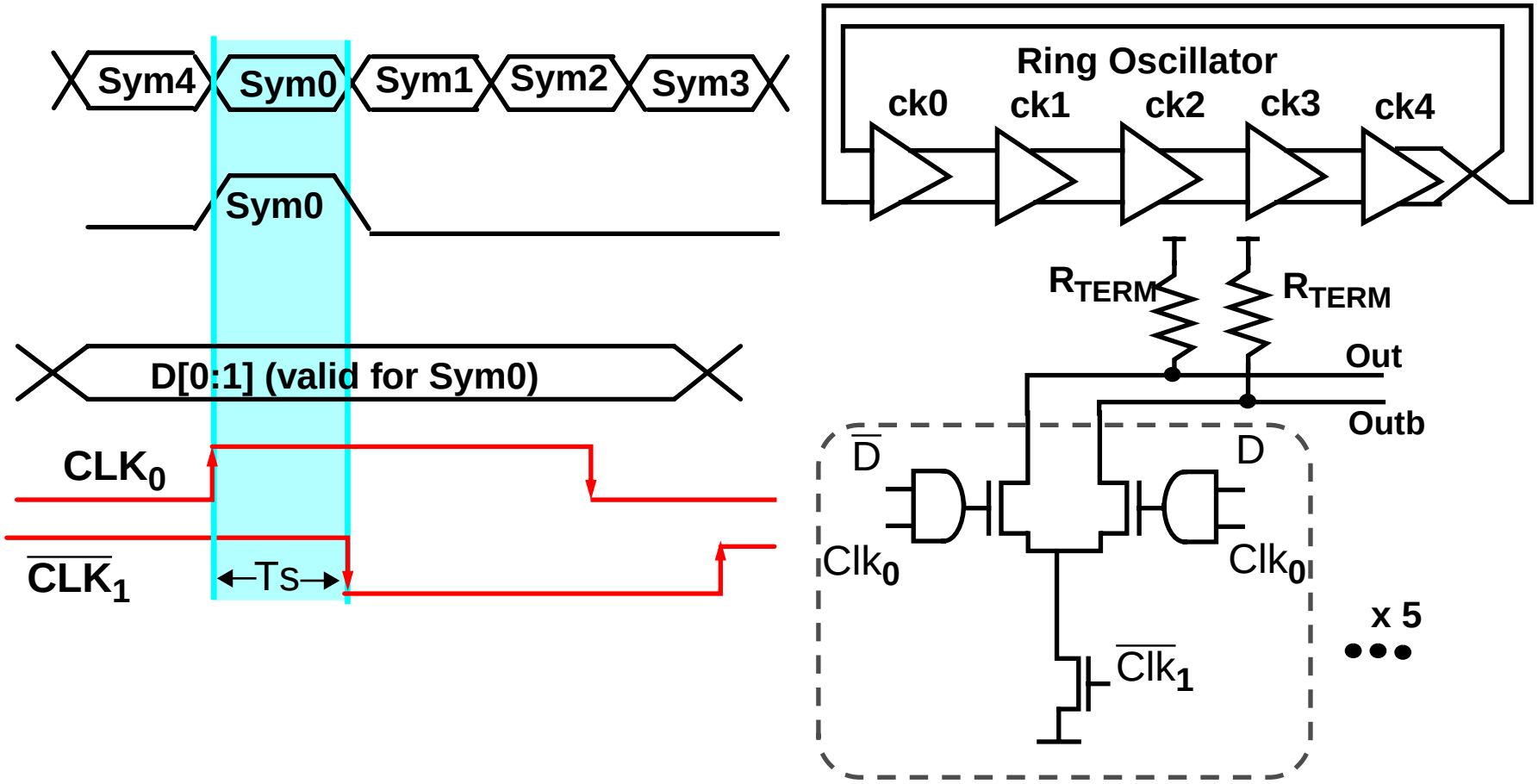
Top Level Architecture

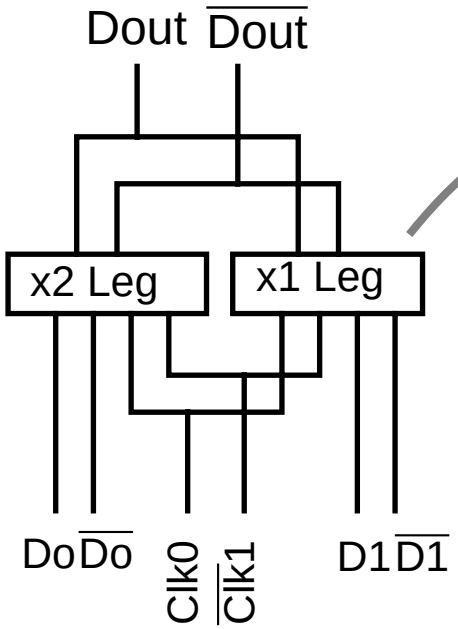


5:1 Multiplexing Transmitter

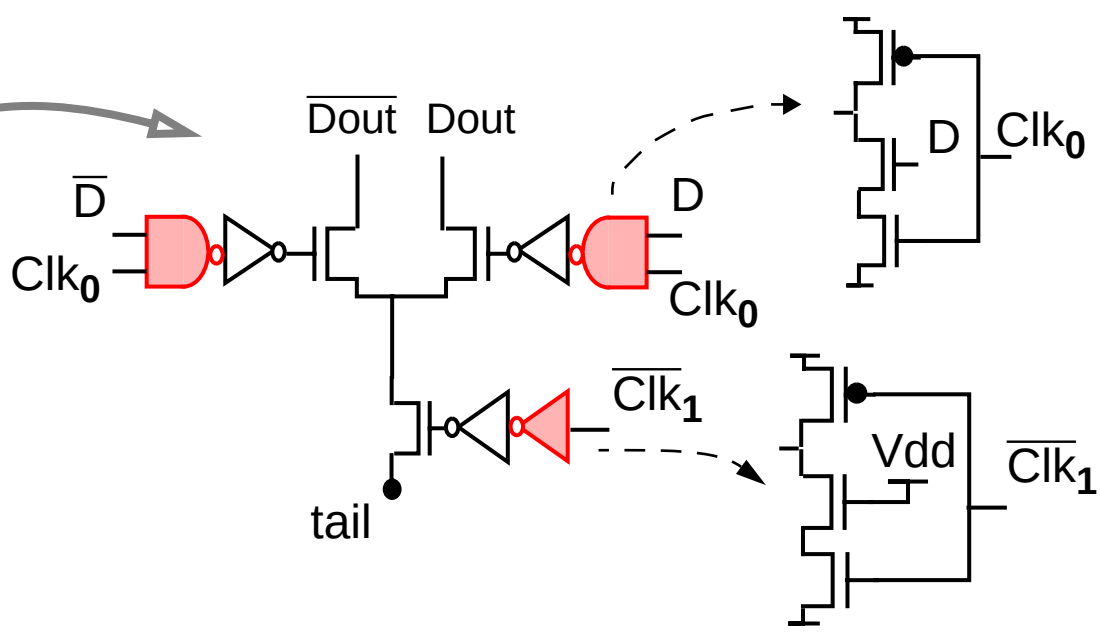


- Each symbol is generated by the rising and falling egdes of two phases of clock

2-bit Output Driver

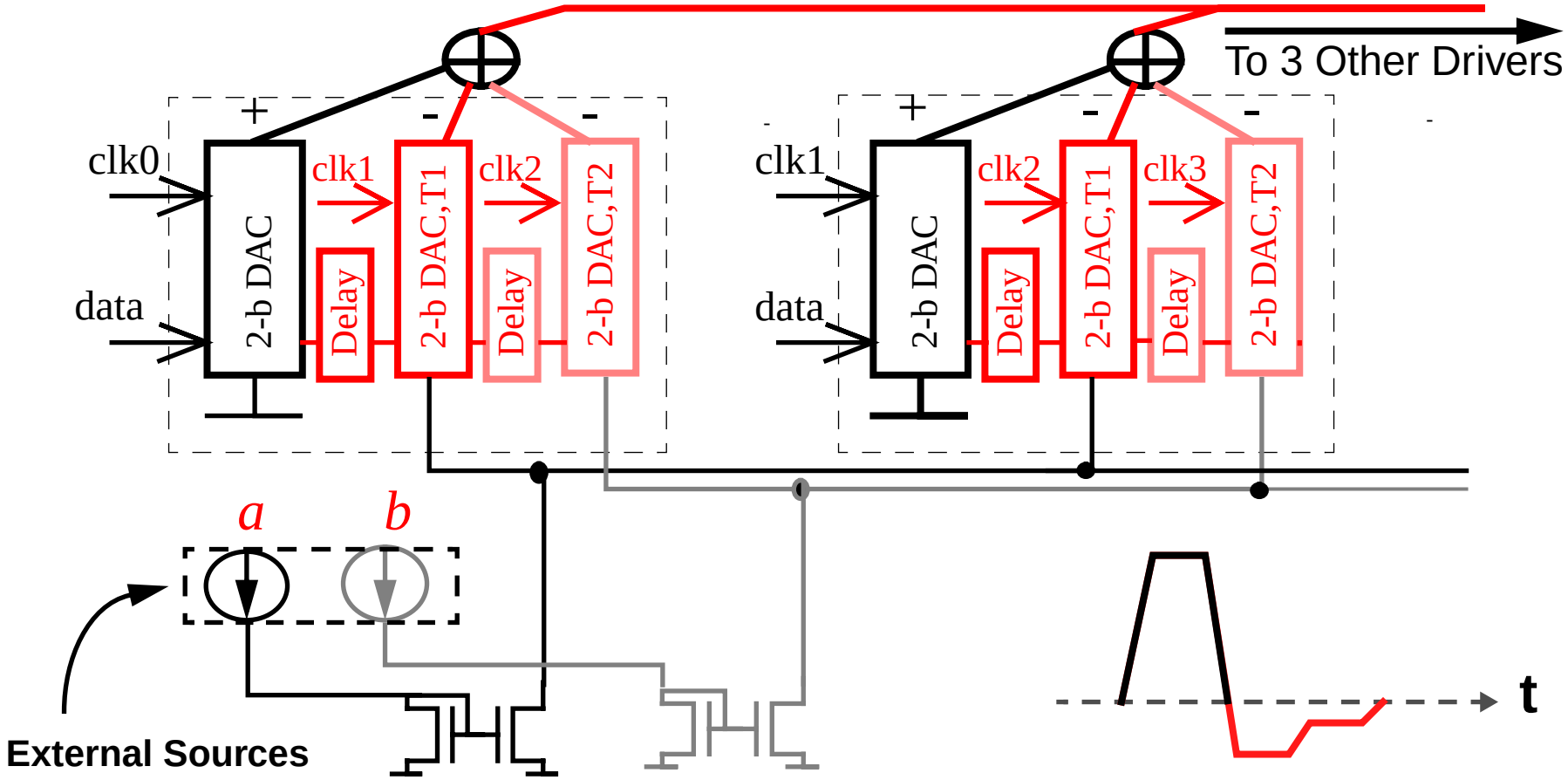


2-bit DAC module



Differential drive leg

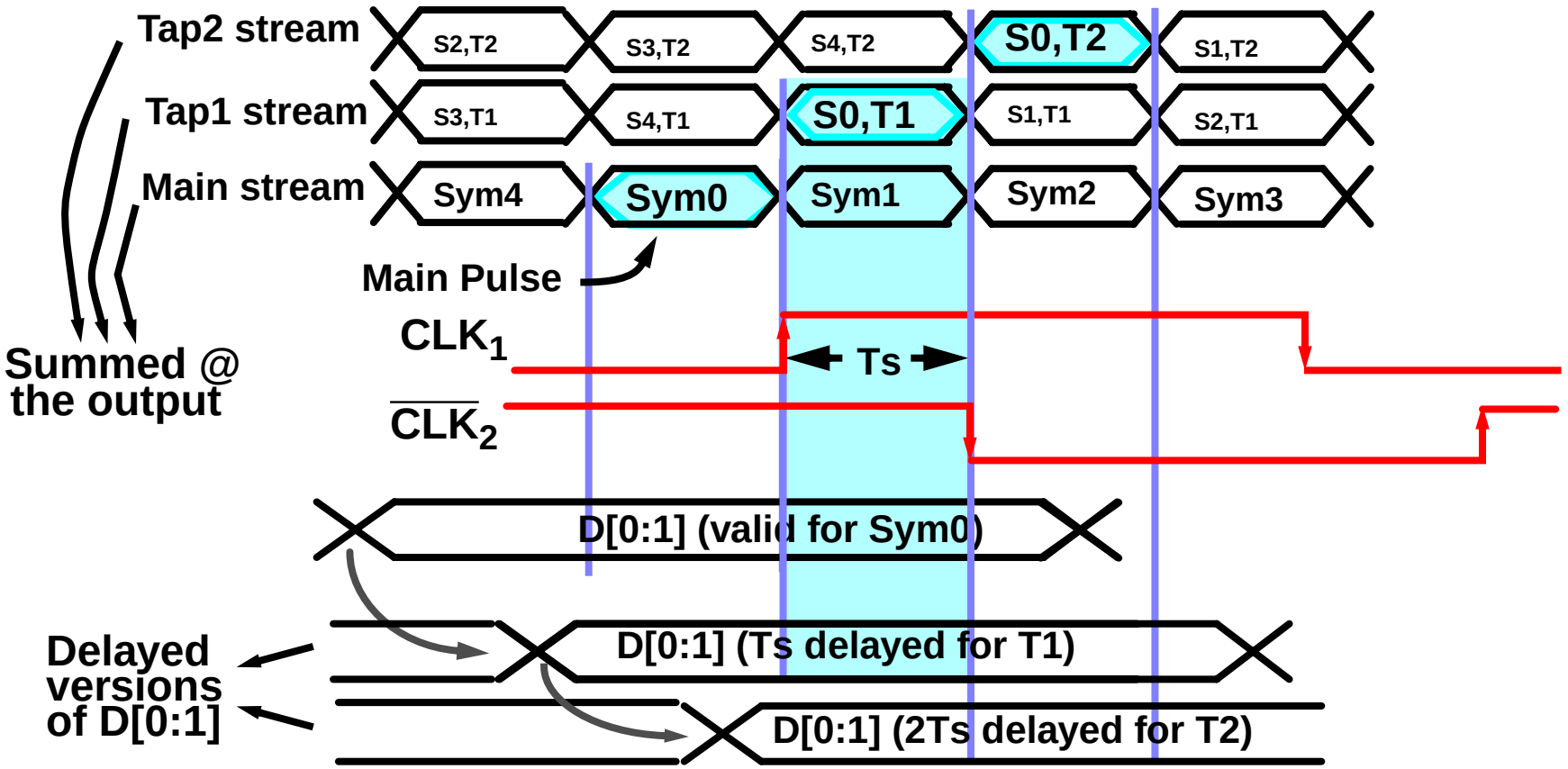
4-PAM Preshaping 5:1 Multiplexer



Multiplexer Drivers & 2-Tap Filters

- Each driver generates a filtered symbol independent of other drivers.
- Simple architecture to implement the filter.

Symbol Generation

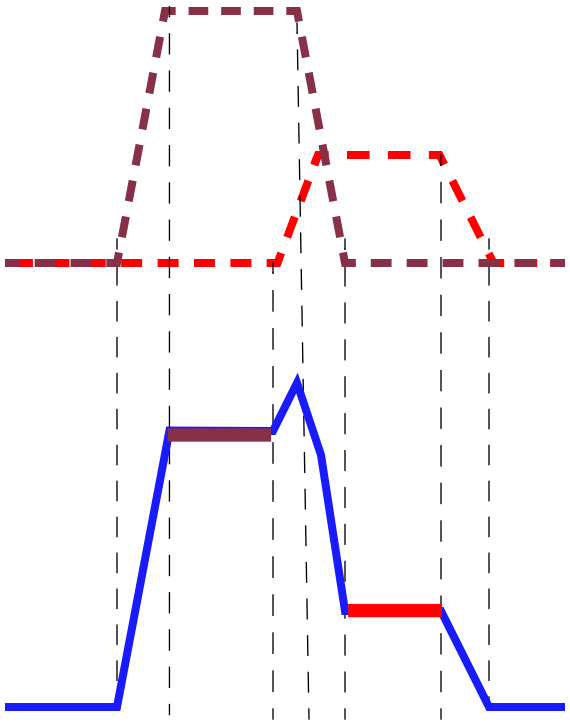


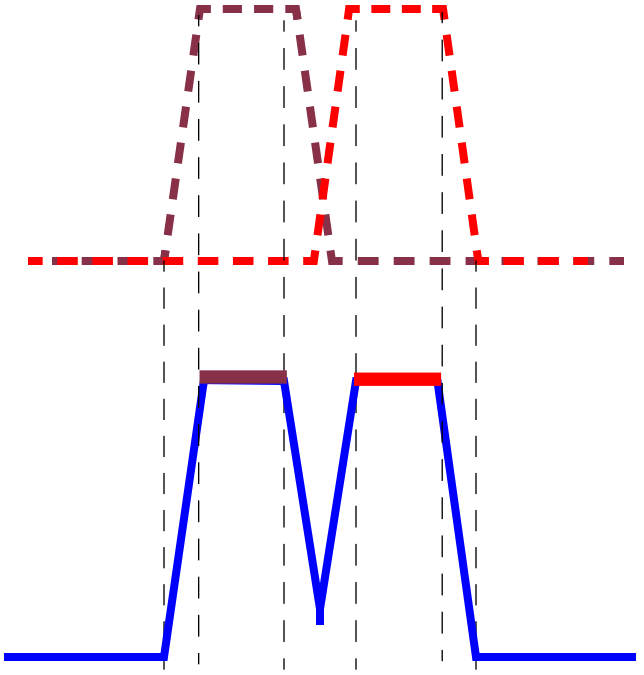
Tap-Drivers timing

Symbol-Width Problem

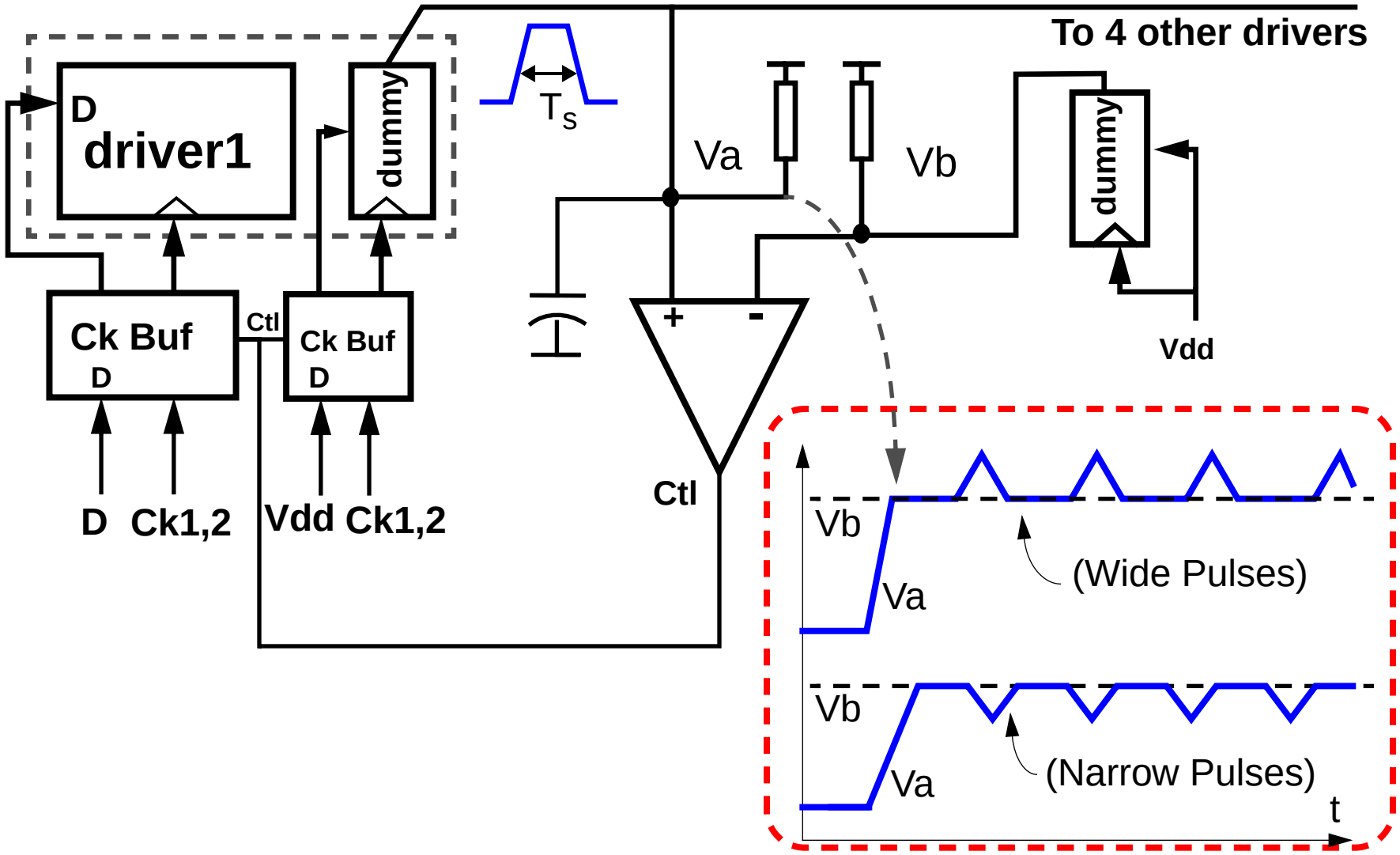
- Variations in PMOS to NMOS strength ratio result in duty cycle error in the clocks (unbalanced falling & rising times)

→ The effective width of the final output symbol decreases.

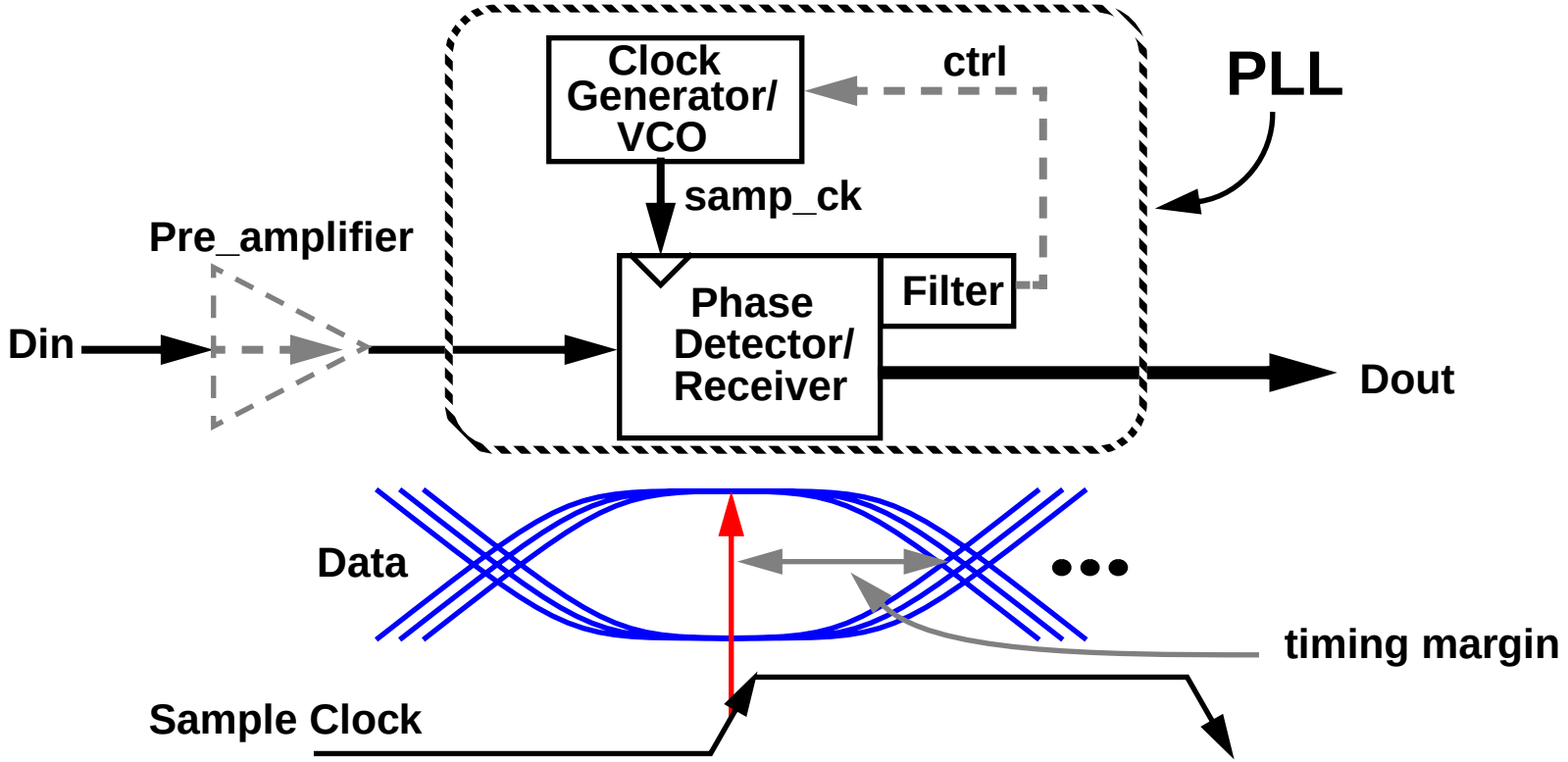




Pulse-Width Control Loop

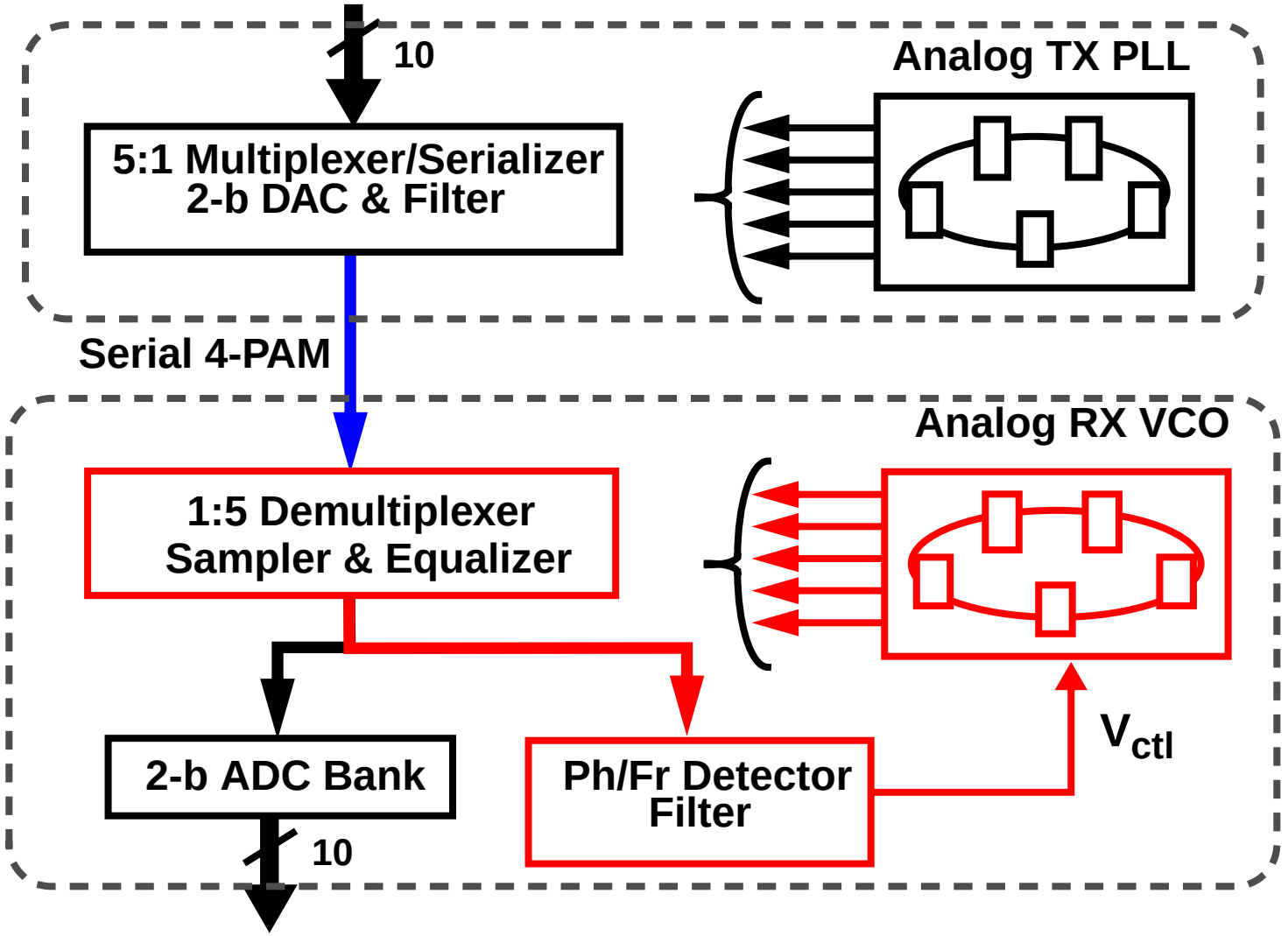


Receiver Timing Recovery

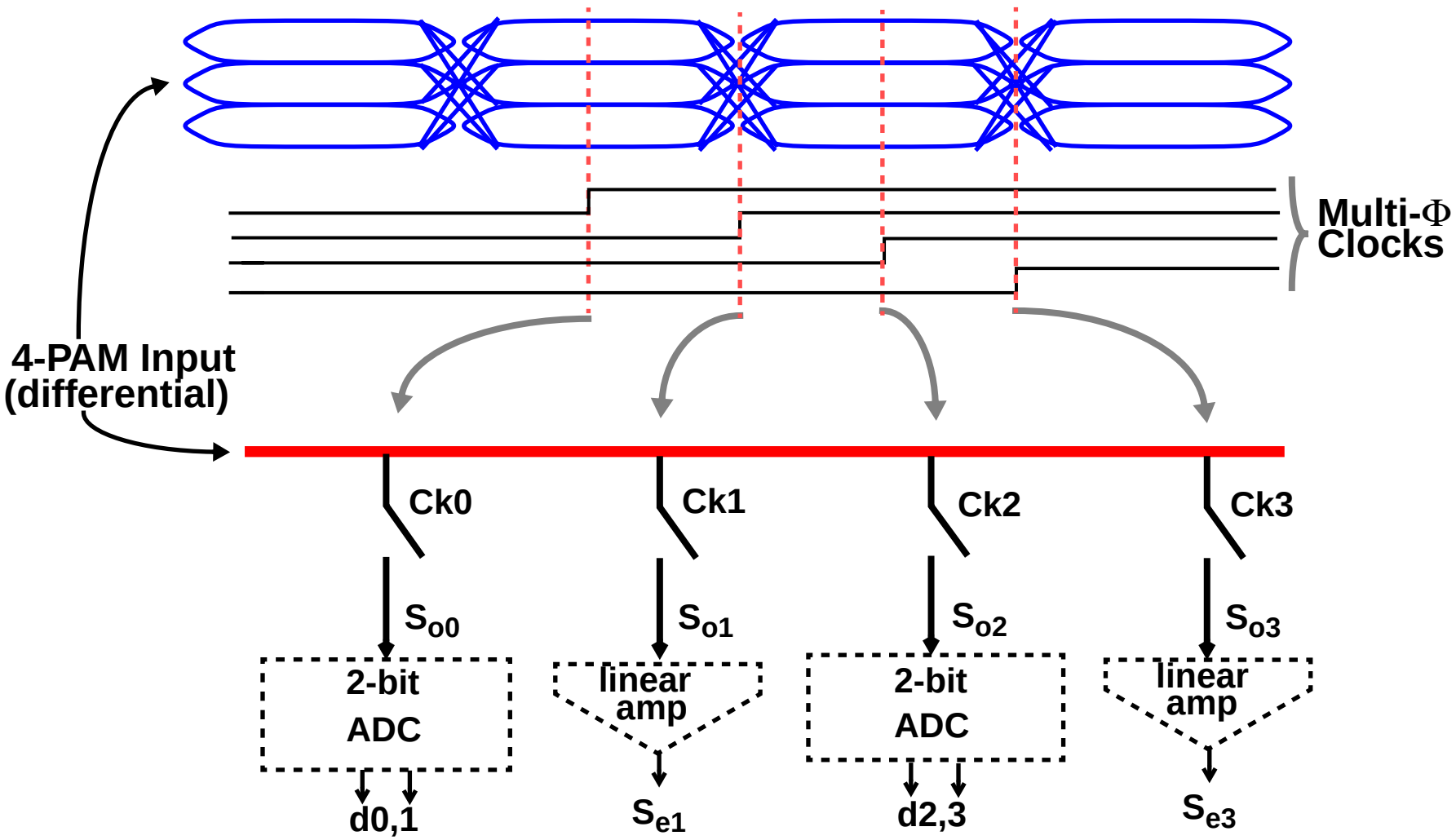


- Oversampling phase detection
  - → Many input samplers, Phase quantization error, Complex logic.
- Tracking phase detection
  - → Conventional bang-bang control: Low loop bandwidth and capture range
  - → Proportional control: Desirable

Top Level Architecture

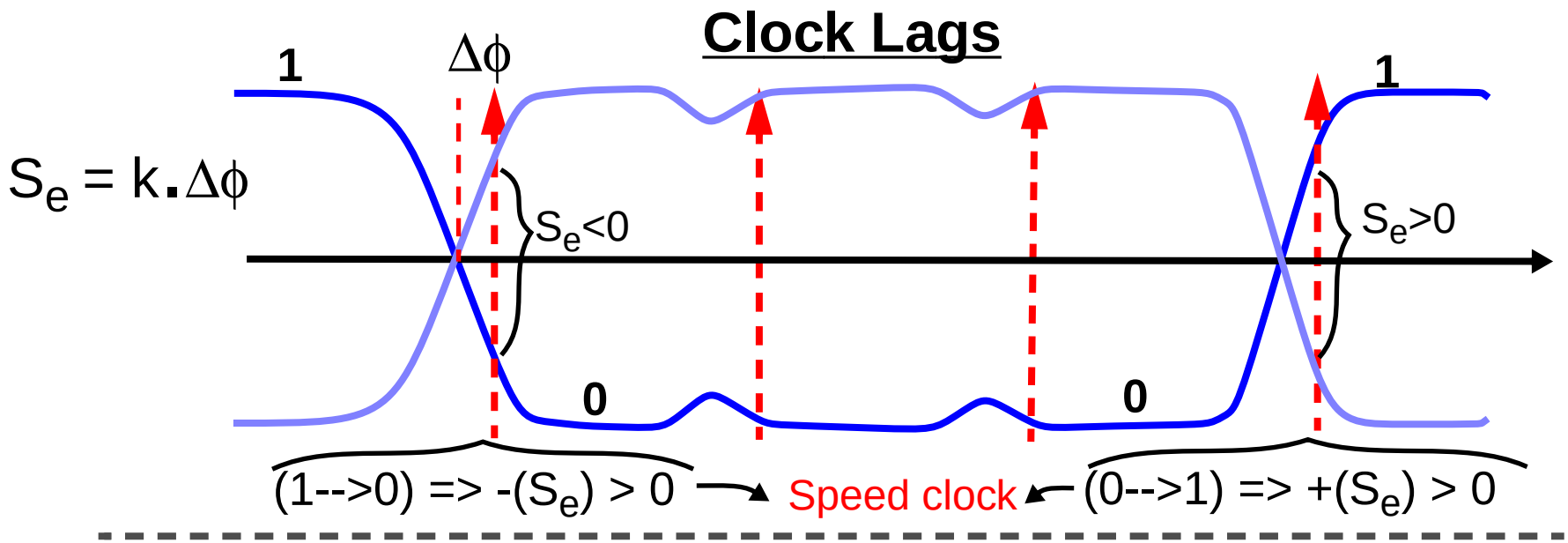


Timing Recovery: Front-end



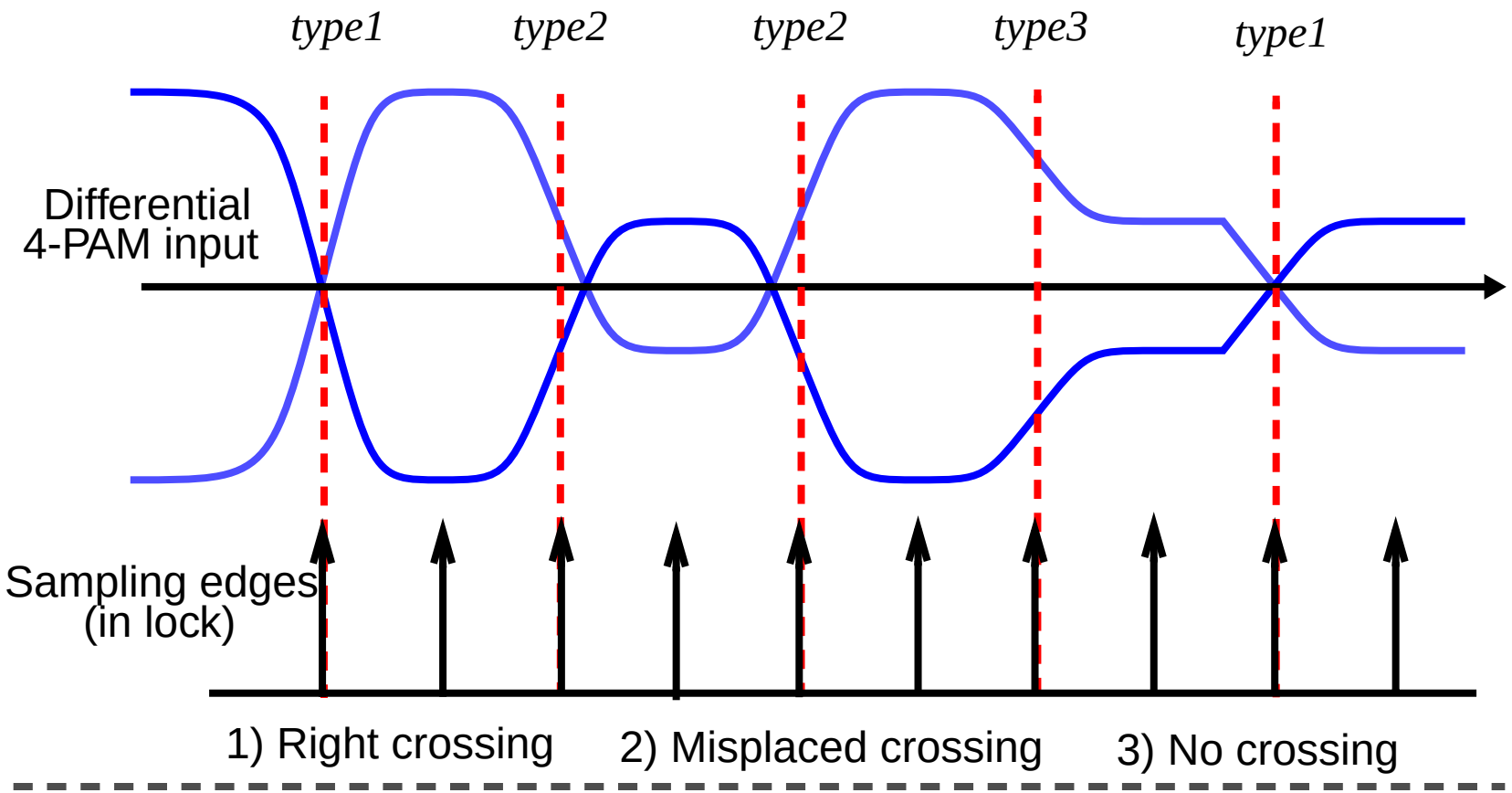
Simplified receiver front-end (x2 oversampling)

Proposed Proportional Phase Detection



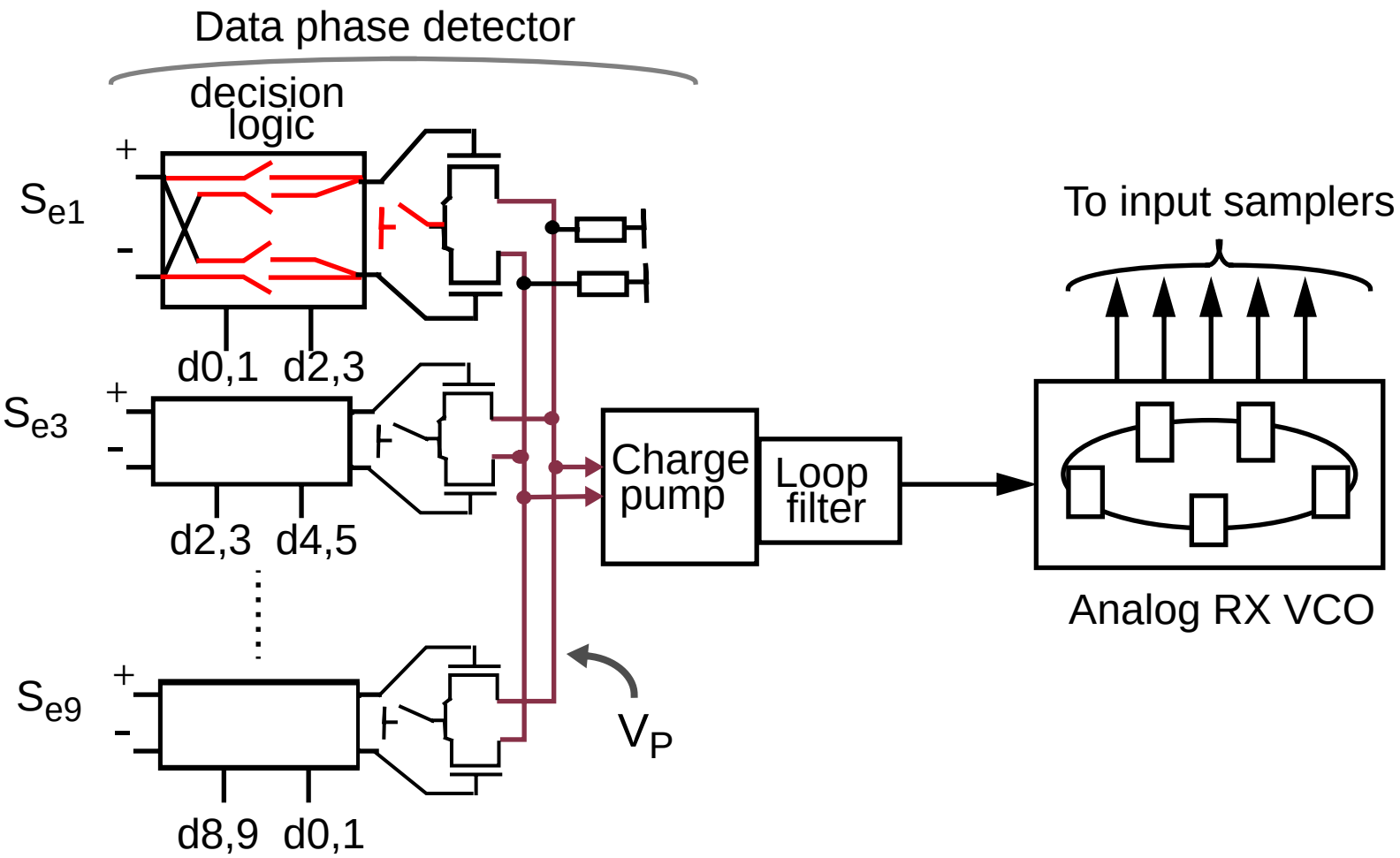
- Advantages:
  - → Larger PLL bandwidth and stability compared to bang-bang PLLs.
  - → Zero systematic phase offset (same detection mechanism for edges and data).
  - → Zero ripple on control voltage of PLL (unlike bang-bang).
- Disadvantage:
  - → Voltage offsets of edge samplers translate into phase error.

Three 4-PAM Transitions



- Only ***type1*** transitions are used for clock recovery
- Transitions ***type2*** and ***type3*** are ignored by a decision logic

Data Phase Detector



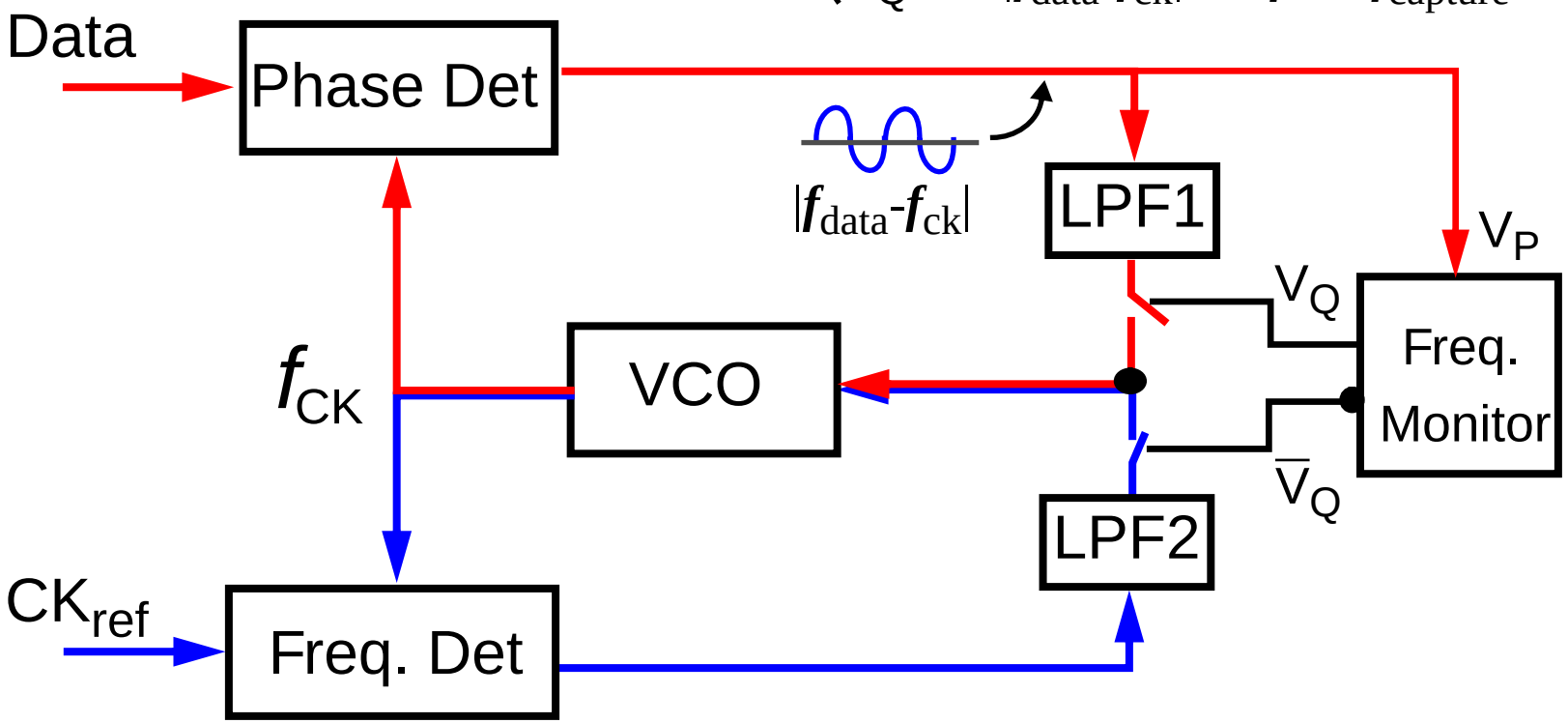
- Edge sample values, S_e, of *type1* are summed with correct polarity at phase detector output (V_P)

Frequency Acquisition

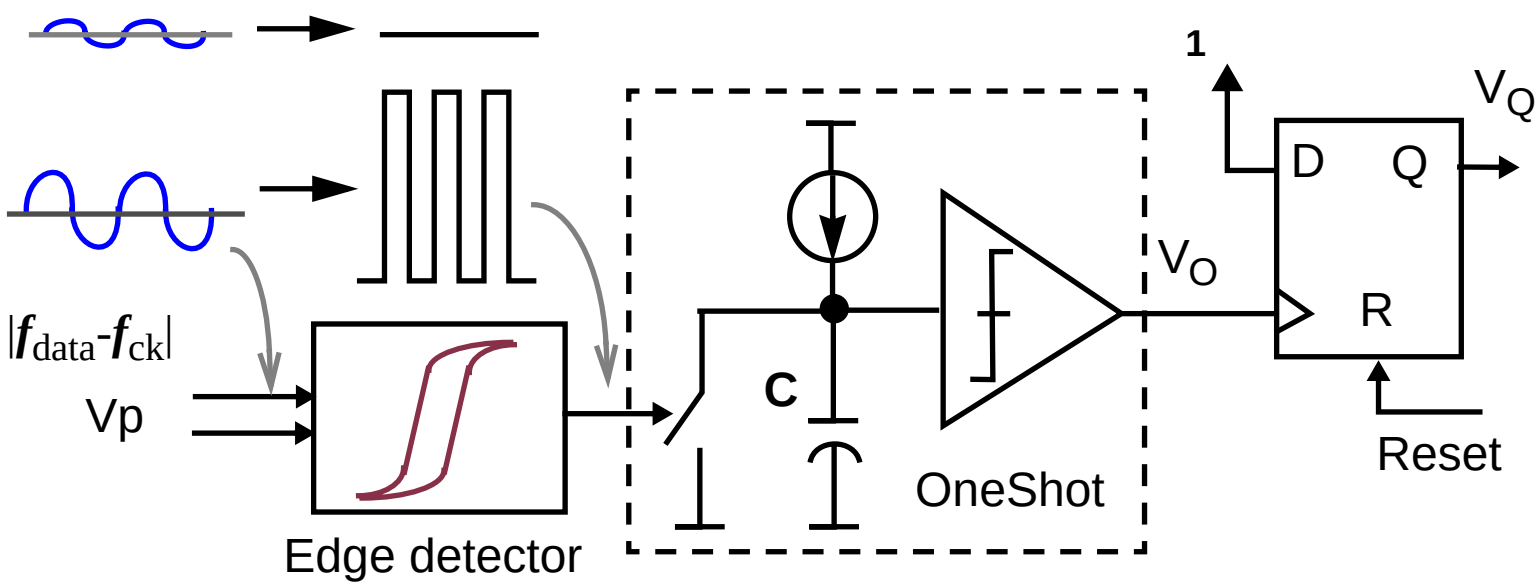
- A frequency acquisition aid solves the small capture range problem of the data-recovery phase detector

  → The frequency acquisition circuit sets the proper oscillation frequency before phase locking starts

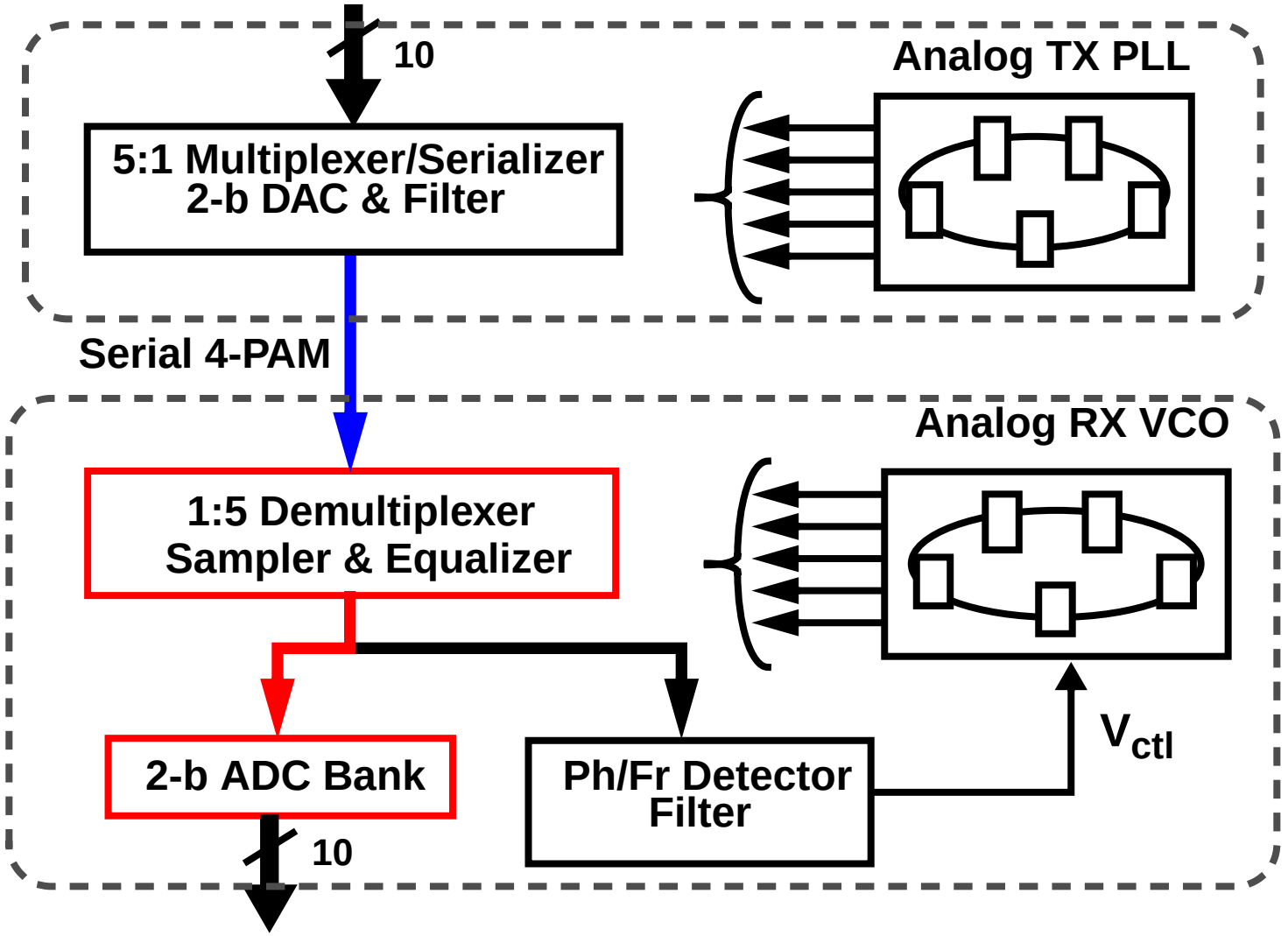
$$\begin{cases} V_Q=0 \; ; \; |f_{data}-f_{ck}| > \Delta f \\ V_Q=1 \; ; \; |f_{data}-f_{ck}| < \Delta f << f_{capture} \end{cases}$$



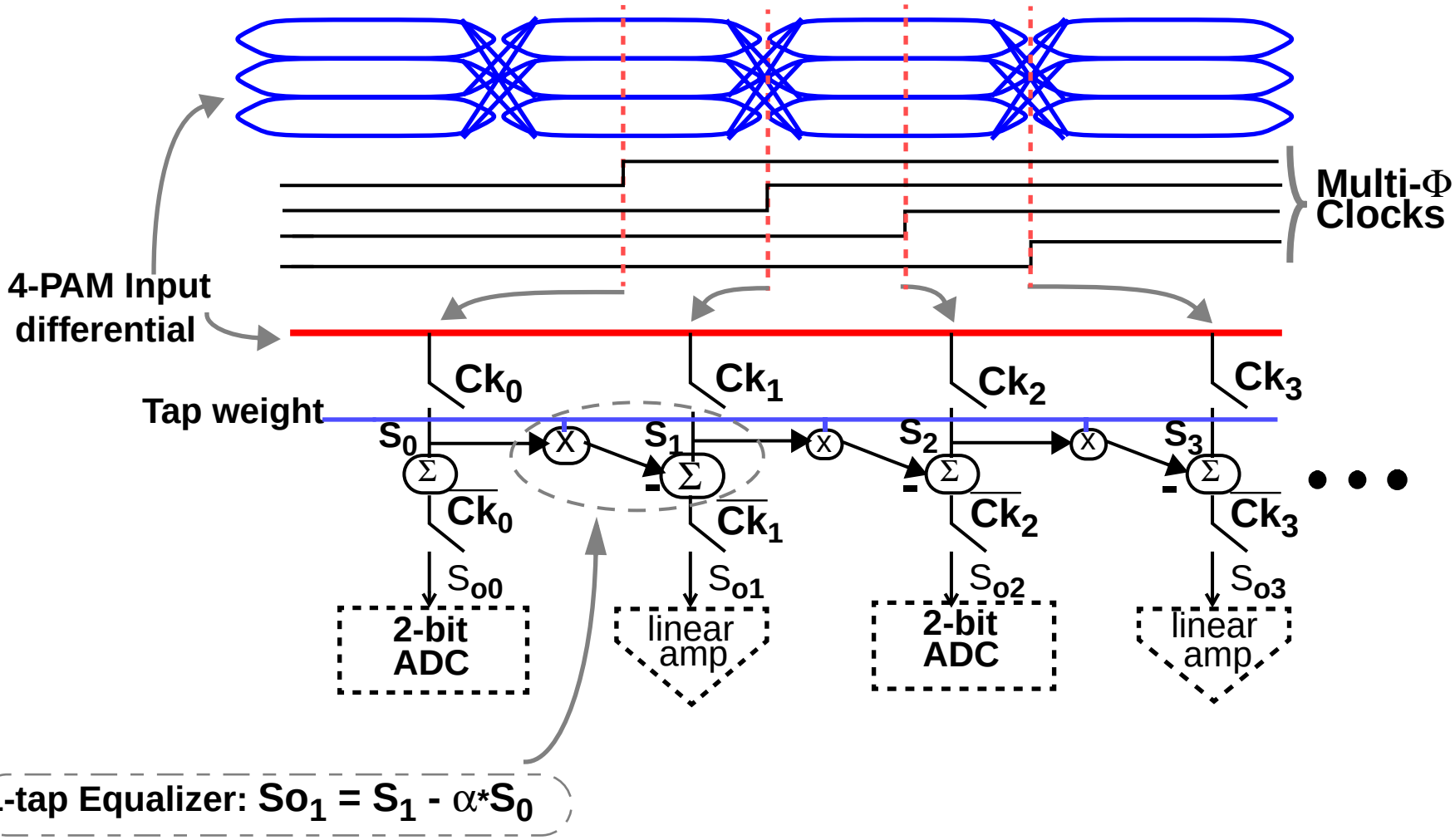
Frequency Monitor



Top Level Architecture



1:5 Demultiplexing Samplers and Equalizers



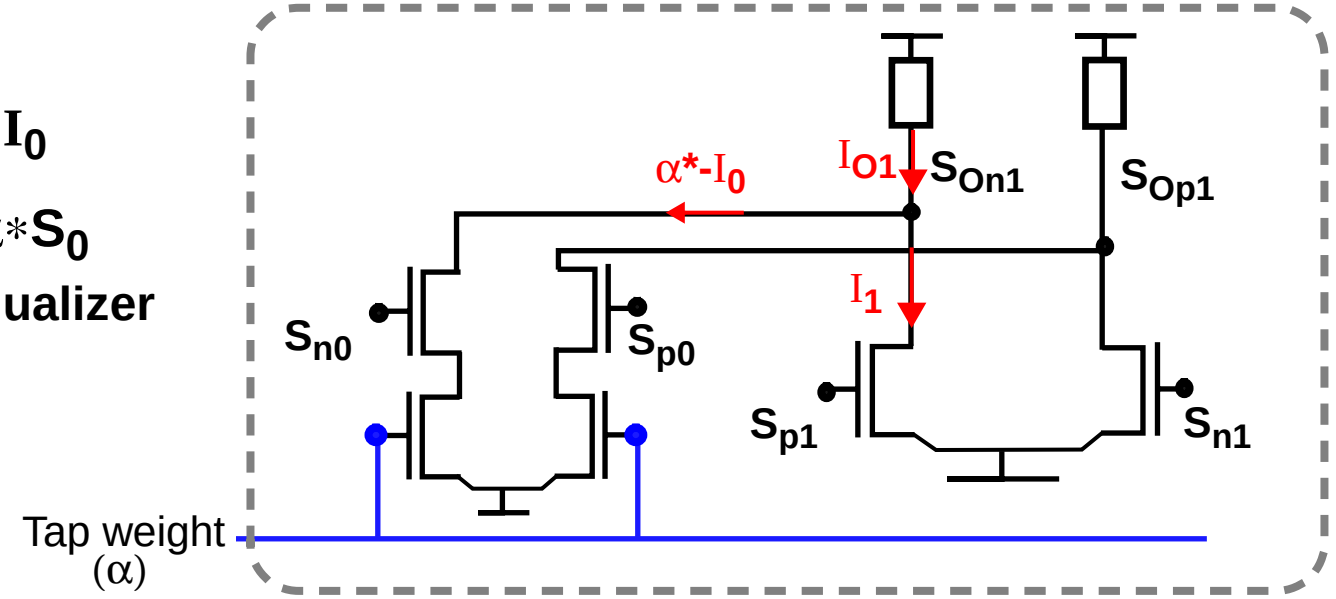
- 5 Samplers for the symbol centers and 5 samplers for transitions (x2 oversampling).
- Each equalizer uses the present and half a symbol earlier sample (half symbol spaced)

Half-symbol-Spaced 1-tap Equalizer

$$I_{O1} = I_1 - \alpha * I_0$$

$$S_{O1} = S_1 - \alpha * S_0$$

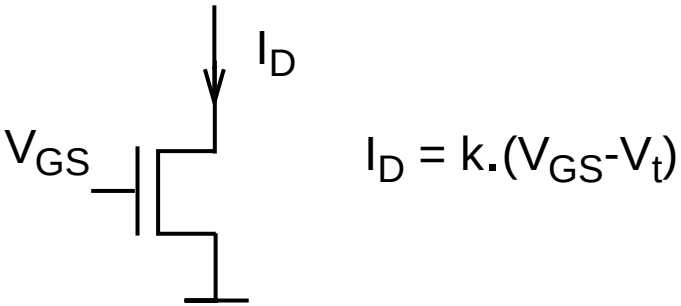
Analog 1-tap equalizer



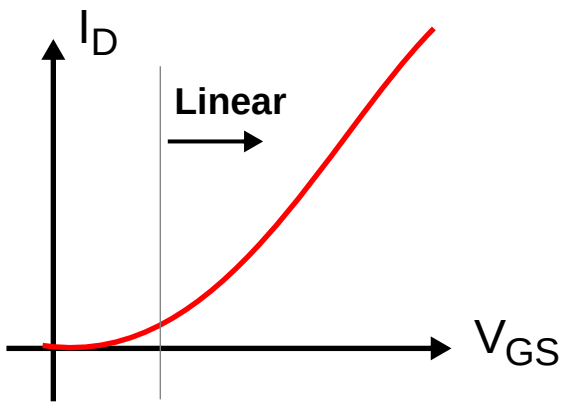
- Equalization function should be performed very fast

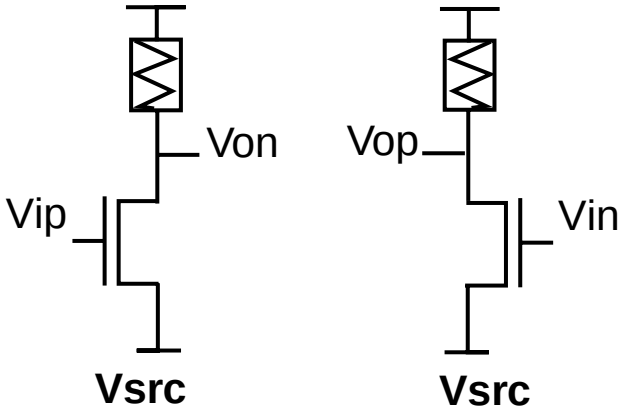
  → Subtraction is done by summing the currents, which are proportional to the sampled values with opposite polarity.
- Differential pairs should have a large linear range for proper operation of analog equalization.

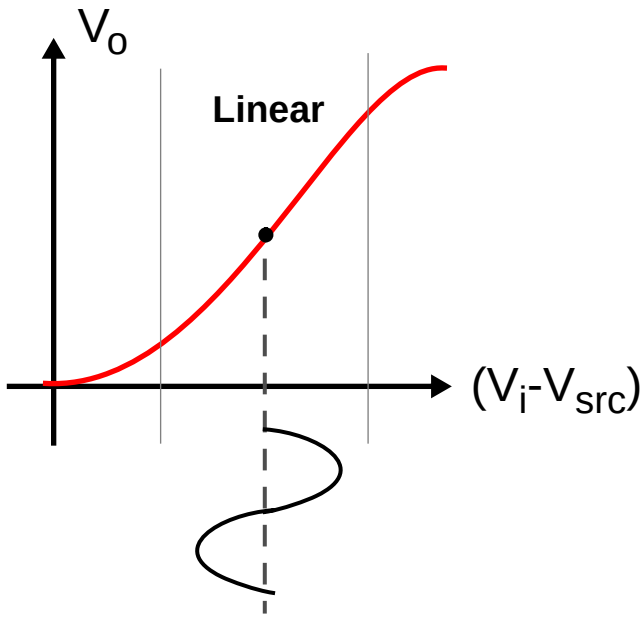
Input Preamplifier



$$I_D = k.(V_{GS}-V_t)$$

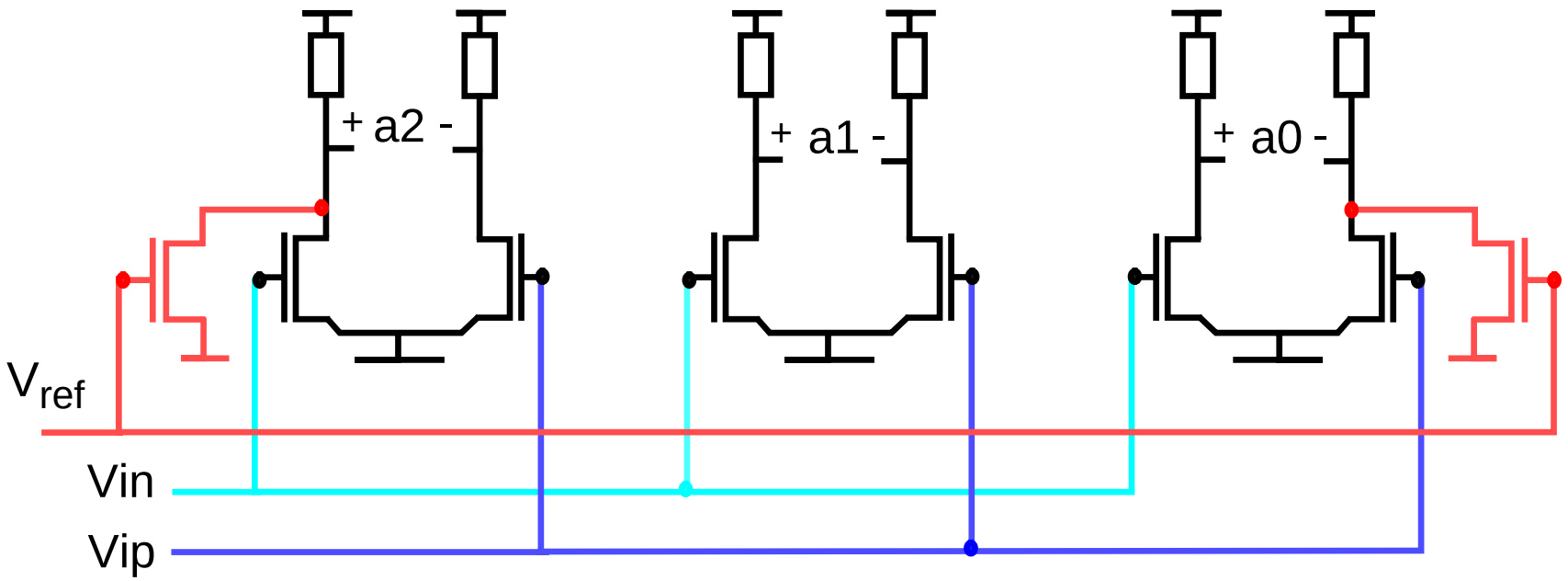


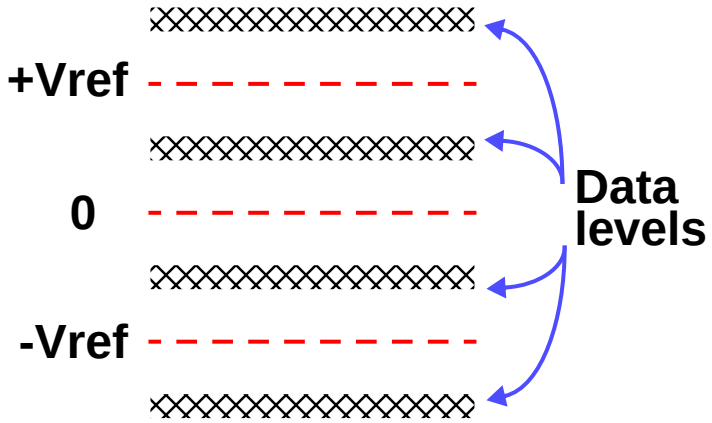




- Short-channel MOS has a linear I_D-V_{GS} characteristic in saturation region
- "Vsrc" should be set such that V_o-V_i is linear for all values of Vi.

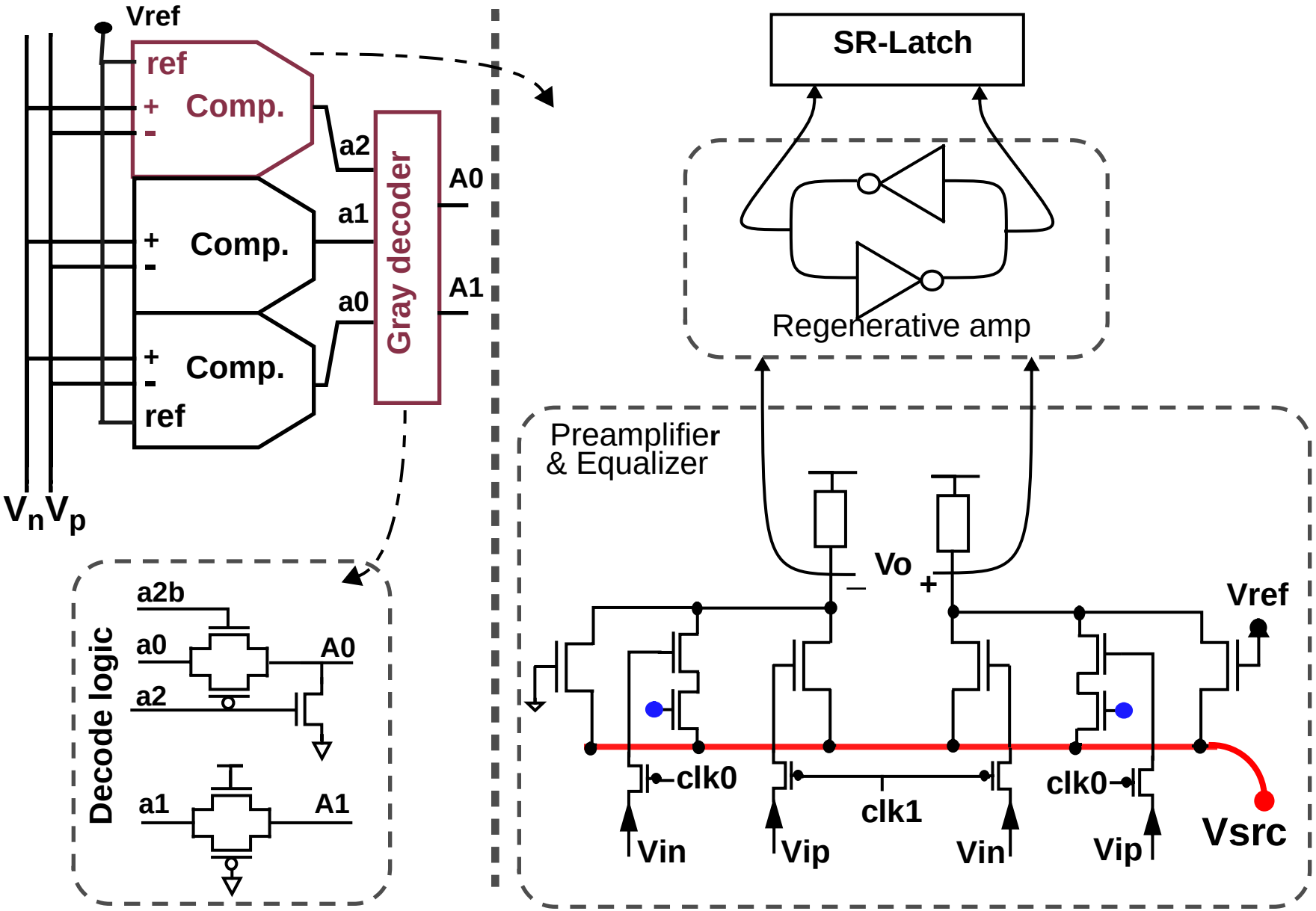
Differential 4-PAM Level detection





- Flash detection: Three comparators to detect the 4 levels.
- Differential signaling: Only one reference voltage is required

Input 2-bit ADC



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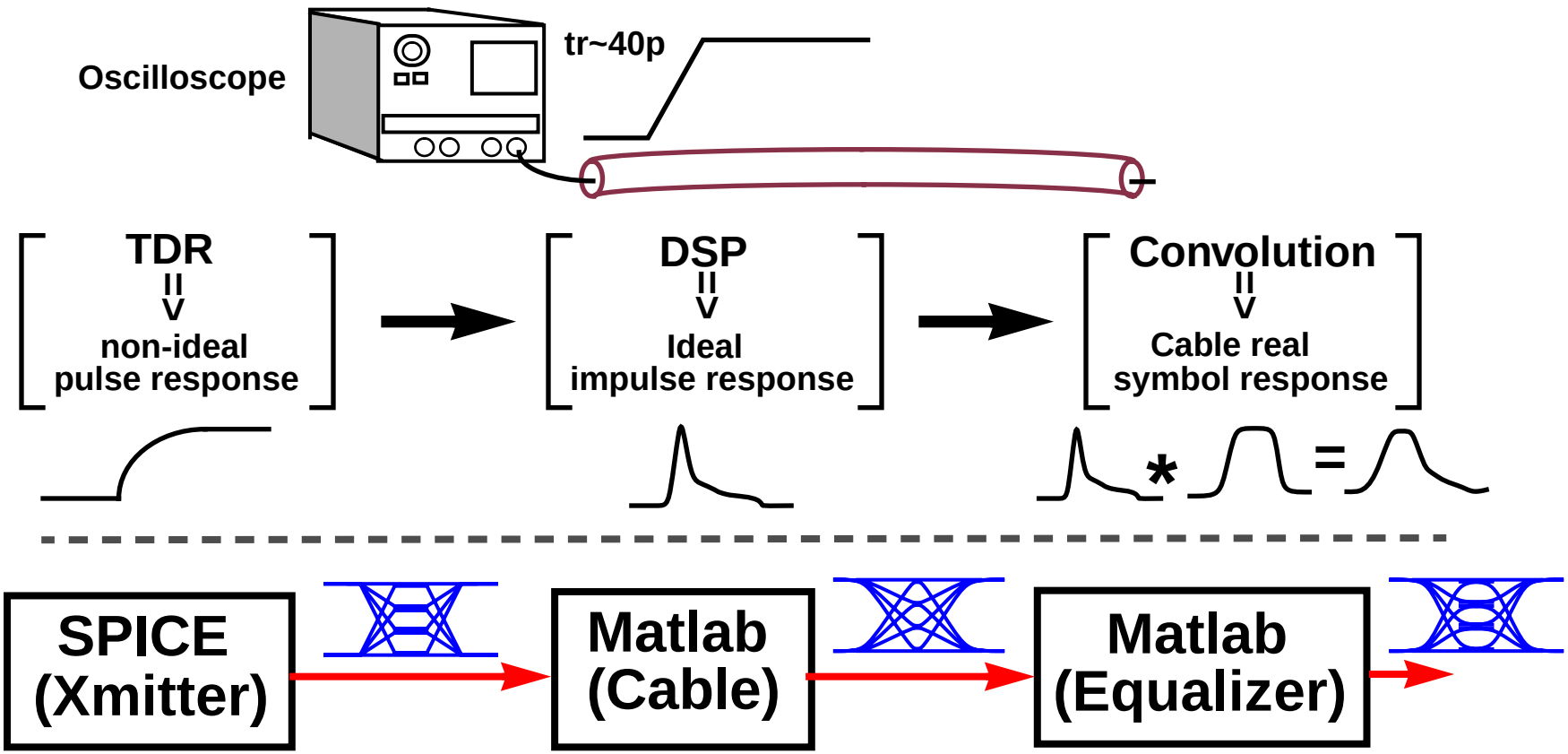
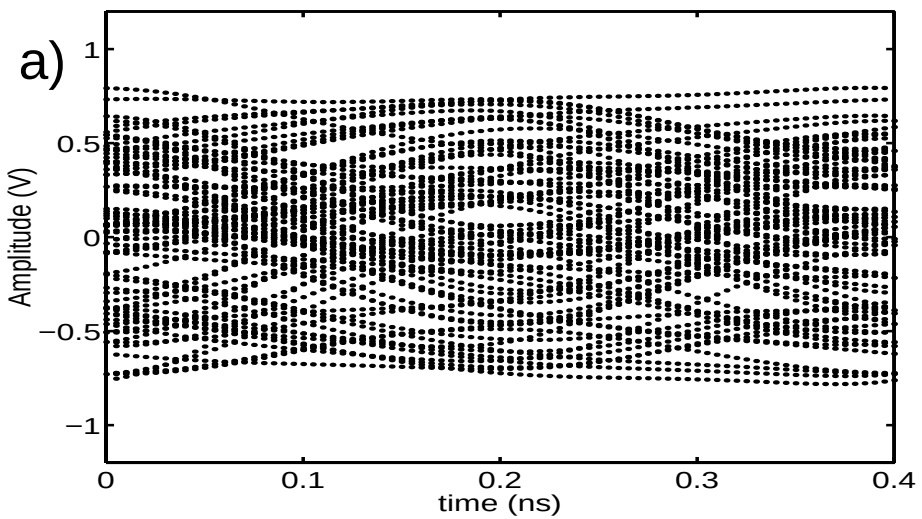
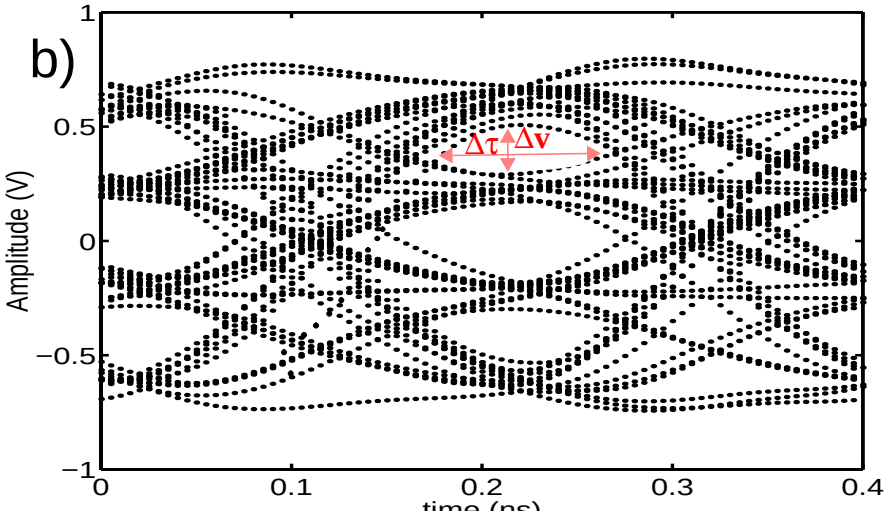
Modeling The Cable

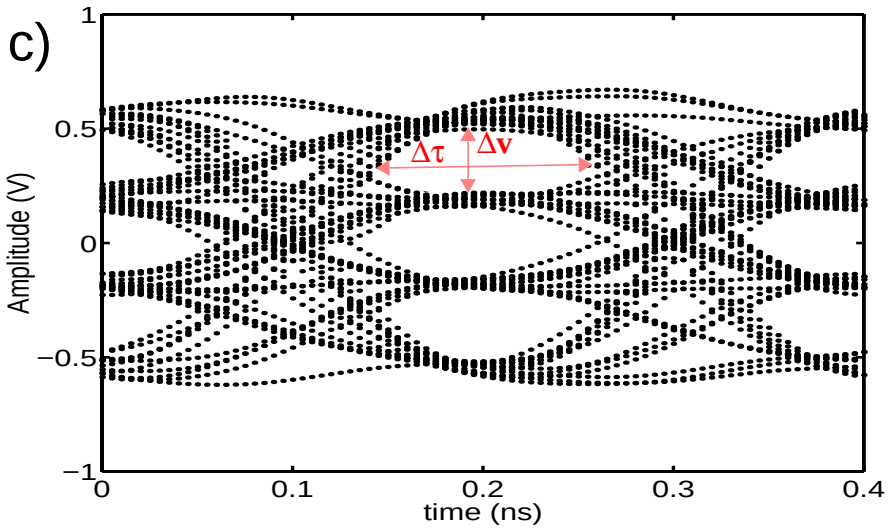


- SPICE models for skin effect are not ideal, need a better model:
  - → Directly measure the cable impulse response (time domain)
  - → Convolve it with the transmitted symbols

Simulated Eye Diagrams





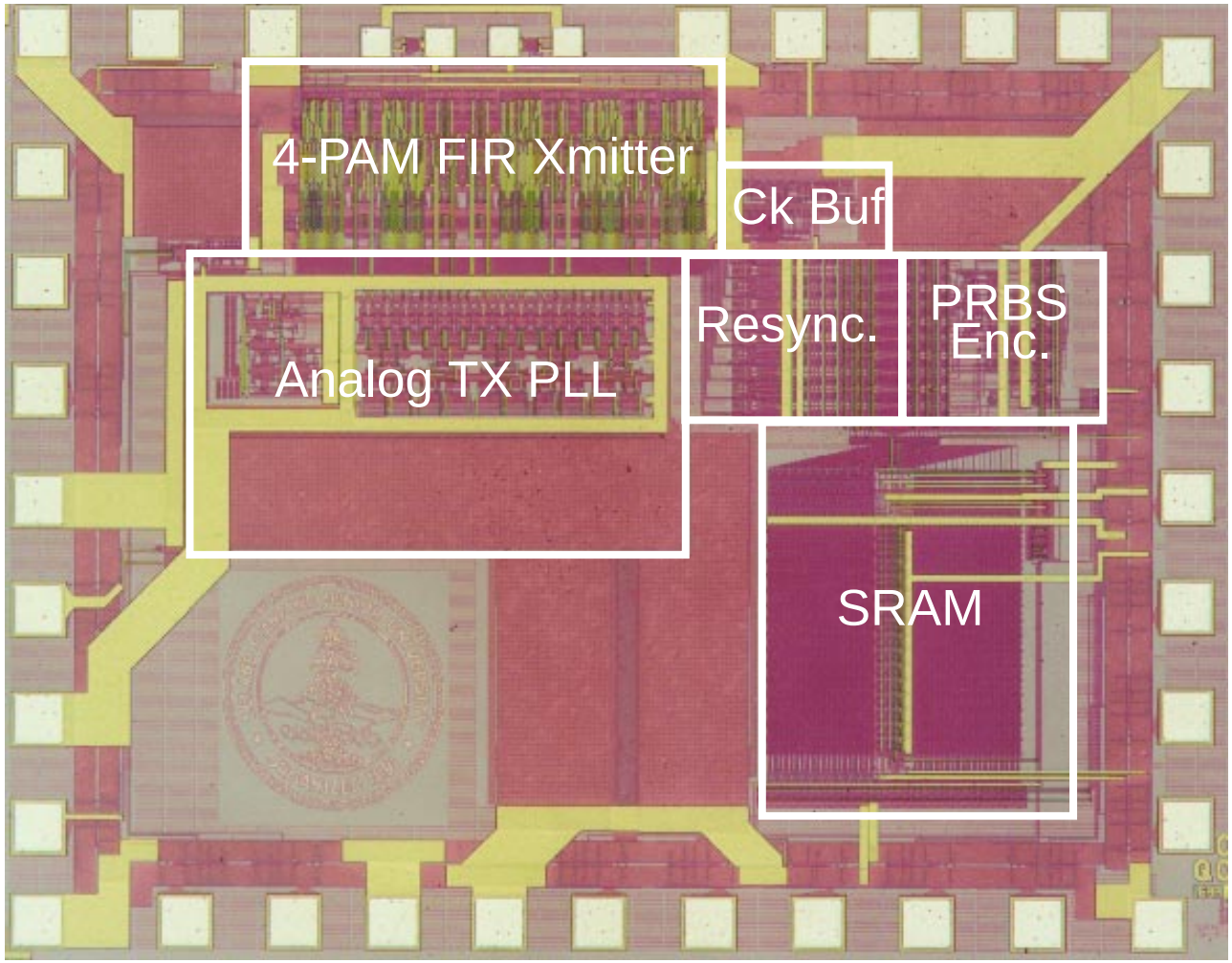


(a) Eye diagram after cable
(Without pre-emphasis)

(b) Eye diagram after cable
(With pre-emphasis)

(c) Eye diagram after cable
(With pre-emphasis/equalization)

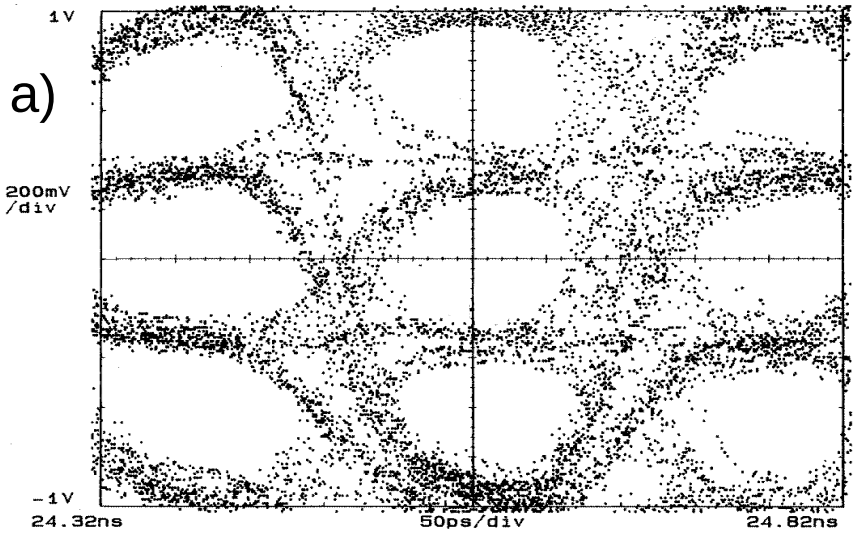
0.35-μm Transmitter Die Photo

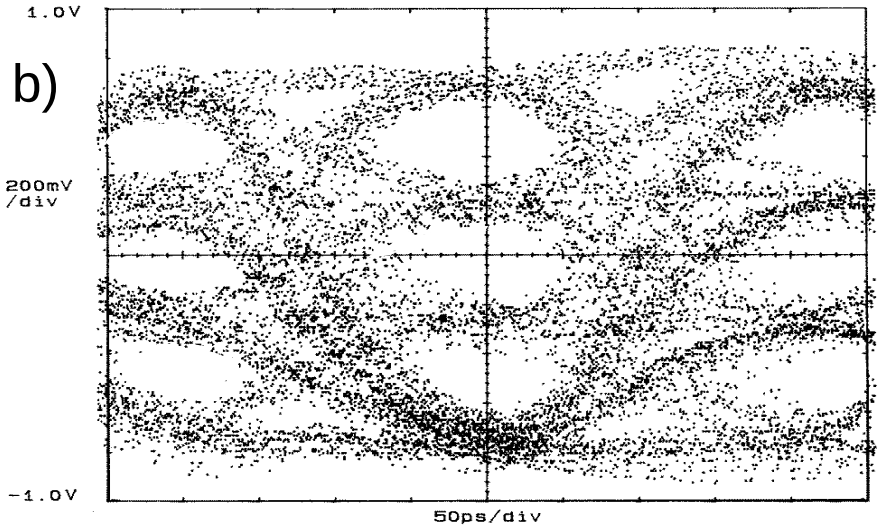


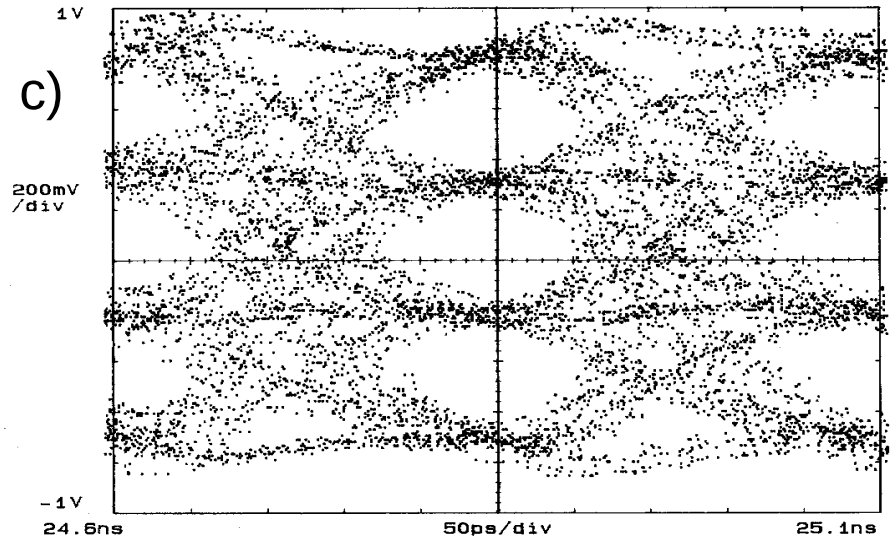
Total die area: 2mm x 1.5mm

4-PAM FIR transmitter: 0.8mm x 0.3mm

Measured Eye Diagrams







(a) 10Gb/s eye diagram at source
(No pre-emphasis)

(b) 10Gb/s eye diagram after the cable
(With Pre-emphasis)

(c) 8Gb/s Eye diagram after the cable
(With pre-emphasis)

0.35-μm Transmitter Performance

Transmitter Data Rate	Eye Height	Eye Width
10Gb/s, 10meter, W/ Pre-emphasis	200mV	90ps - 70ps
10Gb/s, 10meter, No Pre-emphasis	0	0
8Gb/s, 10meter, W/ Pre-emphasis	350mV	110ps - 90ps
8Gb/s, 10meter, No Pre-emphasis	< 60mV	< 50ps

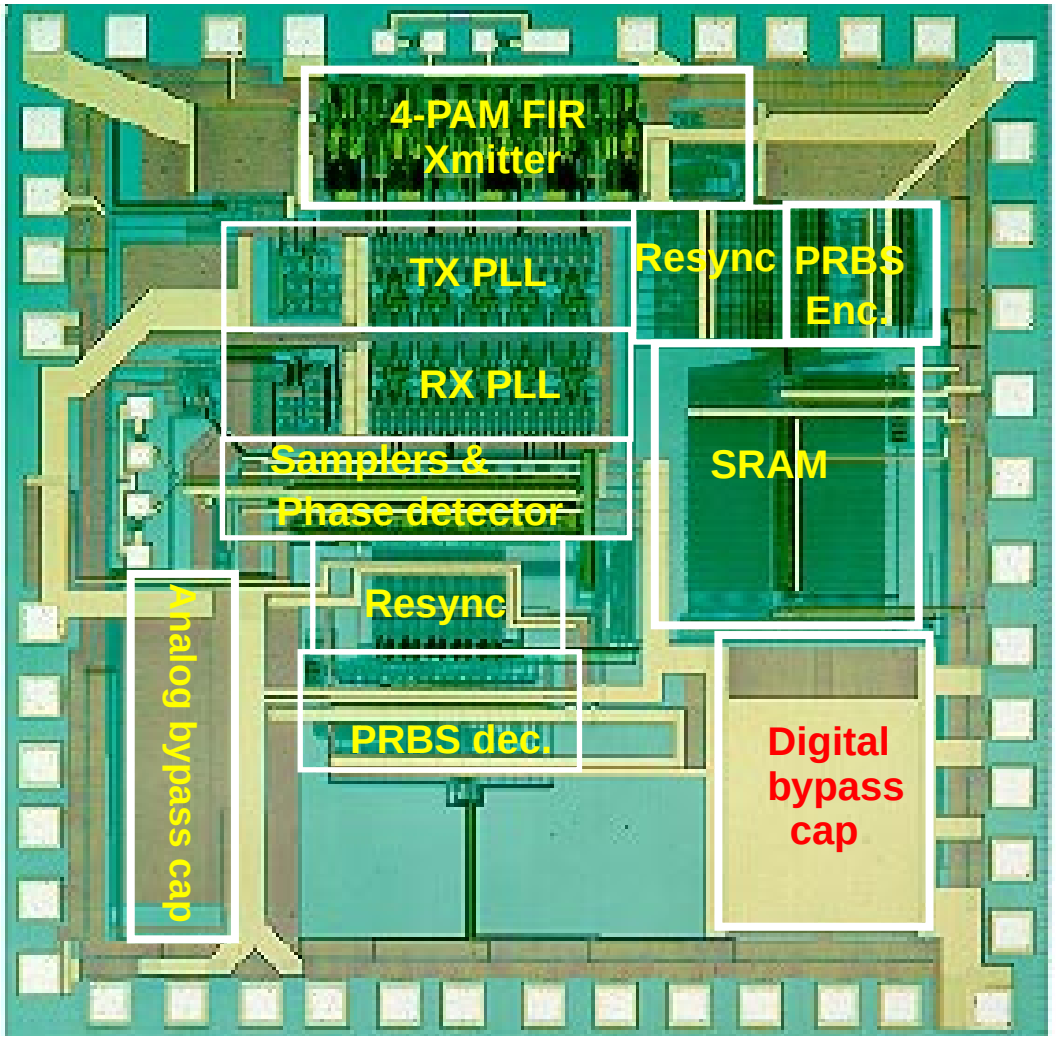
Transmitter Output Jitter:

Peak to peak	32ps
RMS	8ps

Power @ 10Gb/s (5Gsym/s):

Analog	0.7watts
Output Driver	0.5watts
Sync/Logic	0.3watts
Total	1.5watts

0.3-μm Full Transceiver Die Photo



Total die area: 2mm x 2mm

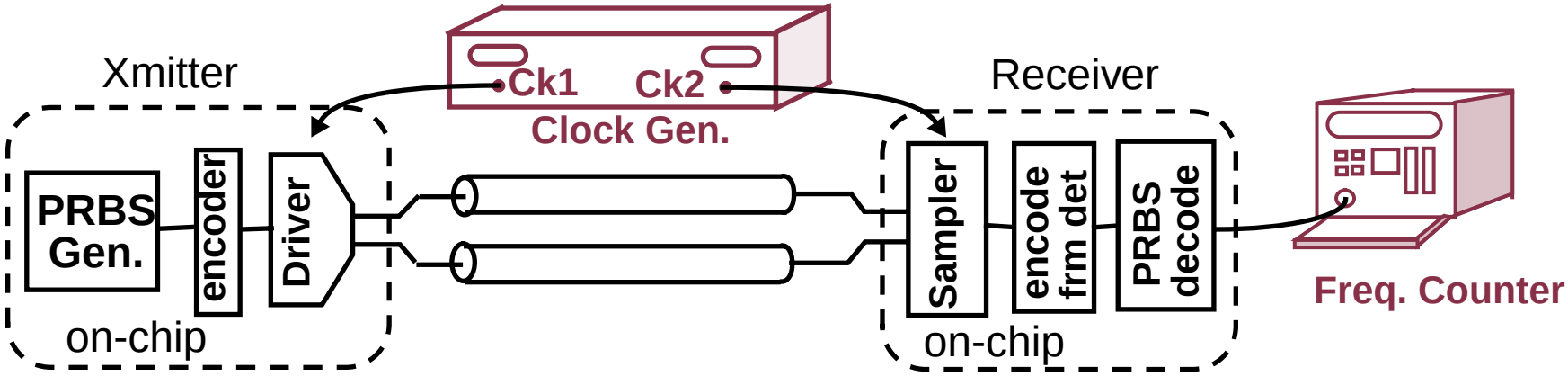
Total receiver data recovery section: 0.85mm x 0.43mm

0.3-μm Transceiver Performance

Maximum link speed	8Gbps @ 3V
Transmitter output **Jitter** @ 8Gbps	11ps (peak-peak), 2ps (rms)
Receiver PLL **Jitter** @8Gbps	28ps (peak-peak), 4ps (rms)
Receiver PLL dynamics	BW > 30MHz, Ph.m. > 48°
Receiver PLL **capture range**	~ 20MHz
Min. input swing to capture lock	±400 mV (diff.)
Min. input swing to maintain lock	±300 mV (diff.)

Power 8Gb/s, 3V	Analog: 750mW	4-PAM driver: 220mW	Other: 130mW	Total: 1.1W

BER Measurements



→ At 8Gbps: BER ~ 10^{-7}, Window = 50ps

(almost no improvement with input equalizer)

→ At 6Gbps: BER ~ 10^{-14}, Window = 150ps

(30ps improvement with input equalizer)

- Possible factors for lower BER at high speeds:
  - **Line Reflection**: Bad on-chip terminations, package/bondwire
  - **EMI** from neighboring high-speed bondwires

Contributions

❑ A solution for multi-Gbps transmission over bandwidth-limited cables in standard CMOS technology:

- Transmitter:
  - → A high-speed 4-PAM DAC design to reduce the symbol rate to half (v.s. 2-PAM).
  - → A FIR preshaping filter to perform at multi-Gbps rates with very low complexity.
  - → A control circuit to optimize the width of the transmitted symbols.
- Receiver:
  - → An analog FIR equalizer effective up to multi-GHz ranges in CMOS technology.
  - → A new proportional data-recovery phase detector for detecting 4-PAM serial data.
  - → A new frequency-acquisition technique for data-recovery PLLs.

❑ A 4-PAM transceiver capable of data transmission up to 8 Gbps over 10-m copper cable with BW~1GHz in 0.3-μm CMOS technology.

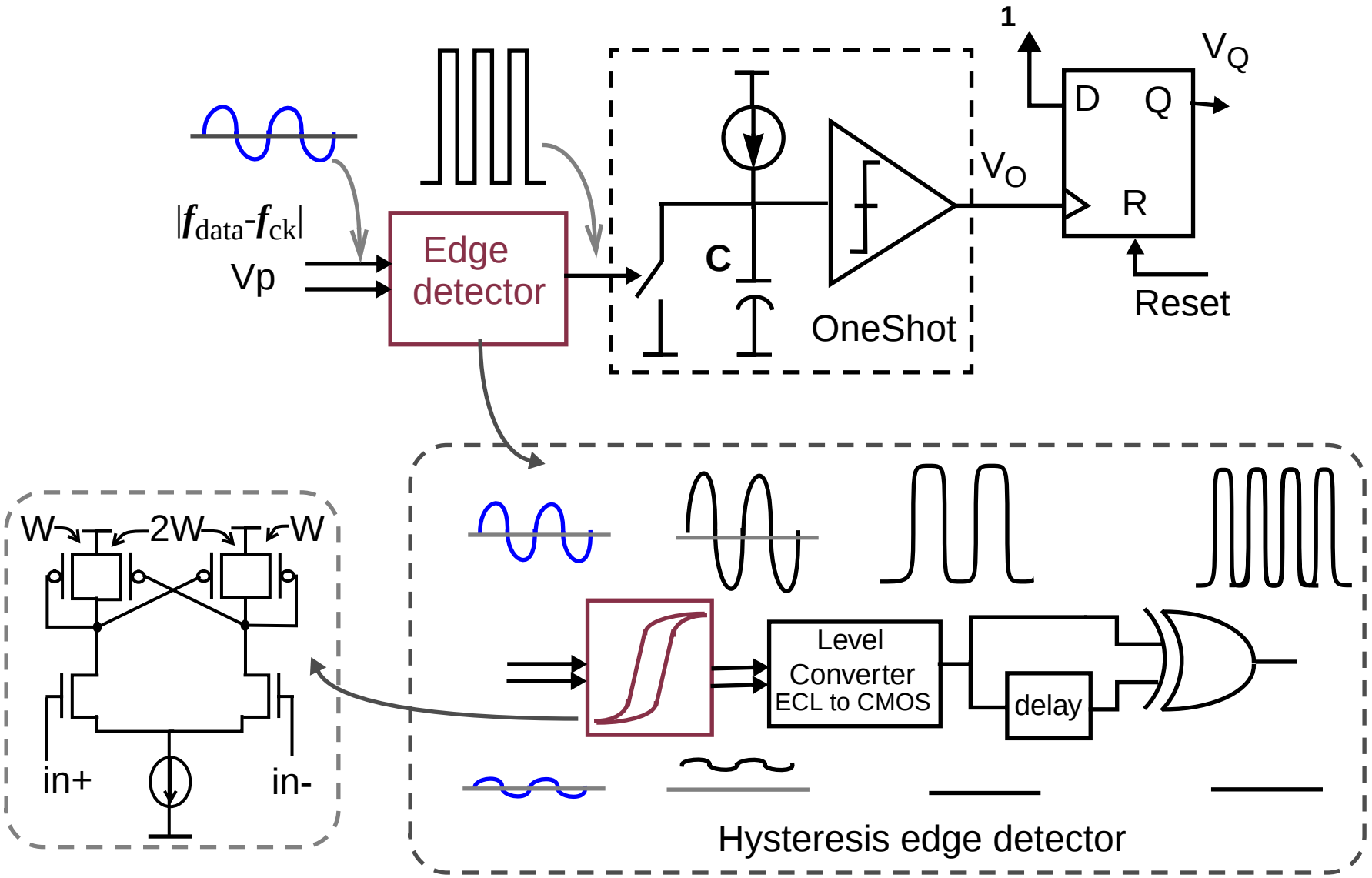
Acknowledgments

Future Work

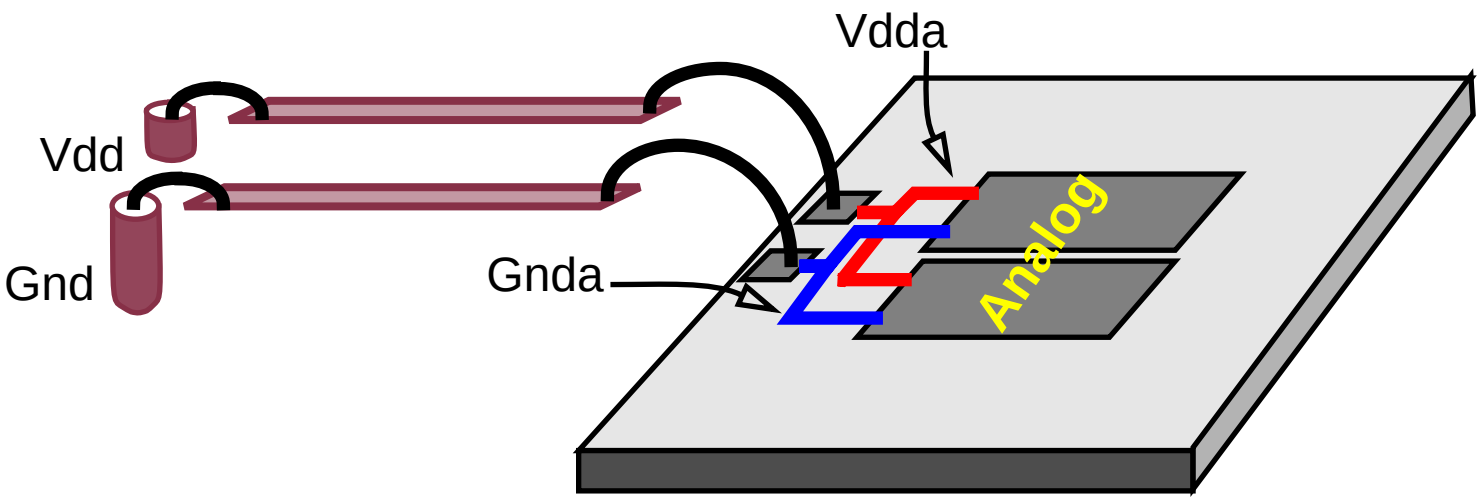
- Use higher-level *N*-PAM modulation
  - → Challenge: Very fast ADCs and DACs with higher resolution.
  - → Explore general methods of N-PAM data recovery.

- Advanced communication methods for narrow-band channels:
  - → Channel eigen function as transmission symbol.
  - → Maximum likelihood detection (ML)
  - → Multi-Carrier techniques (e.g DMT in ADSL)
  - → Use coding methods to reduce BER.

Frequency Monitor



Analog Supply Drop



- The on-chip VCOs speed was limited to 800MHz (8Gbps) due to analog supply drop
  - → Analog supply traces has ~1.8Ω resistance in series.
    - Only one pin for “Vdda” or “Gnda”
  - → 250mA analog supply current at 8Gbps => ~0.45V drop on analog supply!