A 115mW CMOS GPS Receiver

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OUTLINE

- **GPS Overview / Receiver Architecture**
- Low-Noise Amplifiers
  - CMOS noise models.
  - Power-constrained optimization.
- Active $G_m - C$ Filters
  - Dynamic range analysis.
  - Power-efficient transconductor design.
- CMOS GPS Receiver Implementation
- Experimental Results
- Summary and Contributions

GPS OVERVIEW: WHY RF CMOS?

- CMOS enjoys the benefits of aggressive scaling, driven by the microprocessor industry.
- Economies of scale. We want to be a barnacle on the Intel whale.
- Future co-integration of baseband (DSP).
- If it *can* be done competitively in CMOS, it will.

GPS OVERVIEW: THE SYSTEM

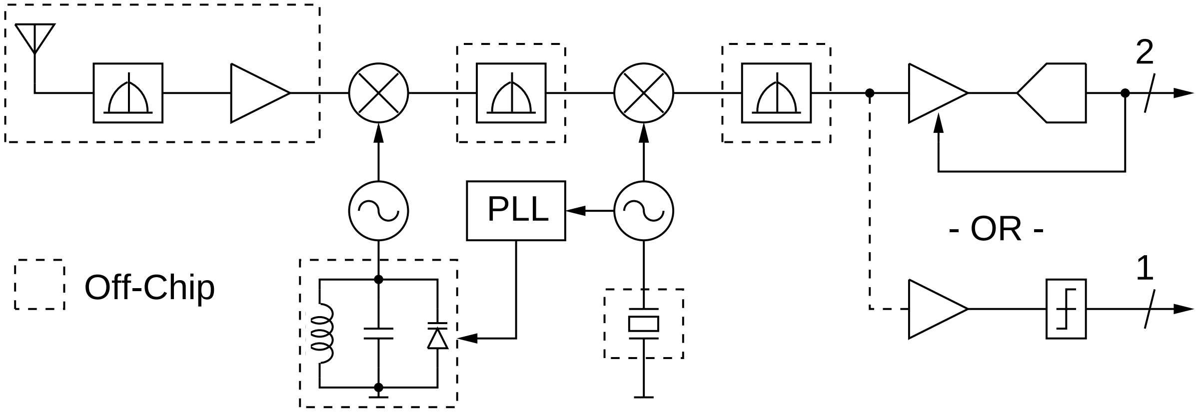
- 24 satellites in LEO, broadcasting their position and local time.
- With 4 satellites in view, can use one-way ranging to solve for x,y,z,t.
- Consumer applications: automotive navigation, smart cellular handoff, cellular emergency (911) dispatch, smart clocks.
- For wide proliferation, need receivers to be cheap, compact (single-chip), low-power and easy to use.

GPS OVERVIEW: TYPICAL RECEIVER ARCHITECTURES

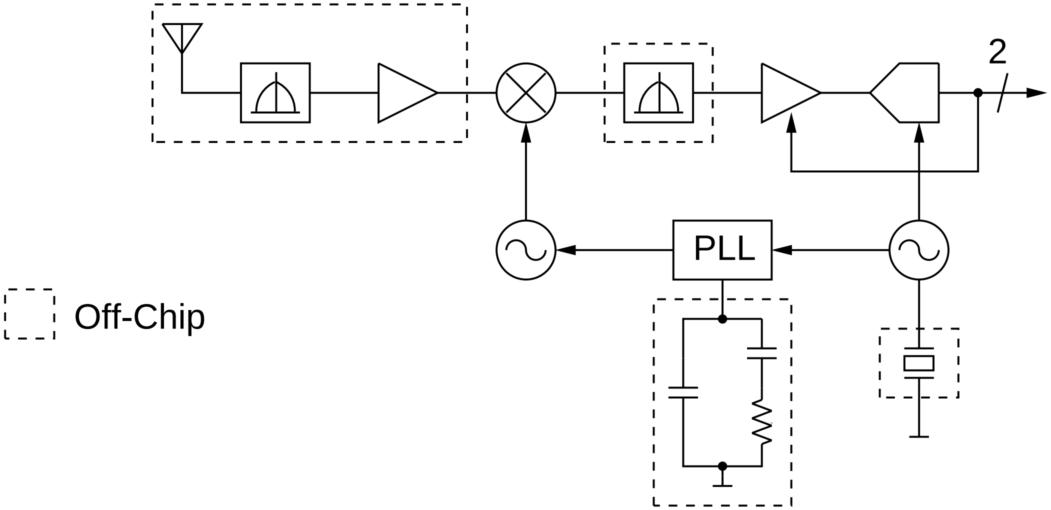
Distinguishing Features:

- Typical on-chip P_D is 100mW – 500mW
- Off-chip LNA or active antenna
- Off-chip IF filtering
- 1 or 2 bit quantization

Dual-Conversion



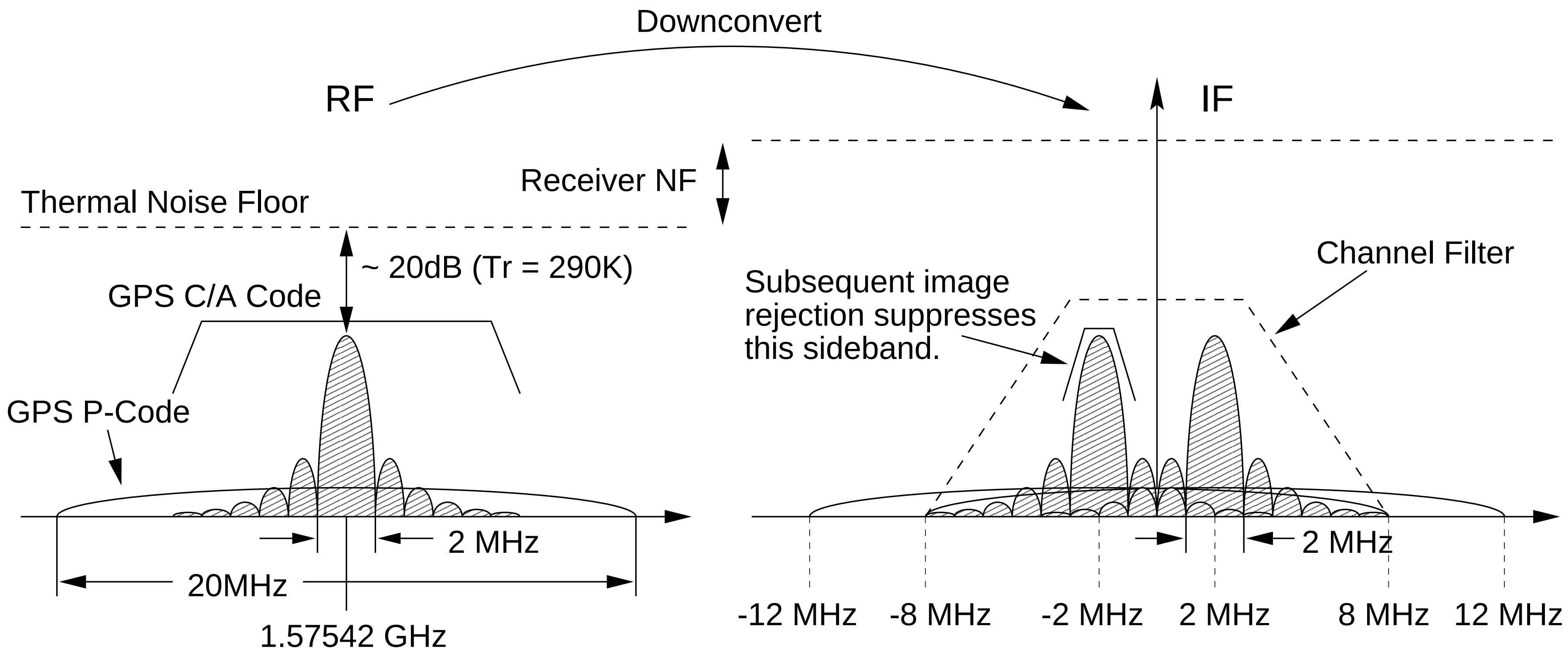
Single-Conversion



GPS OVERVIEW: TYPICAL RECEIVER SPECIFICATIONS

Spec	Sony (JSSC Apr’97)	GEC Plsy. GP2010	SiRF GRF-1
LNA NF	2dB (ext)	$\approx$ 2dB (ext)	(ext)
Chip NF	6.1dB	$\approx$ 10dB	—
IIP3	-14.5dBm	—	—
P-1dB	-29dBm	—	—
Total Gain	107dB	106dB	—
ADC	1-bit	2-bit	2-bit
Power	81mW @ 3V	200mW @ 3V	500mW @ 5V
Technology	15GHz Bipolar	Bipolar	—
Missing	2 Filters LNA, PLL LF	2 Filters, LNA, PLL LF	Filter, LNA

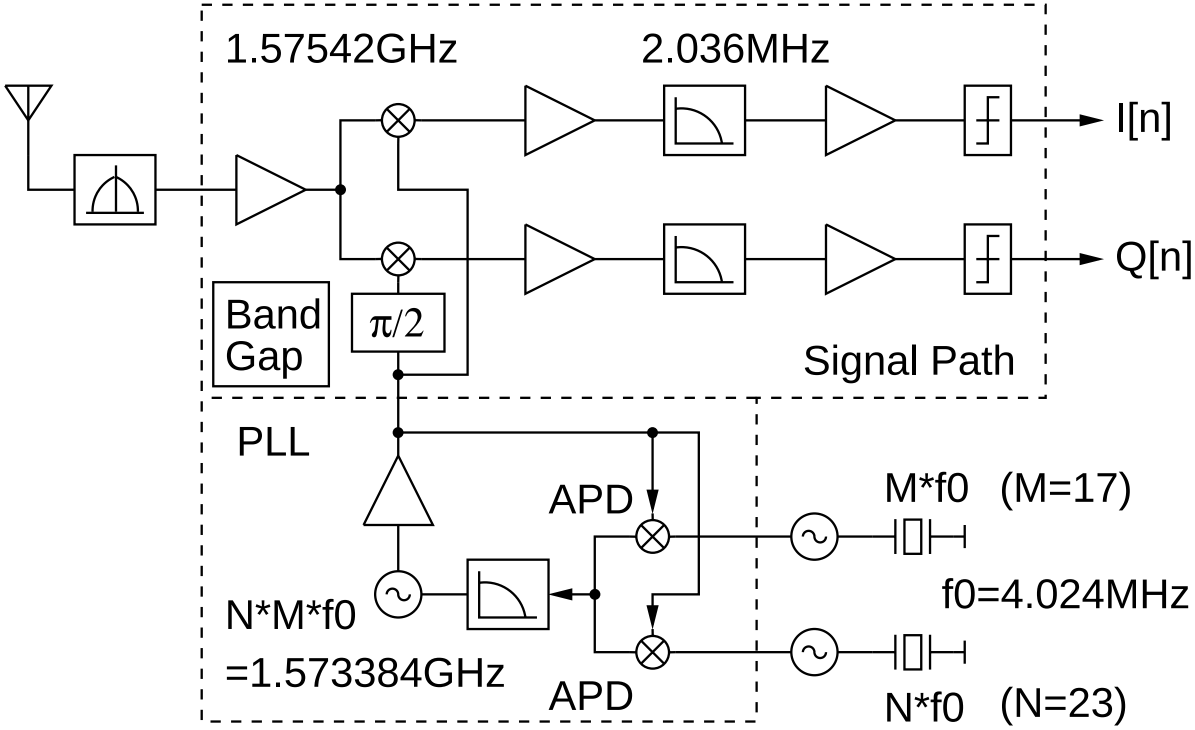
GPS OVERVIEW: SIGNAL STRUCTURE



ARCHITECTURE: LOW-IF RECEIVER

Primary Goal: Make choices to minimize P_D, maximize integration.

- Low-IF ⇒ On-chip active channel filter.
- Image in GPS band ⇒ Relaxed I/Q matching.
- Eliminate PLL prescaler ⇒ Saves power / noise.
- 1-bit quantization for simplicity.



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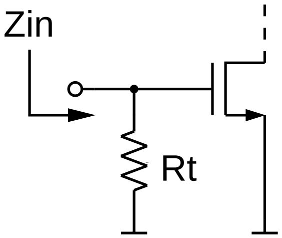
LNA: How to get 50Ω

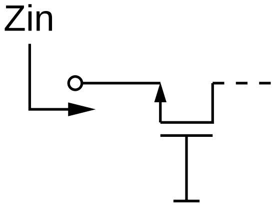
Several Common Techniques



Resistive Termination

$$Z_{in} = R_t$$

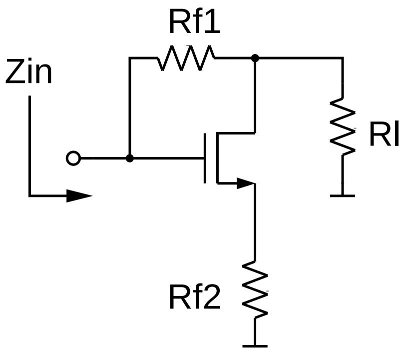
Great termination.
Poor NF.



g_m Termination

$$Z_{in} = \frac{1}{g_m}$$

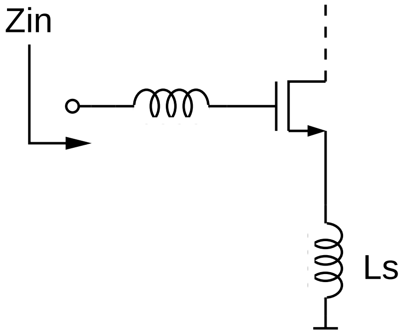
NF $>$ 3dB
($\gamma > 1$)



Dual Feedback

$$Z_{in} = \sqrt{R_{f1} R_{f2}}$$

Broadband.
High power dissipation.

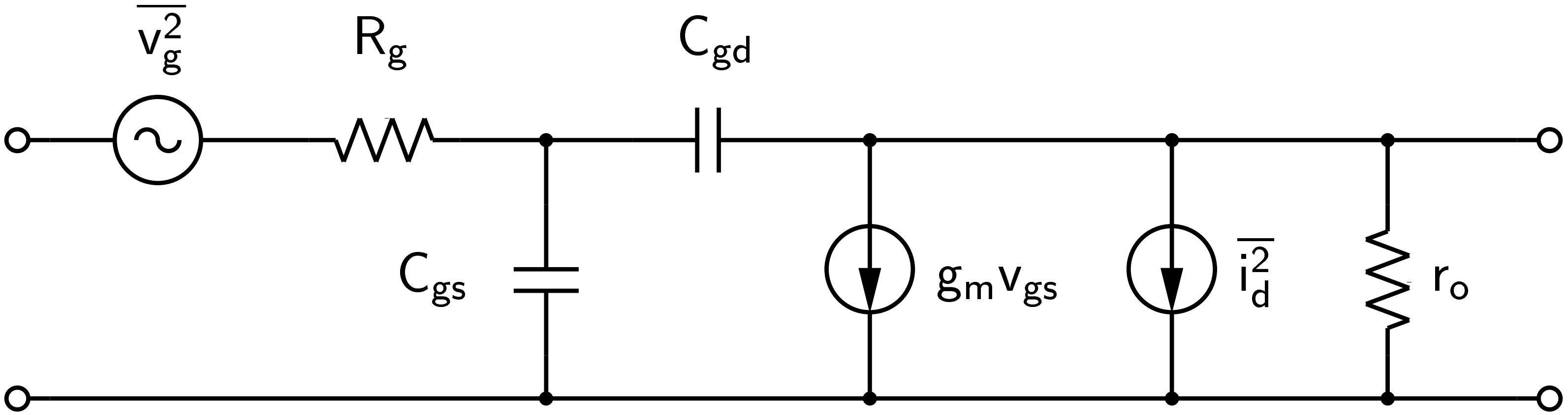


Inductive Degeneration

$$\mathrm{Re}\left[Z_{in}\right] = \frac{g_m L_s}{C_{gs}}$$

Narrowband.
Best NF.

LNA: STANDARD CMOS NOISE MODEL

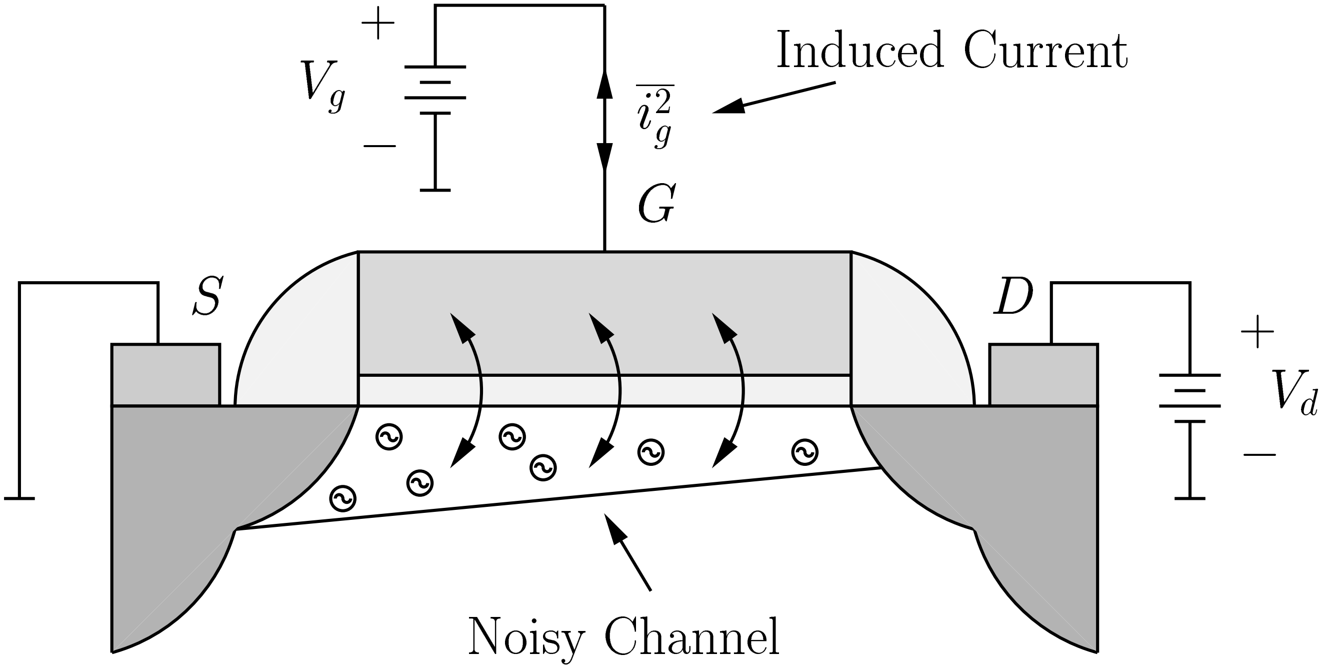


- Channel thermal noise is the dominant source of noise.

$$\overline{i_d^2} = 4kTB\gamma g_{d0}$$

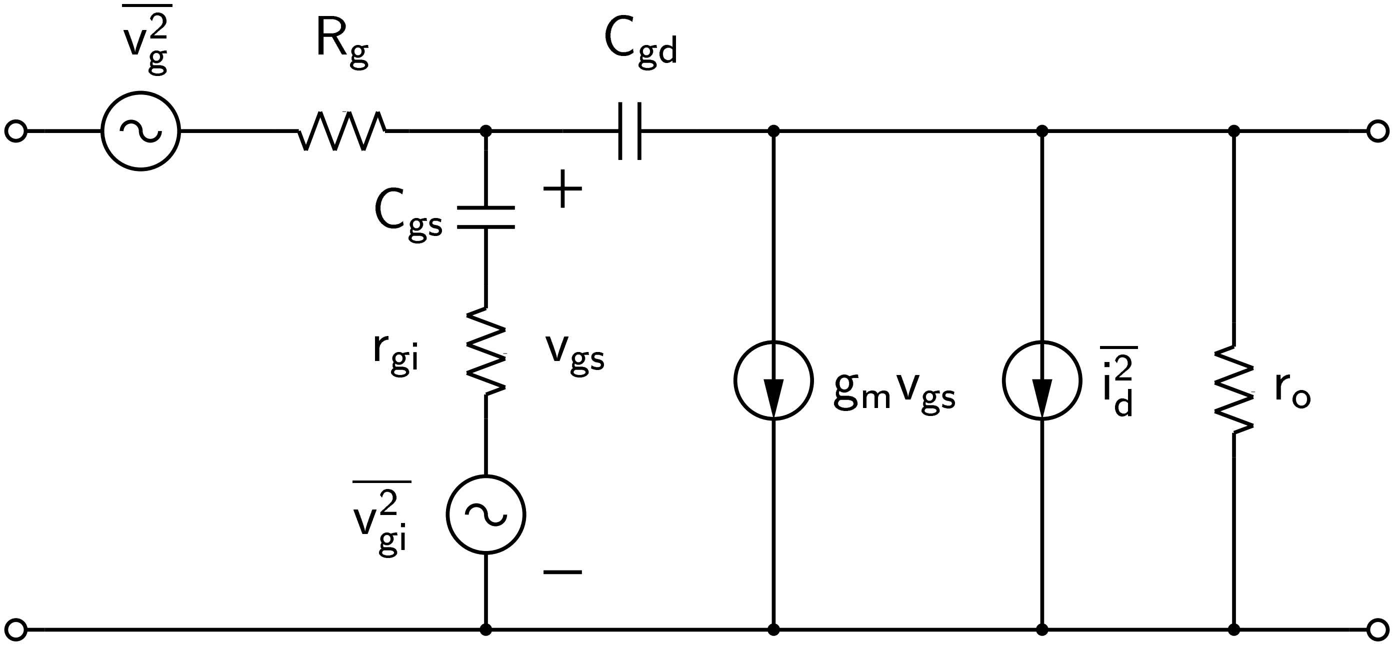
- Gate resistance noise can be minimized by good layout.
- Problem: Yields $F_{min} = 0\ \mathrm{dB}$!

LNA: INDUCED GATE EFFECTS



- Gate noise current. $\overline{i_g^2} = 4kTB\delta\frac{(\omega C_{gs})^2}{5g_{d0}}$
- Real component of Y_g. $\mathrm{Re}\left[Y_g\right] = \frac{(\omega C_{gs})^2}{5g_{d0}}$

LNA: REVISED CMOS NOISE MODEL



$$\begin{aligned}\overline{v_{gi}^2} &= 4kTB\delta r_{gi}\\ r_{gi} &= \frac{1}{5g_{d0}}\end{aligned}$$

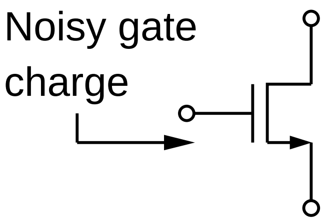
(Note the placement of v_{gs}.)

LNA: INDUCED GATE NOISE MODELS

Induced gate noise is not included in standard CMOS simulation models!
(Exceptions: Philips MOS9, Tektronix BSIM3)

How do we get around this?

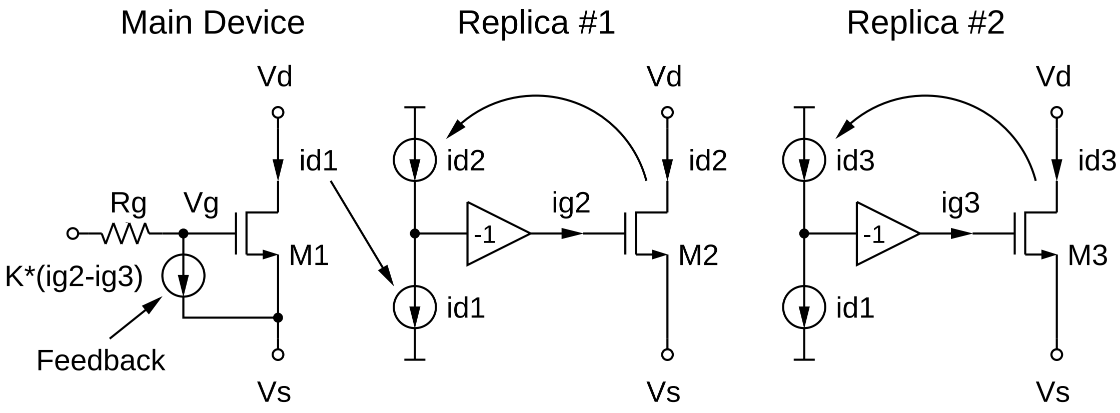
Charge Model



$$\overline{Q_g^2} = 4kTB\delta\frac{C_{gs}^2}{5g_{d0}}$$

Modify simulation code.

Macro Model



Can be used with any simulator/model.

LNA: OPTIMIZING NF

Two approaches:

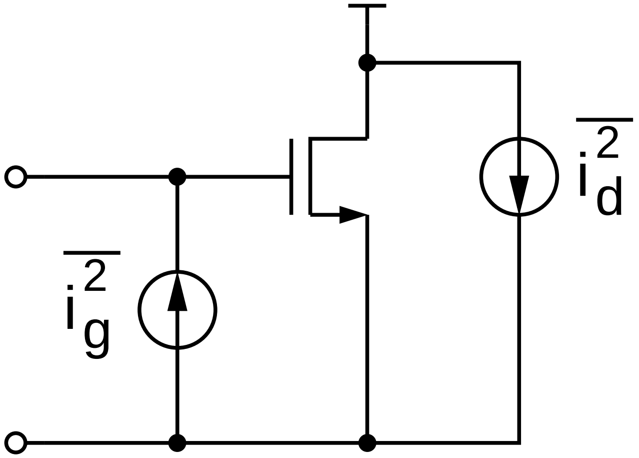
- Classical: Assume a *fixed* small-signal model for the device. Optimize the source impedance for minimum noise factor. (Haus et al. 1960)

  Problem - Ignores input match, power gain.

- Power-constrained: Assume conditions for input impedance match. Fix P_D and vary the device width for minimum noise factor.
  (Shaeffer, Lee 1997)

LNA: CLASSICAL F_{min}

The minimum noise figure can be calculated for the MOSFET according to the classical two-port approach, once the induced gate noise is included.

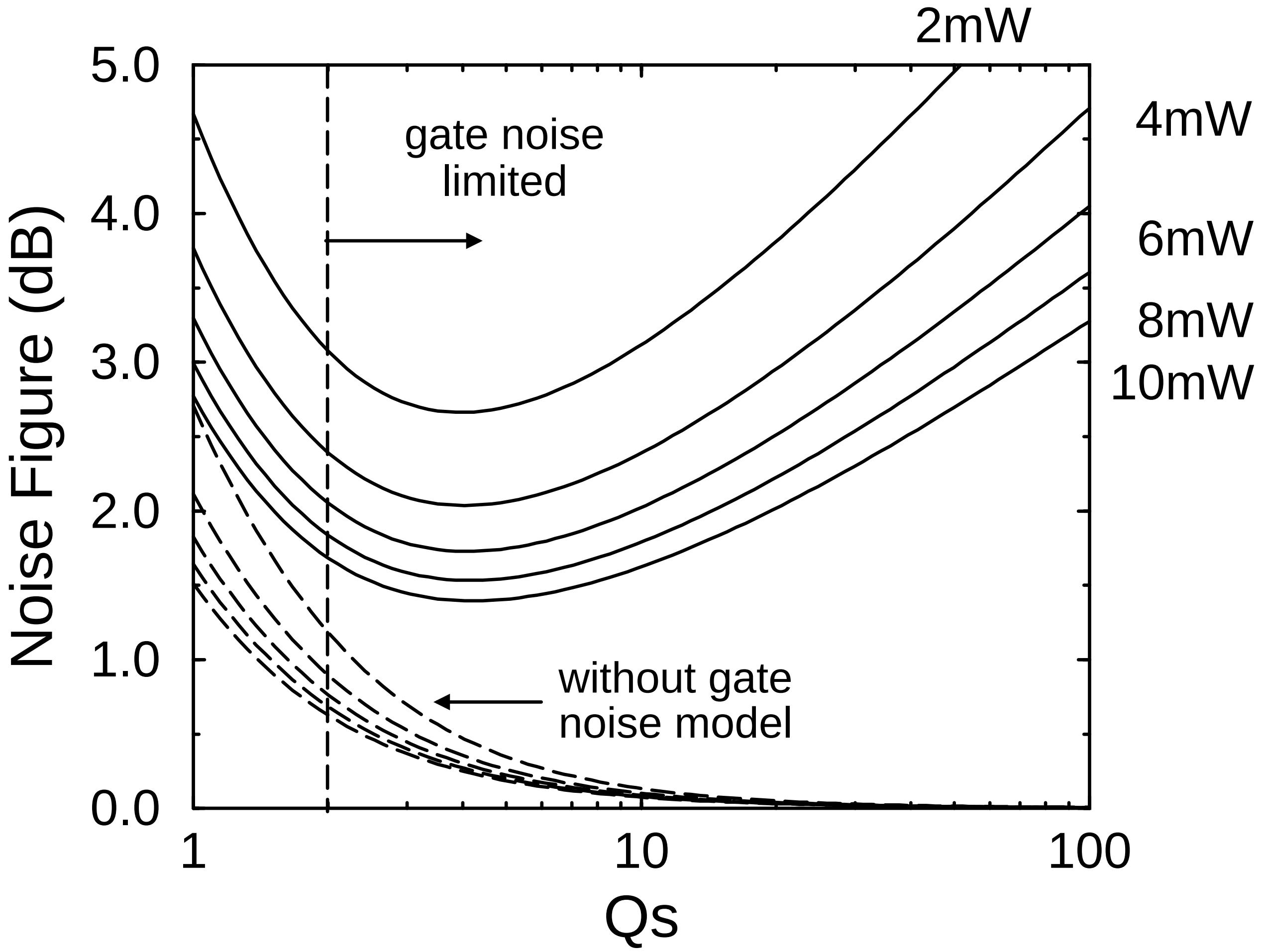


$$F_{min} = 1 + \sqrt{\frac{4}{5}\delta\gamma(1 - |c|^2)}\left(\frac{\omega_0}{\omega_T}\right)$$

$$Q_{opt} = \left|\frac{B_{opt}}{G_{opt}}\right| = \frac{\sqrt{\frac{5\gamma}{\delta\alpha^2}} + |c|}{\sqrt{1 - |c|^2}} \approx 2.162$$

H.A. Haus et al., ”Representation of noise in linear twoports,” Proc. of the IRE, January 1960.

LNA: POWER CONSTRAINED OPTIMIZATION



Assumptions

- $L_{eff} = 0.44\mu m$
- $\gamma = 1.3, \delta = 2.6$
- $V_{DD} = 2.5\mathrm{V}$
- $f_0 = 1.6\mathrm{GHz}$
- $R_s = 50\Omega$

Result: $Q_{opt} \approx 3.5$

Shaeffer and Lee, ”A 1.5V, 1.5GHz CMOS Low Noise Amplifier”, JSSC May 1997

LNA: POWER CONSTRAINED OPTIMIZATION

Power-constrained optimization yields a design with:

- Lowest NF for a given P_D
  $\frac{F_{min,P_D}-1}{F_{min}-1} = 0.763$
- Input impedance match.
- Higher G_m than the classical method.
- Higher current densities than the classical method.

Rule of thumb: $W_{opt} f_0 \approx 500\mu m \cdot \mathrm{GHz}$.

LNA: SUMMARY

- CMOS noise models are currently insufficient for design.
  - Modeling of hot electron effects.
  - Modeling of the induced gate noise.
- Power-constrained noise optimization technique permits:
  - Optimized noise performance.
  - Simultaneous input impedance matching.
  - Maximum LNA gain.
- Results: 2.4dB NF, 1.6GHz, 12mW, differential LNA in a 0.5μm CMOS technology. (6mW single-ended equivalent.)

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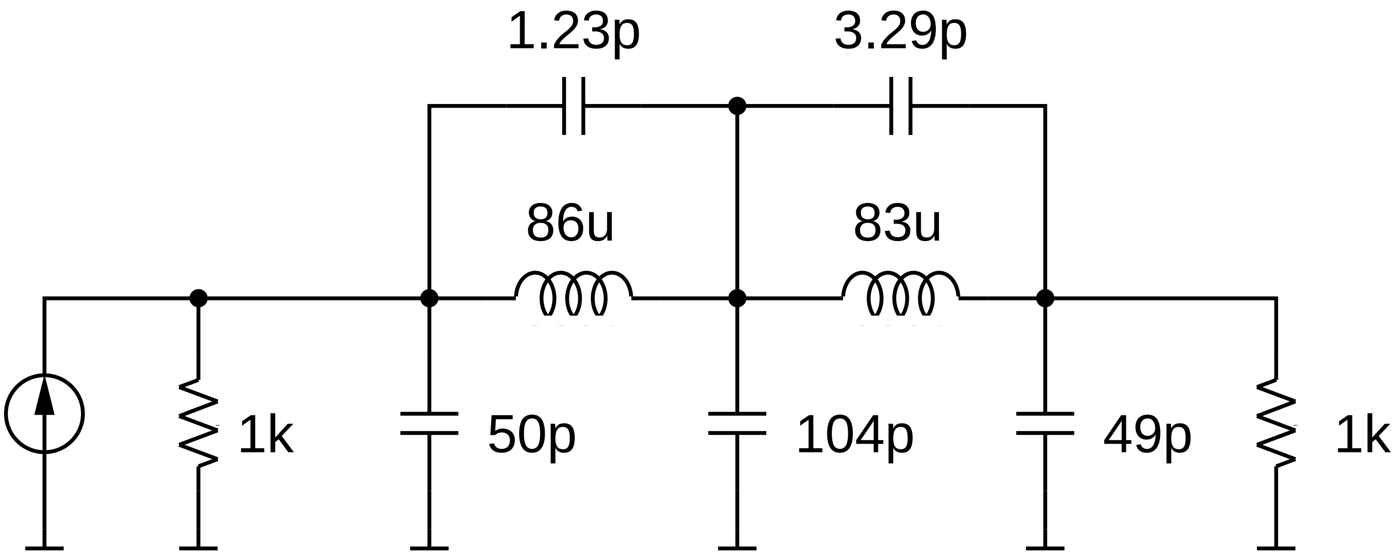
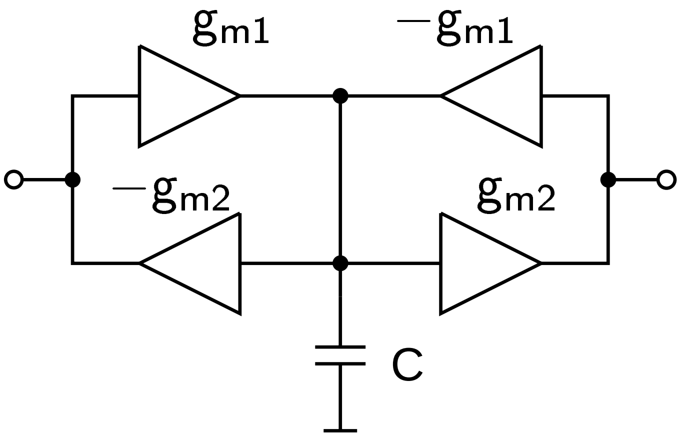
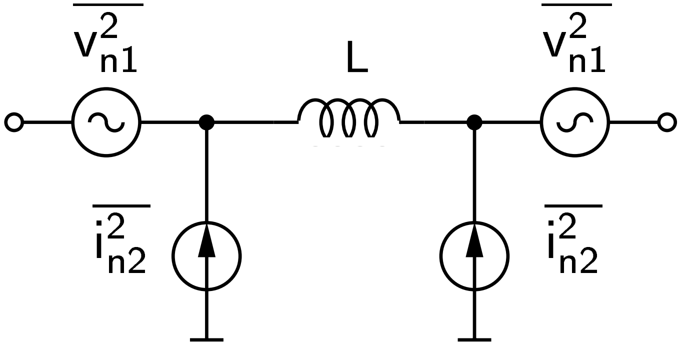
FILTER: ARCHITECTURE



- 5th-order elliptical lowpass filter.
- 3MHz bandwidth, 77dB stopband rejection.
- Inductors are impractical for integration.

FILTER: GYRATOR





$$L = \frac{C}{g_{m1} g_{m2}}$$

- A gyrator implements an active inductor.
- Noise, distortion limit the gyrator's utility.

FILTER: DESIGN APPROACH

The filter is the most critical signal path element, and therefore requires the most attention to detail. Some relevant ideas:

- Interesting fact: $F_{min} = 2\left(1 + \epsilon N\right)$. Independent of filter Z_0! This implies a fixed amount of *power gain* to suppress filter noise.
- Fixed $G_P \Rightarrow A_V \propto \sqrt{Z_0}$. Need to minimize Z_0 to maximize dynamic range.
- Seek linearization techniques that maximize G_m/I_{bias}. One sub-optimal approach would be linearization by degeneration.
- Use Class-AB techniques, if possible, to maximize power efficiency.

In short: *It all depends on the transconductor!*

FILTER: MAXIMIZING DYNAMIC RANGE

- Filter architecture.
  - Minimize Q and order of the filter.
  - Maximize transition bandwidth.

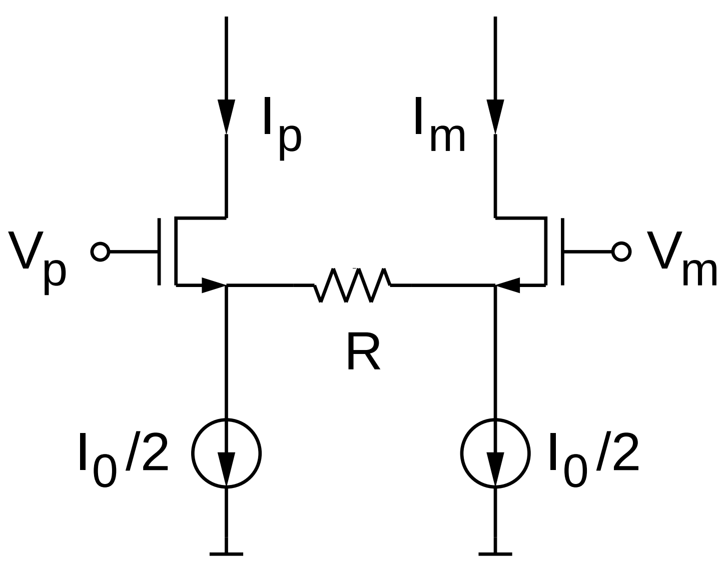
- Transconductor architecture.

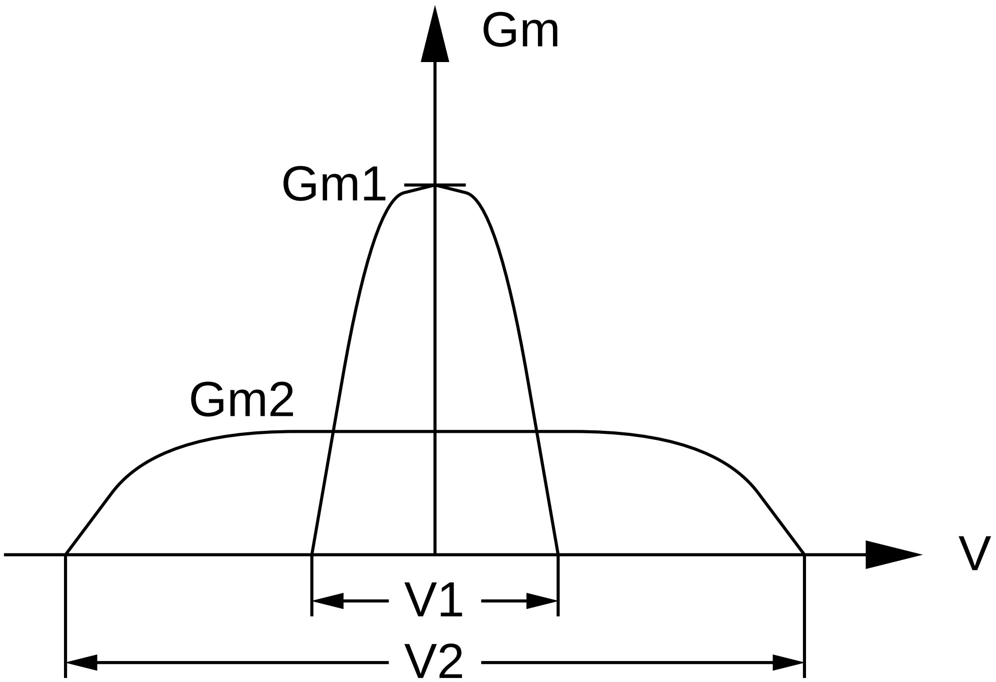
Transconductor F.O.M. : $\Gamma_m = \frac{\beta V_{IP3}^2}{\epsilon}$

β	G_m/P_D.
V_{IP3}^2	Voltage IIP3.
ϵ	Noise factor.

FILTER: PROBLEMS WITH CLASS-A

Class-A transconductors trade G_m for linearity.

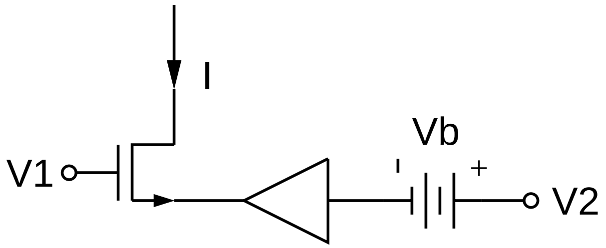




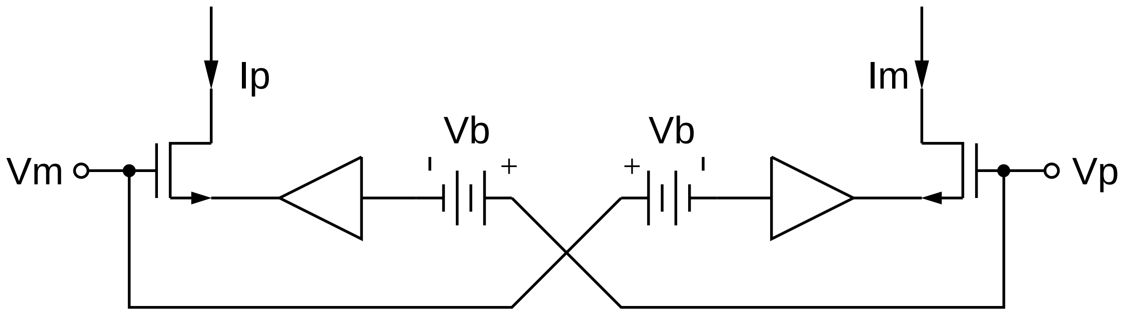
$$G_{m1} V_1 = G_{m2} V_2 \propto I_0$$

FILTER: A SQUARE-LAW TRANSCONDUCTOR.

Square-law
half transconductor.



Linear full transconductor.

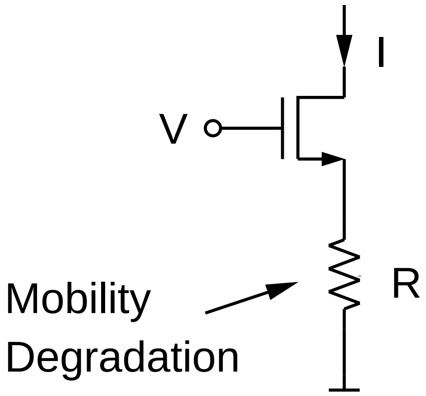


Problems:

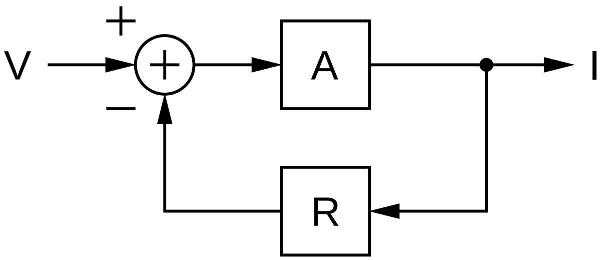
- Velocity saturation. → Use longer L.
- Vertical-field mobility degradation.

FILTER: MOBILITY DEGRADATION

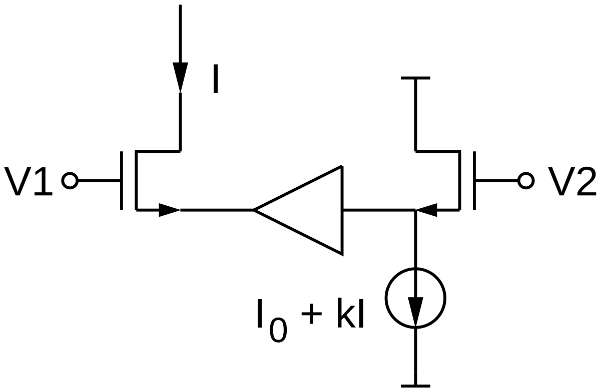
Equivalent circuit.



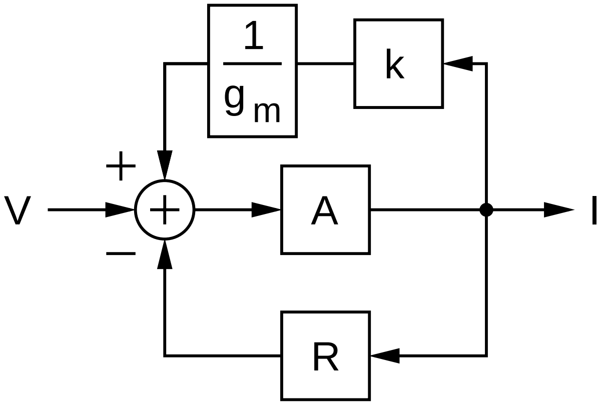
Equivalent system.



With PFB.

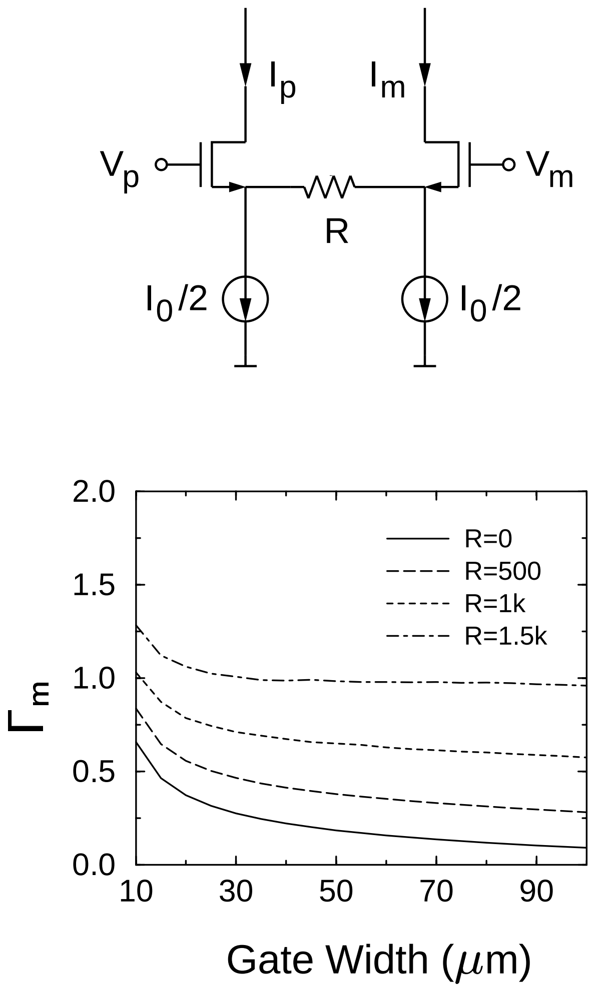


With PFB.

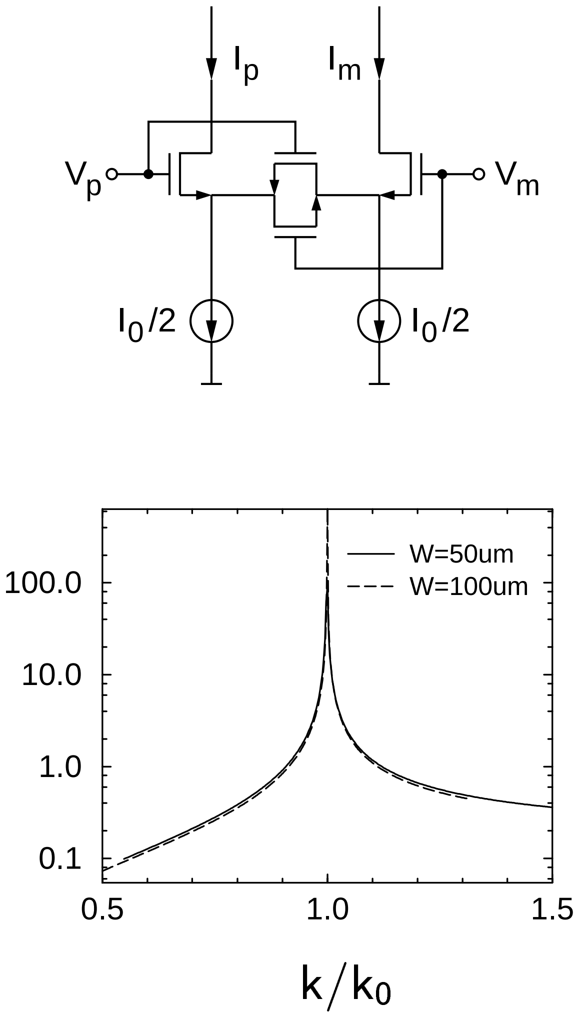


FILTER: TRANSCONDUCTOR SURVEY

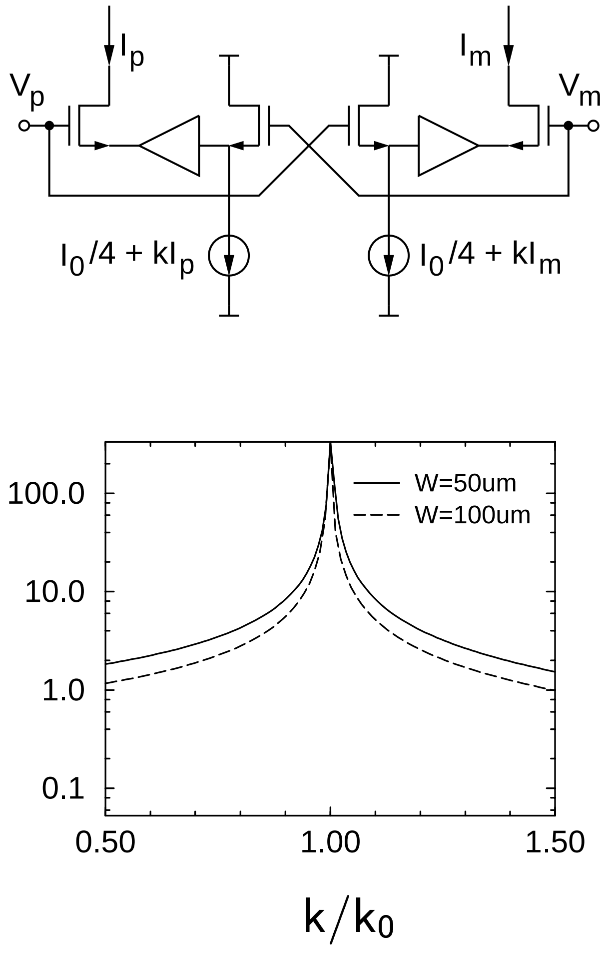
Differential Pair



MOS-Degenerated Pair



PFB Pair



FILTER: SUMMARY

- The active filter is the dynamic-range bottleneck.
  - Noise figure is independent of power consumption.
  - Minimize the filter impedance level to increase dynamic range.
  - Minimize the order and Q of the filter.
- Transconductor architecture figure of merit Γ_m.
  - Power-efficiency, β.
  - Noise factor, ϵ.
  - Linearity, V_{IP3}.
- Results: 60dB SFDR, 10mW power consumption, enabled by new transconductor architecture.

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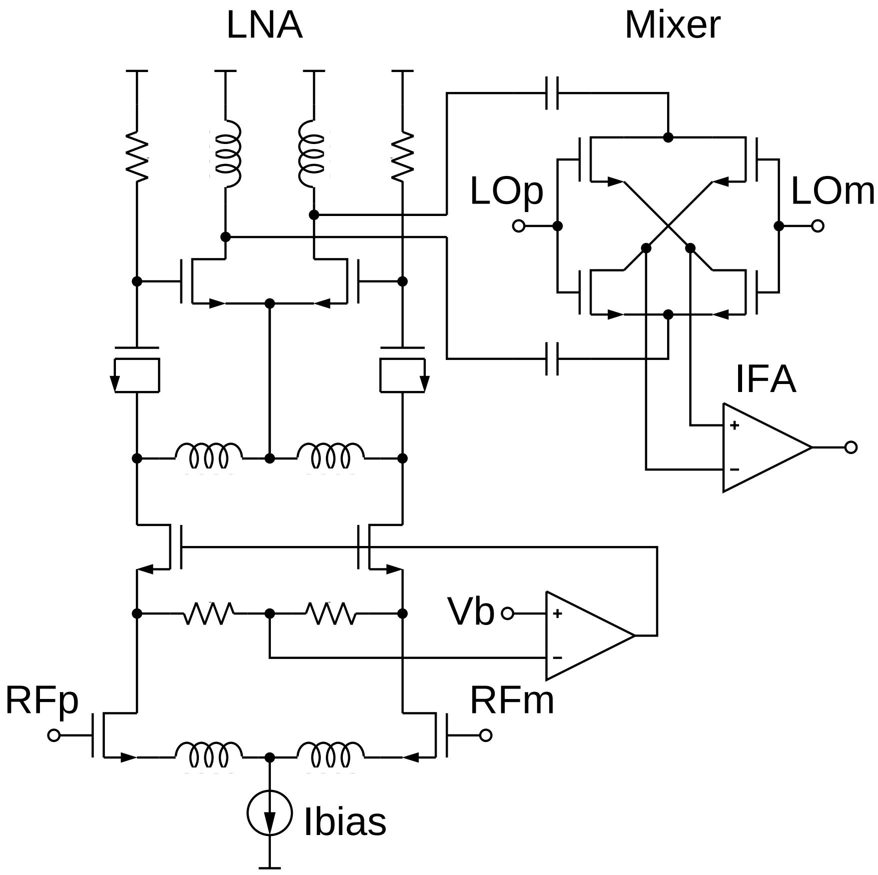
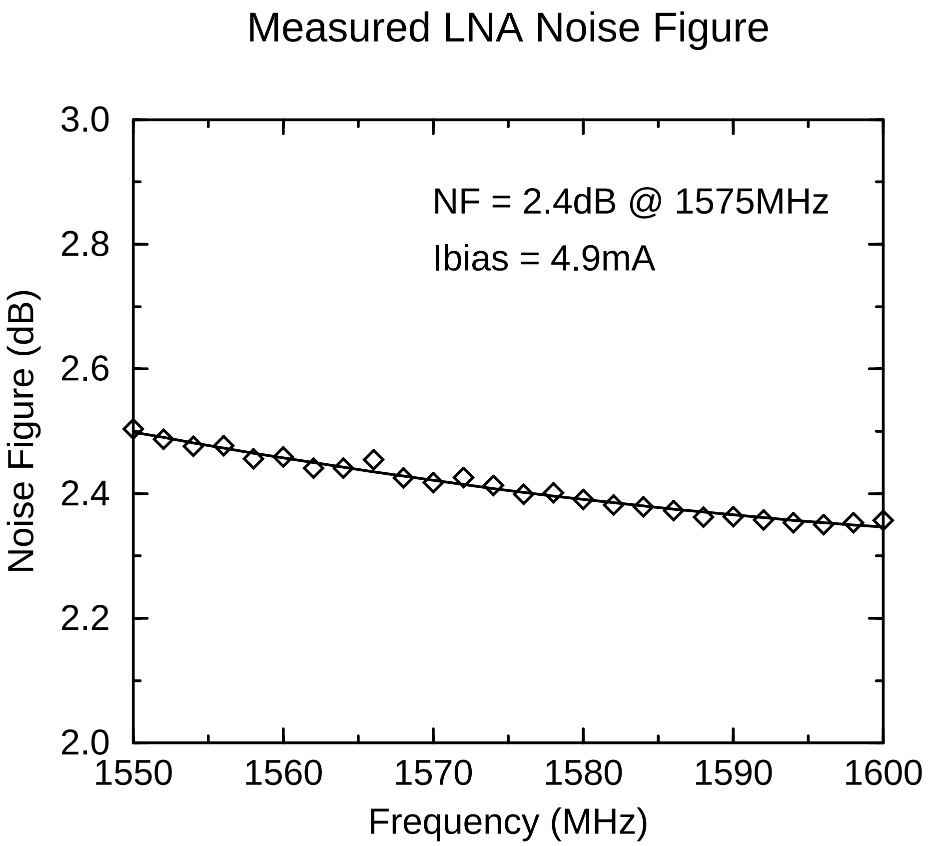
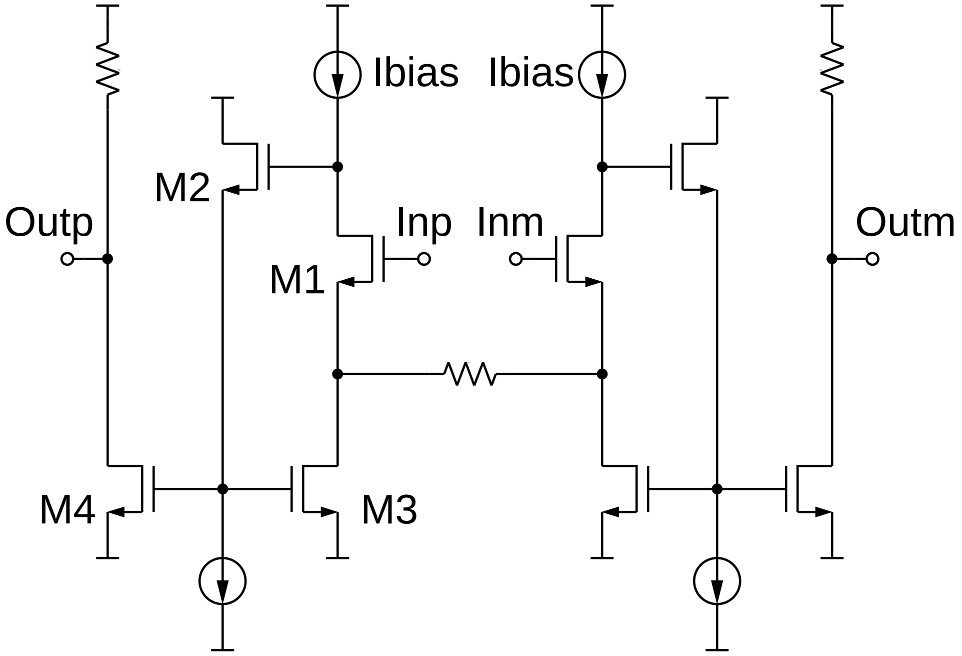
IMPLEMENTATION: LNA / MIXER



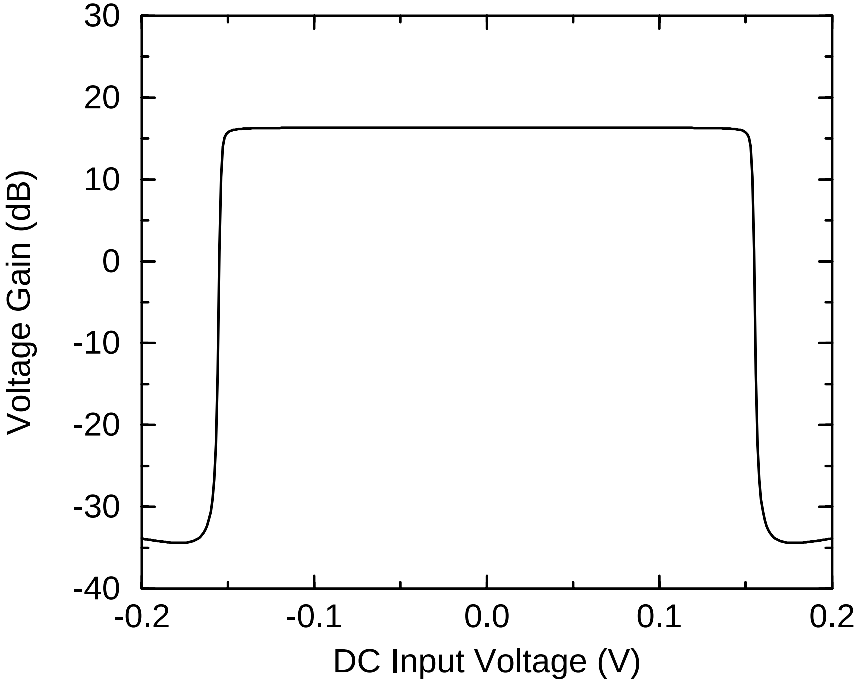

Measured LNA Noise Figure

Shahani, Shaeffer and Lee, ”A 12mW Wide Dynamic Range CMOS GPS Receiver”, ISSCC 97

IMPLEMENTATION: IFA

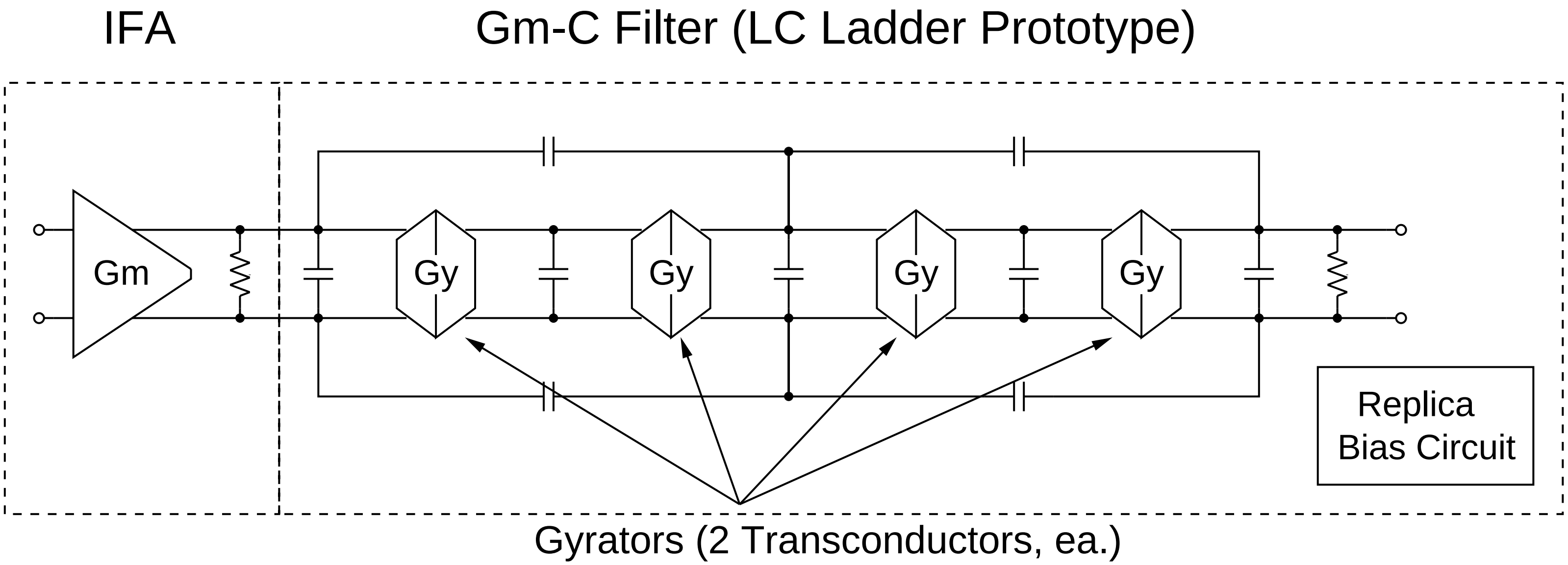


Simulated IFA Voltage Gain



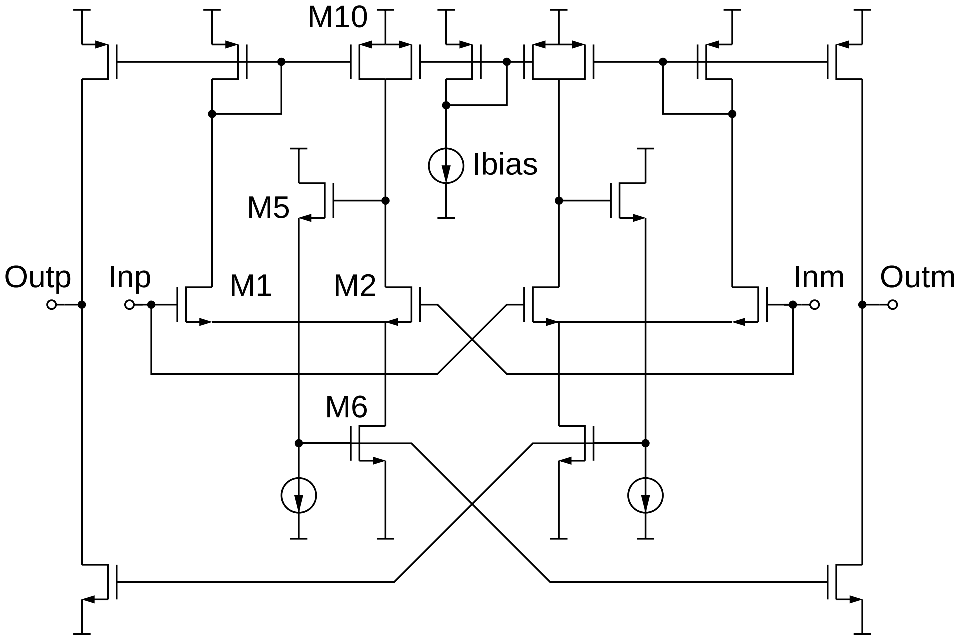
- Low input capacitance, high linearity.
- Load resistors terminate the active filter input.

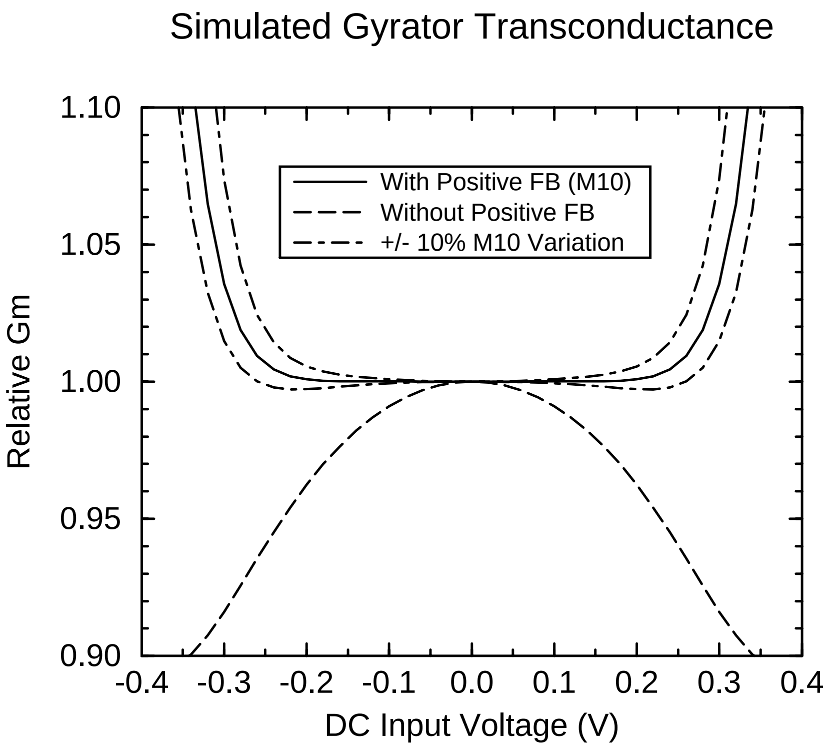
IMPLEMENTATION: GM-C FILTER ARCHITECTURE



- Design based on a 5th-order LC elliptical prototype.
- The dynamic-range limiting block in the system.

IMPLEMENTATION: GM-C FILTER TRANSCONDUCTOR





Use two *square-law* transconductors to build a *linear*, class-AB transconductor.
A little positive feedback (M10) compensates for mobility degradation in M1.

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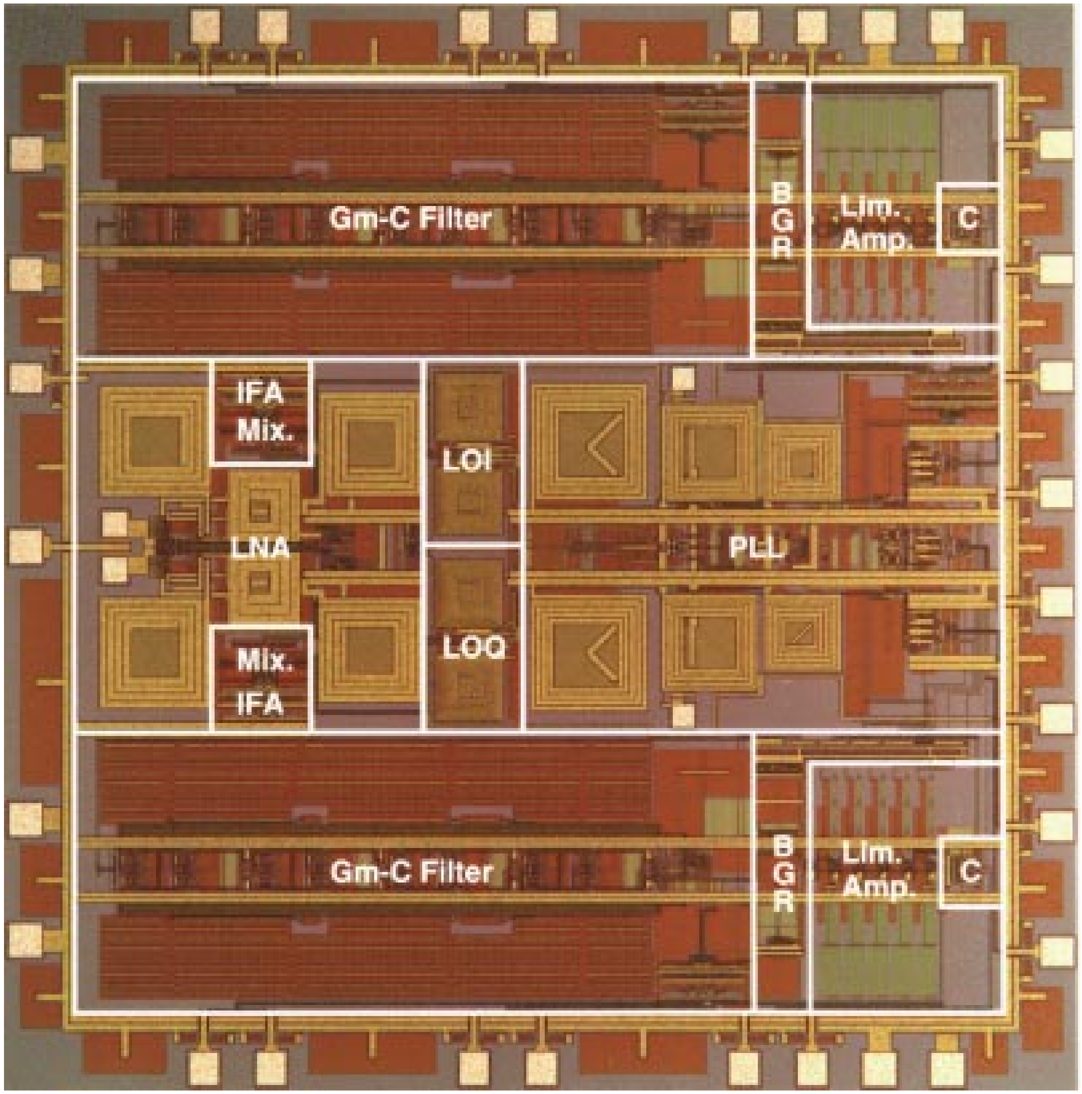
EXPERIMENTAL RESULTS: DIE PHOTO

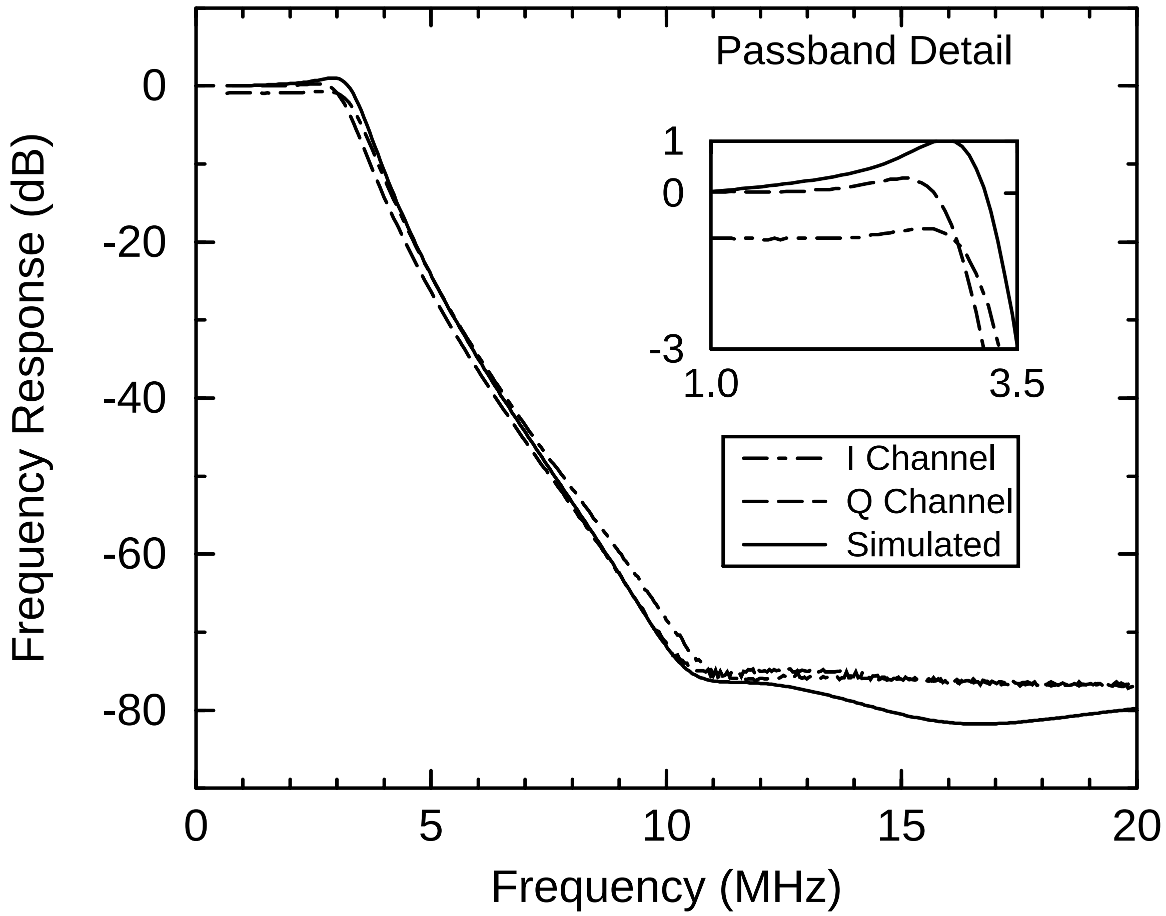
A 115mW CMOS GPS receiver

- 11.2mm^2 die area.
- 0.5μm CMOS technology.
- Polysilicon salicide block.
- Metal/poly capacitors.
- 16 spiral inductors w/ patterned ground shields. Avg. # turns = 5.5
- 1.2nF on-chip supply decoupling cap.

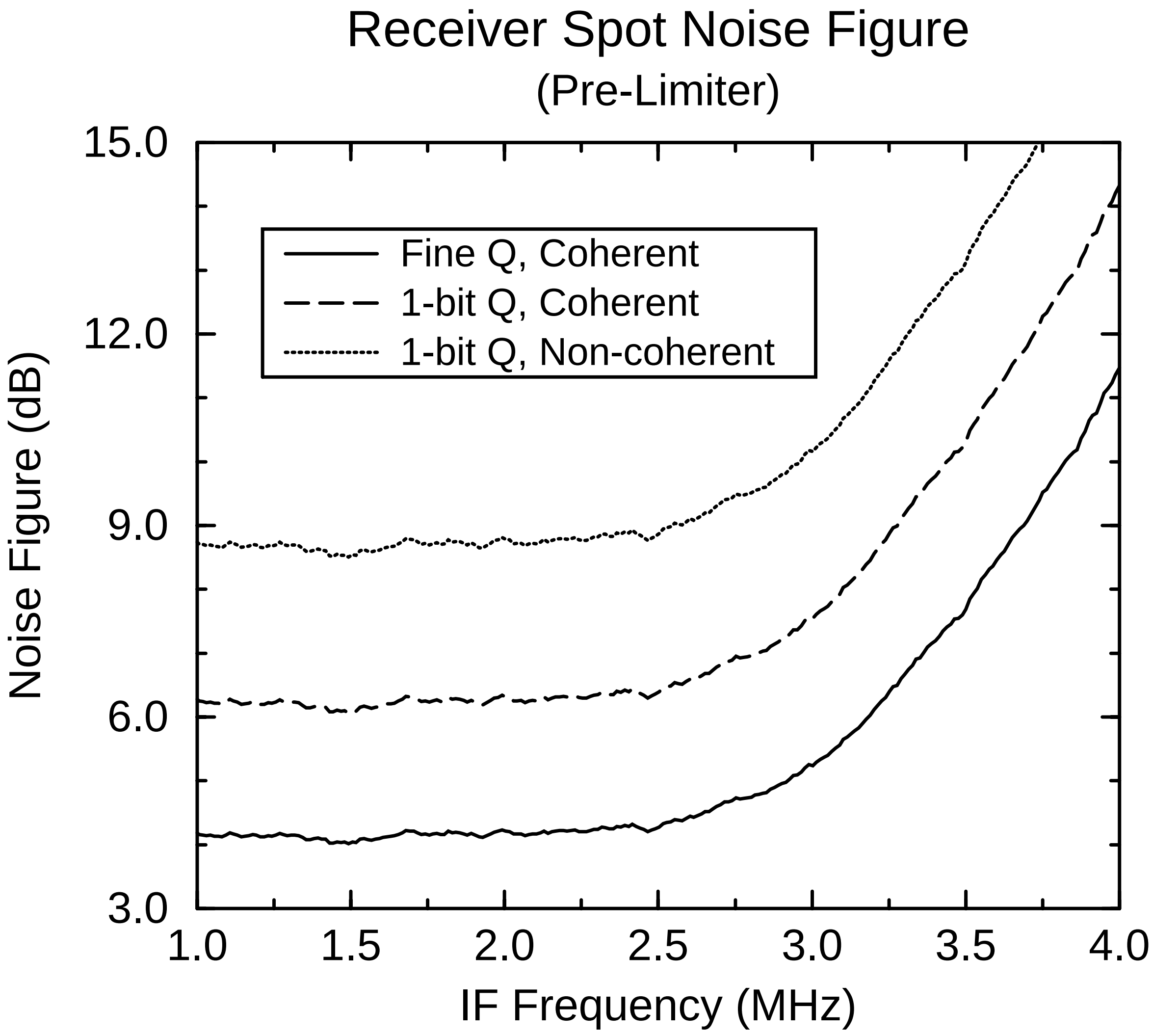


EXPERIMENTAL RESULTS: FREQUENCY RESPONSE

Signal Path Frequency Response

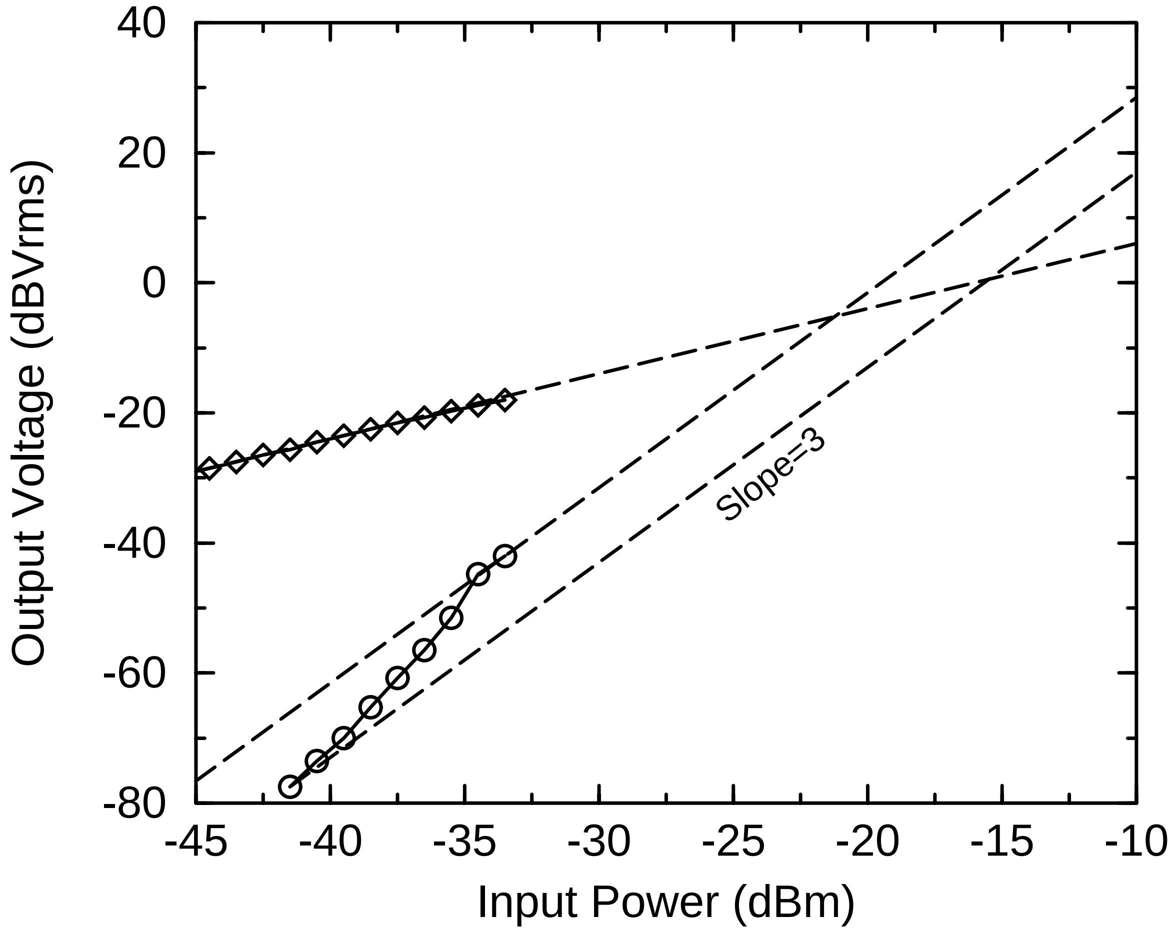


EXPERIMENTAL RESULTS: NOISE FIGURE

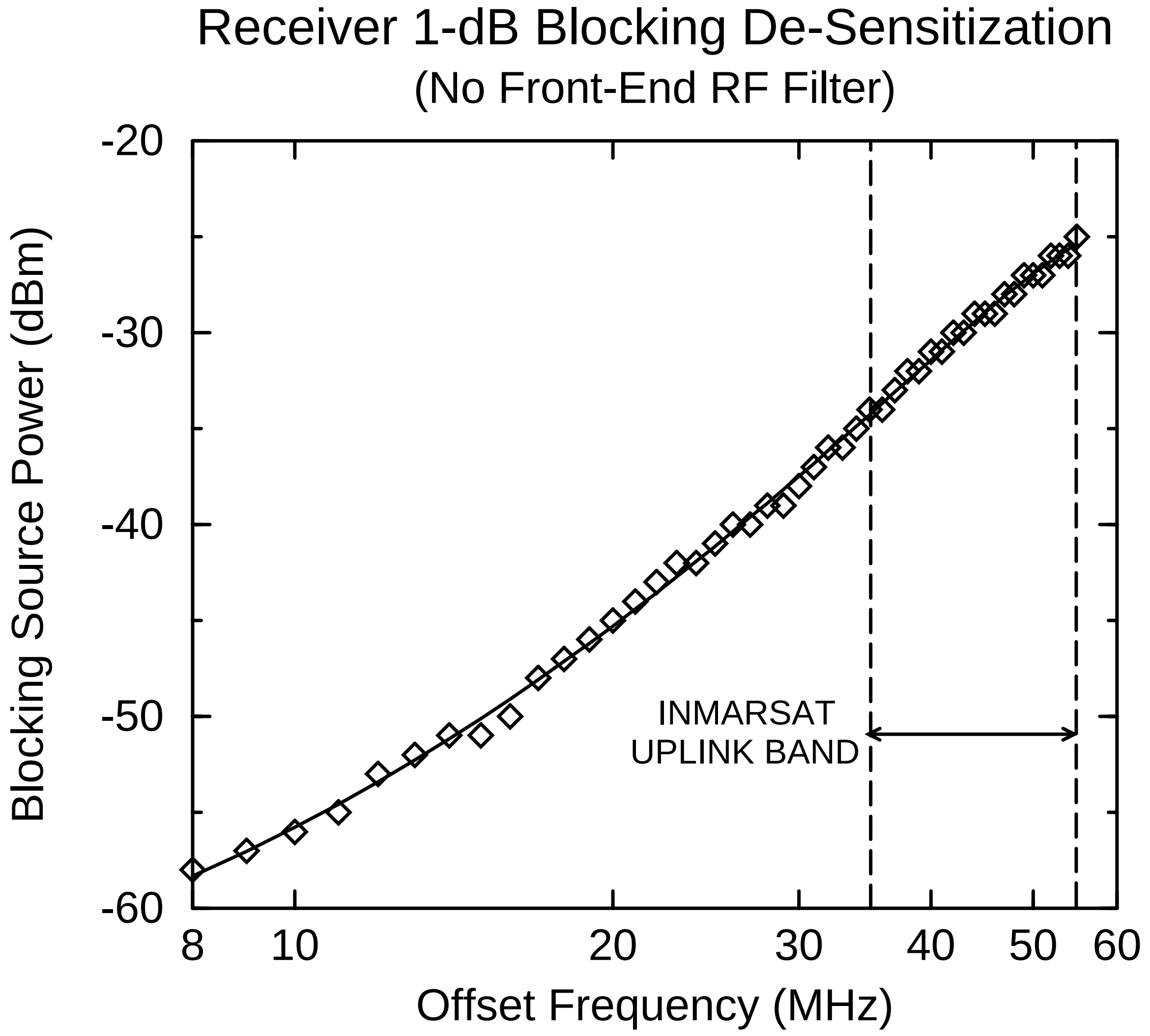


EXPERIMENTAL RESULTS: LINEARITY

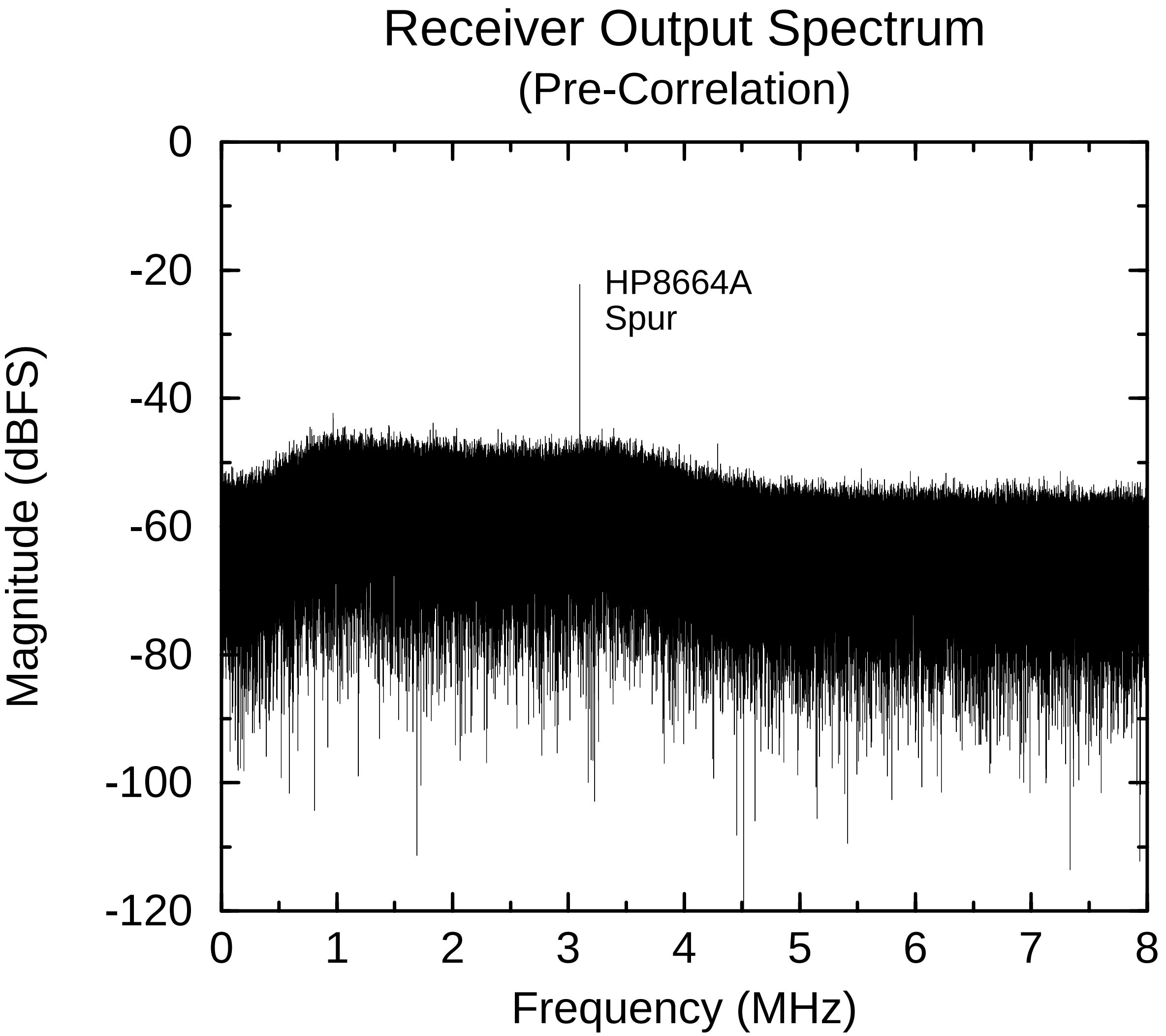
Signal Path 3rd Order Intermodulation



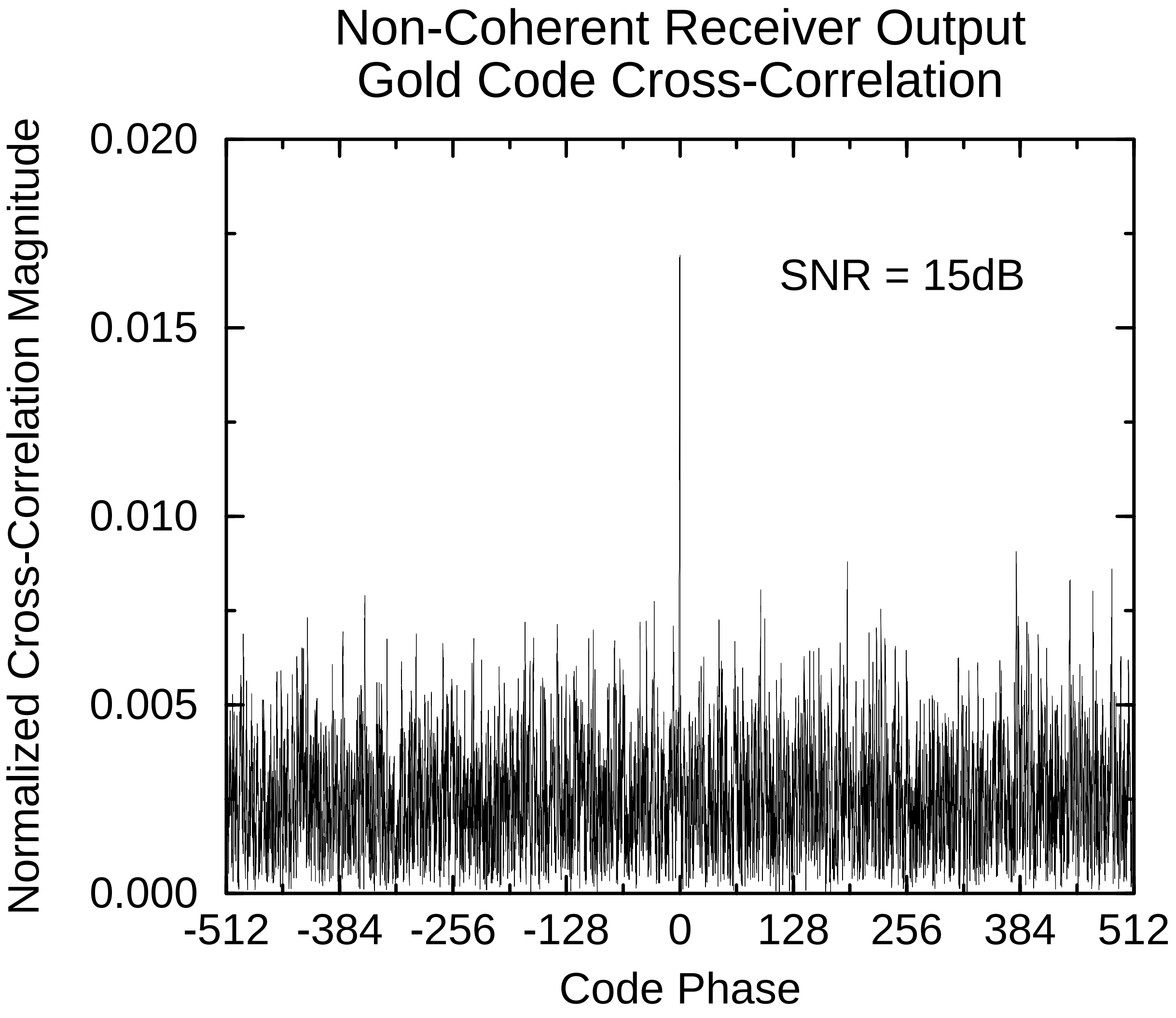
EXPERIMENTAL RESULTS: BLOCKING PERFORMANCE



EXPERIMENTAL RESULTS: 1-BIT OUTPUT SPECTRUM



EXPERIMENTAL RESULTS: CODE CORRELATION



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PERFORMANCE SUMMARY

Signal Path Performance		*PLL Performance*	
LNA Noise Figure	2.4dB	Loop Bandwidth	5MHz
LNA S11	$\leq$ -15dB	Spurious Tones	$\leq$ -42dBc
Coherent Receiver NF	4.1dB	VCO Tuning Range	240MHz ($\pm$ 7.6%)
IIP3 (Filter-limited)	-16dBm @ -43dBm P_s	VCO Gain Constant	240MHz/V
Peak SFDR	60dB	LO Leakage @ LNA	$<$ -53dBm
Filter Cutoff Freq.	3.5MHz		
Filter PB Peaking	$\leq$ 1dB	*Power/Technology*	
Filter SB Atten.	$\geq$ 52dB @ 8MHz	Signal Path	79mW
	$\geq$ 68dB @ 10MHz	PLL / VCO	36mW
Pre-Filter G_p	19dB	Supply Voltage	2.5V
Pre-Filter A_v	32dB		
Total G_p	$\approx$ 94dB	Die Area	11.2mm^2
Total A_v	$\approx$ 122dB	Technology	0.5μm CMOS
Non-Coherent Output SNR	15dB		

CONTRIBUTIONS

- CMOS LNAs:
  - Theoretical investigation of induced gate noise.
  - Power-constrained noise figure optimization technique.
  - CMOS LNA with 2.4dB noise figure at 1.6GHz on 12mW P_D.
- CMOS Active Filters:
  - Theoretical SFDR investigation, transconductor F.O.M., Γ_m.
  - New transconductor architecture with high Γ_m.
  - CMOS filter with 60dB SFDR at 3MHz on 10mW P_D.
- First CMOS GPS Receiver:
  - Developed a new GPS receiver architecture.
  - High performance, highly integrated, low P_D of 115mW.

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