Radio-Frequency Conversion and Synthesis
(for a 115mW GPS Receiver)

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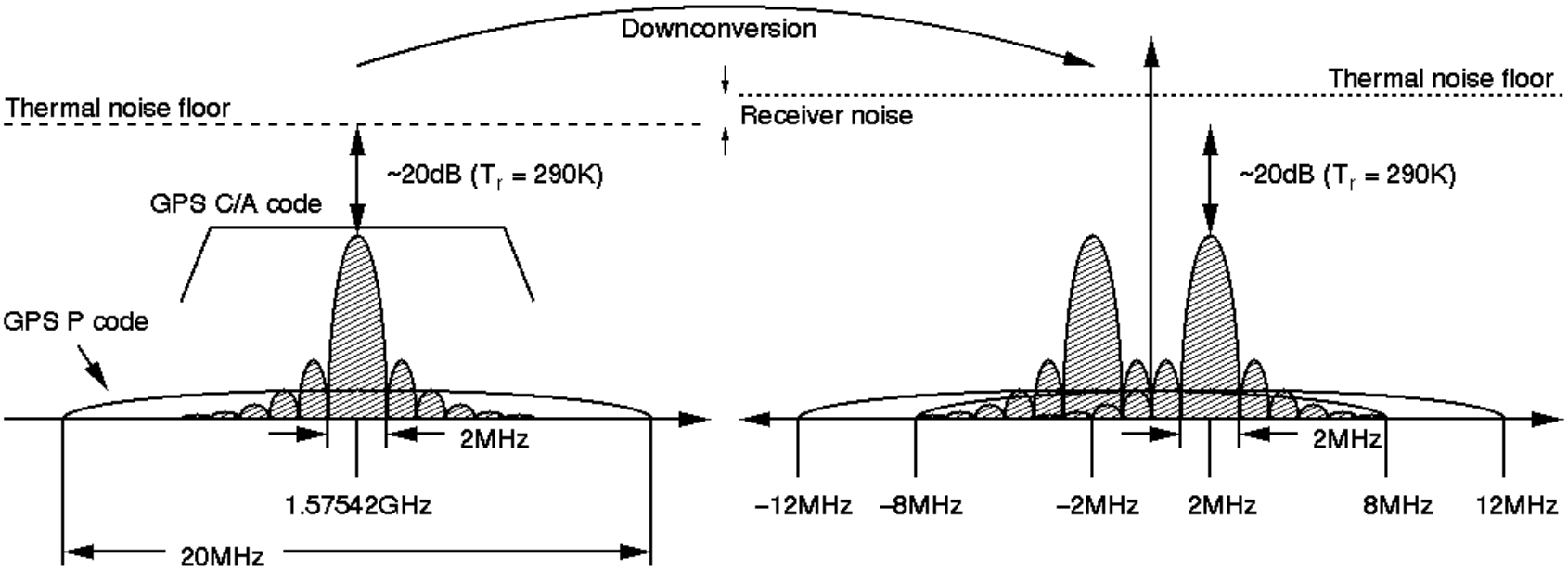
Overview

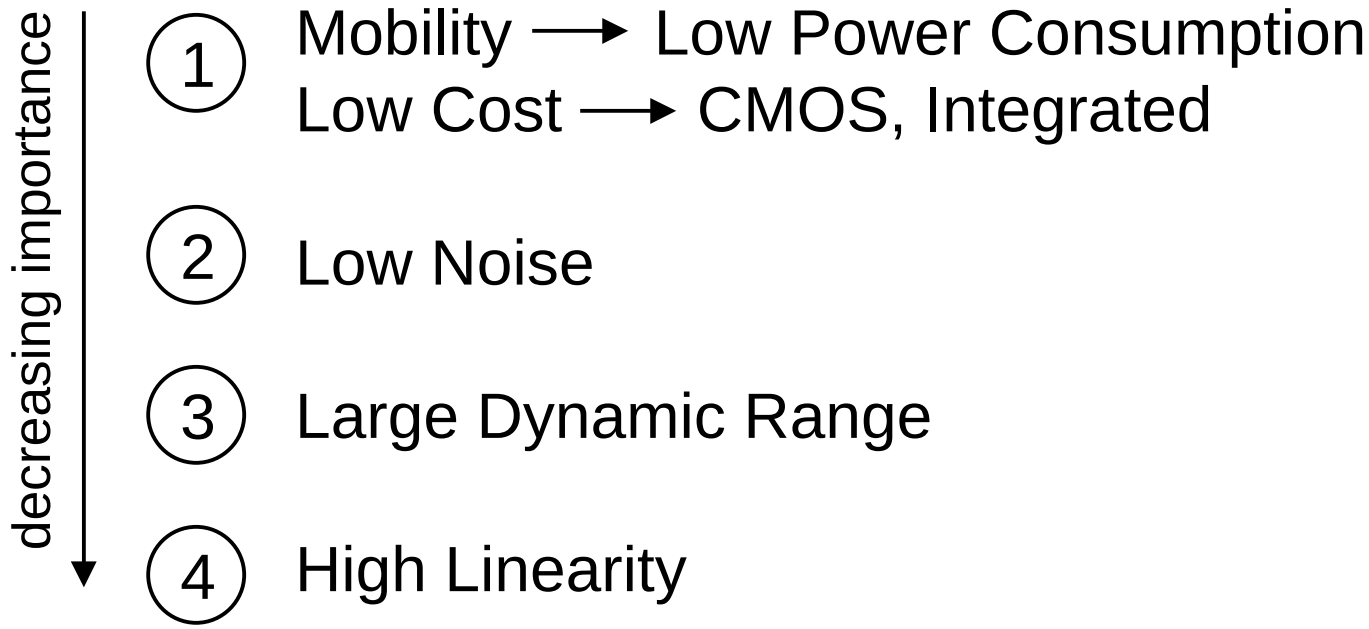
- GPS Overview
- Frequency Conversion
- Frequency Synthesis
- Conclusion

GPS Overview: Signal Structure

- Carrier frequency = 1.57542GHz
- Signal is below the noise floor at the antenna ($P_S \approx$ -130dBm, $P_N \approx$ -110dBm)
- Large processing gain (GPS data bit, T_b = 20ms; C/A code chip, $T_c \approx$ 1μs $\longrightarrow$ $G_P \approx$ 43dB)



GPS Overview: Receiver Requirements



After power, the receiver's noise figure is most important!
(not linearity or dynamic range) ⟶ must have an LNA

GPS Overview: Commercial Receivers

	Sony	GEC Plessey GP2010	SiRF GRF-1
Power	81mW (3V)	200mW (3V)	500mW (5V)
Chip NF	6.1dB	10dB	
Technology	15GHz Bipolar	Bipolar	
Missing	LNA, 2 Filters, PLL LF	LNA, 2 Filters, PLL LF	LNA, Filter

Frequency Conversion

- Performance Metrics
- Architectures
- Double-Balanced Passive CMOS Mixer

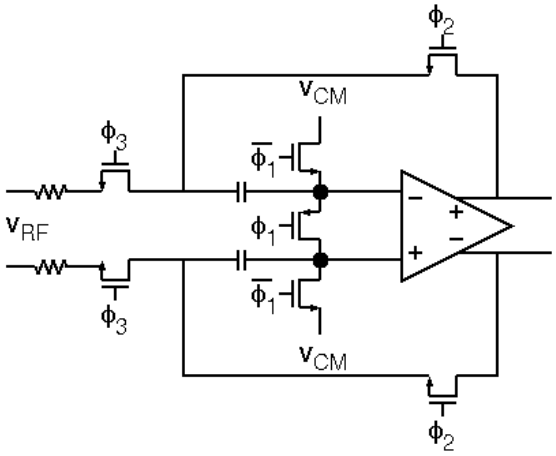
  (with capacitive load)
- Die Photos + Measurement Results

Frequency Conversion: Performance Metrics

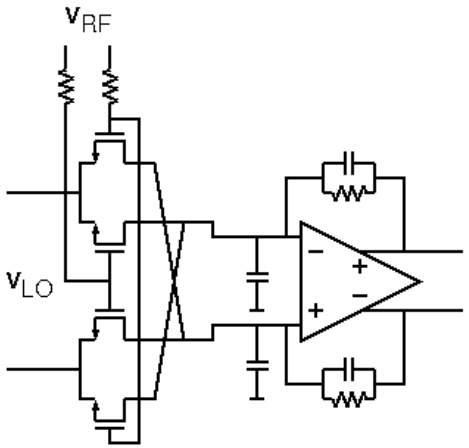
- Power
  - Most important parameter in architecture choice
- Noise Figure
  - LNA relaxes the maximum tolerable noise figure
- Linearity
  - Mixer should not be the limiting block for dynamic range
- Conversion Gain
  - Less important due to the presence of an LNA

Frequency Conversion: Architectures

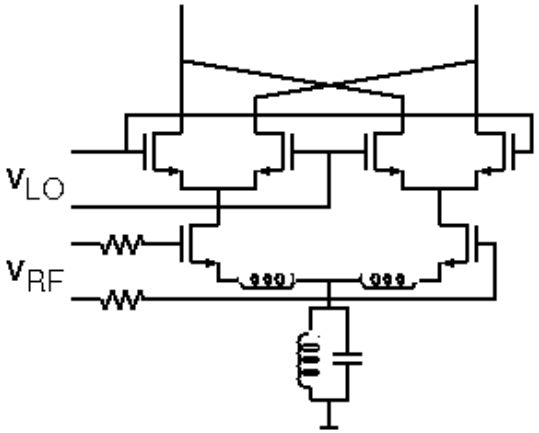
Subsampling Mixer



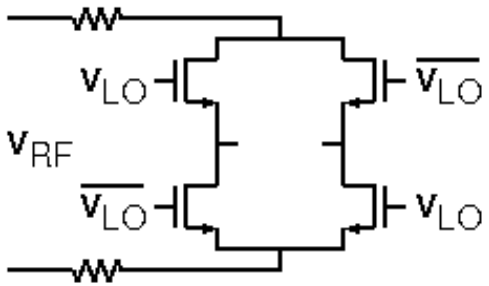
Potentiometric Mixer



Gilbert-Type Mixer



Passive Mixer



Frequency Conversion: Architectures

Subsampling Mixer

Power	41mW (3.3V)
Noise Figure	47dB
IIP3	-16dBm
Voltage Conversion Gain	36dB
Technology	0.6μm BiCMOS
Die Area	3.6mm^2

- Noise figure and power consumption are too large
- Extraordinary demands are placed on the phase noise of the sampling clock

D.H. Shen, C. Hwang, B.B. Lusignan, and B.A. Wooley, “A 900-MHz RF front-end with integrated discrete-time filtering,” *IEEE J. Solid-State Circuits*, vol. 31, pp. 1945-1954, Dec. 1996.

Frequency Conversion: Architectures

Potentiometric Mixer

Power	1.3mW (5V)
Noise Figure	32dB
IIP3	45.2dBm
Voltage Conversion Gain	18dB (12dBm LO)
Technology	1.2μm CMOS
Die Area	$1mm^2$

- Noise figure is too large
- If preceded by a 2nd LNA to improve the noise figure, then the cost is in power, linearity, and area

J. Crols and M. Steyaert, “A 1.5-GHz highly linear CMOS downconversion mixer,” *IEEE J. Solid-State Circuits*, vol. 30, pp. 736-742, July 1995.

Frequency Conversion: Architectures

Gilbert-Type Mixer

Power	7mW (2.7V)
Noise Figure	9.7dB
IIP3	-4.1dBm
Power Conversion Gain	8.8dB
Technology	0.5μm CMOS
Die Area	0.14mm^2

- Main advantage is in the conversion gain, but this costs power and linearity

A.N. Karanicolas, “A 2.7-V 900-MHz CMOS LNA and mixer,” *IEEE J. Solid-State Circuits*, vol. 31, pp. 1939-1944, Dec. 1996.

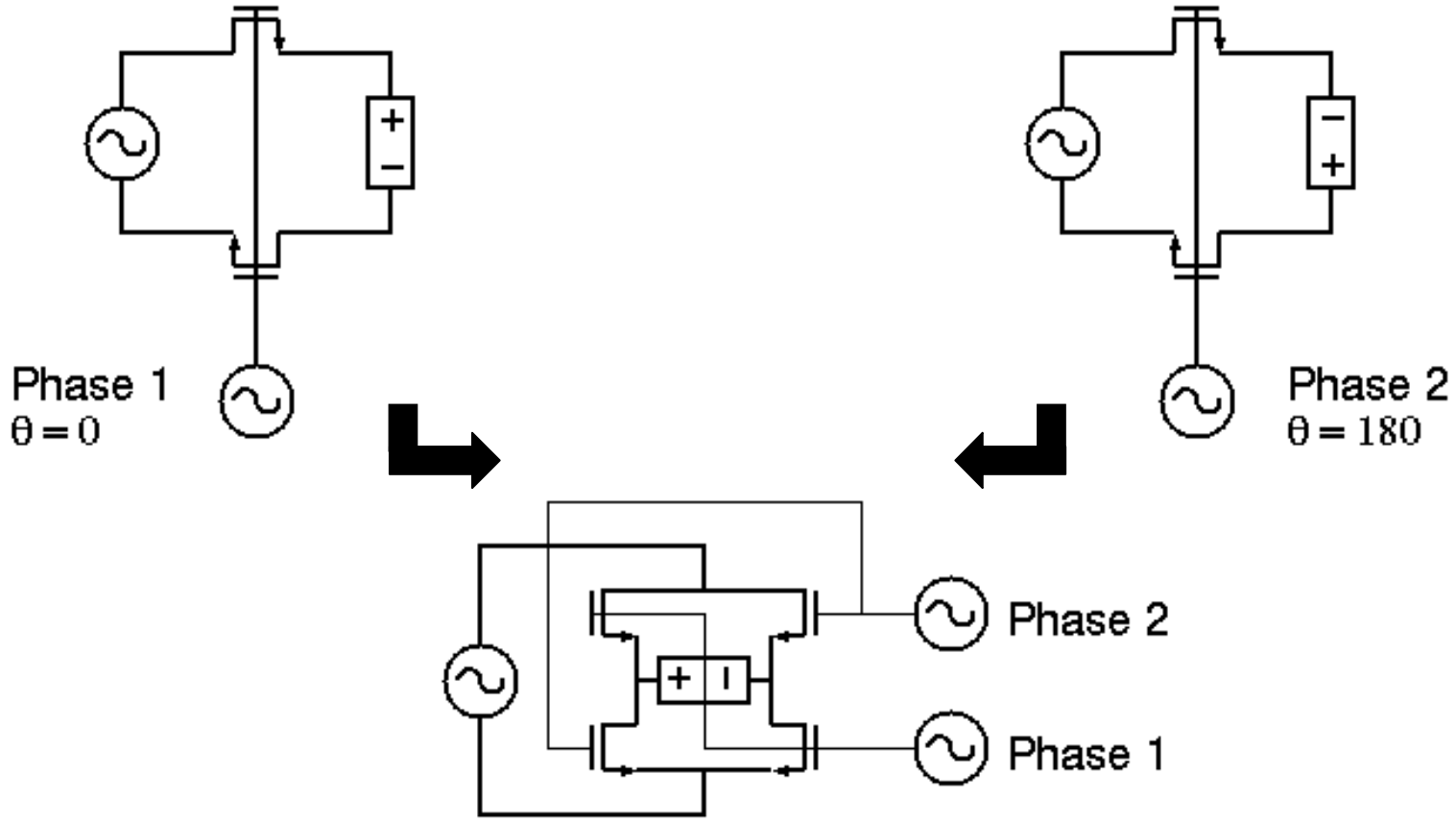
Frequency Conversion: Architectures

Passive Mixer	
Power	< 500μW
Noise Figure	6dB
IIP3	9dBm
Voltage Conversion Gain	-3dB
Technology	0.5μm CMOS
Die Area	pad limited

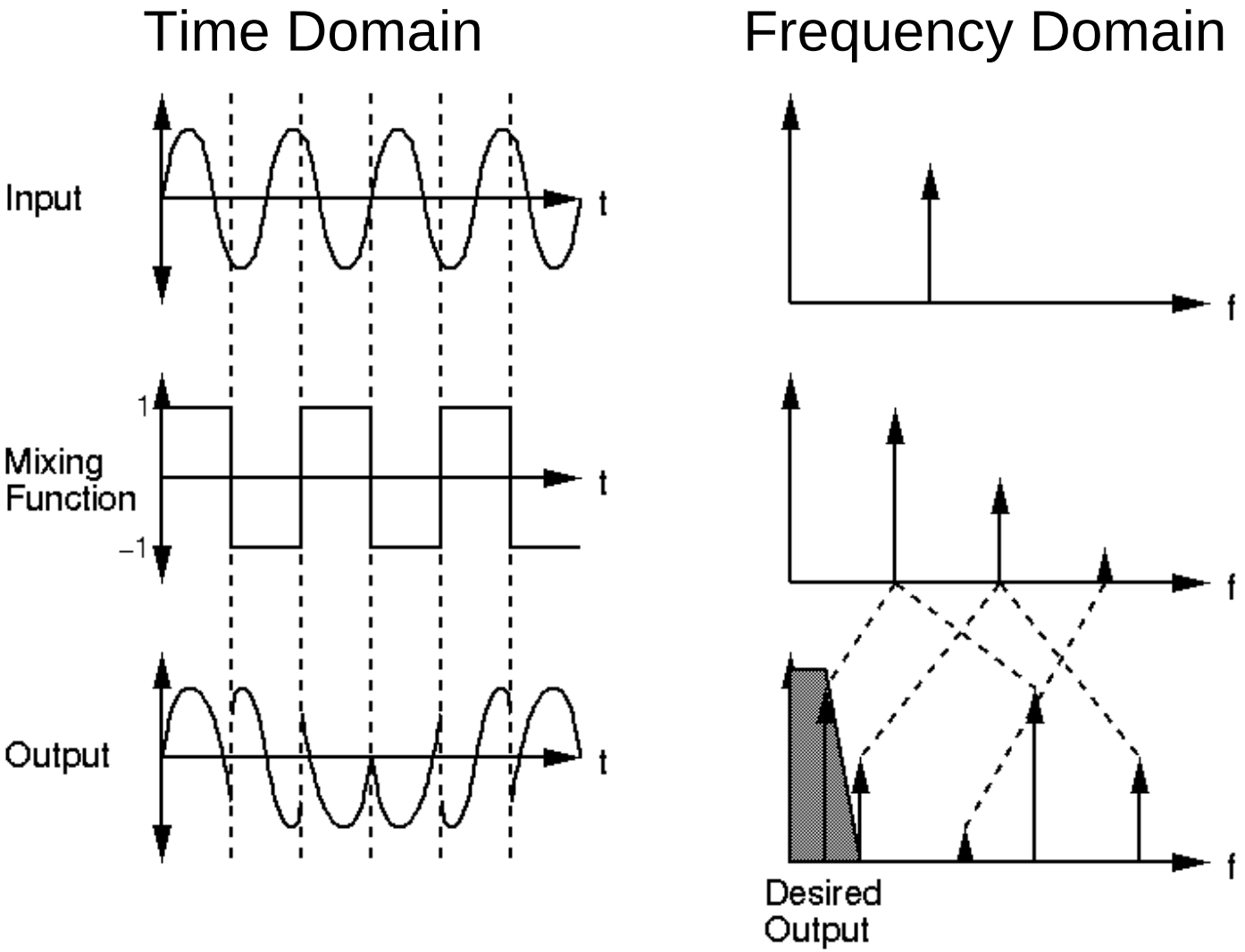
- If gain can be postponed to the IF amplifier, this is the most attractive architecture

Frequency Conversion: Passive CMOS Mixer

CMOS provides good voltage switches when transistors are operated in triode.

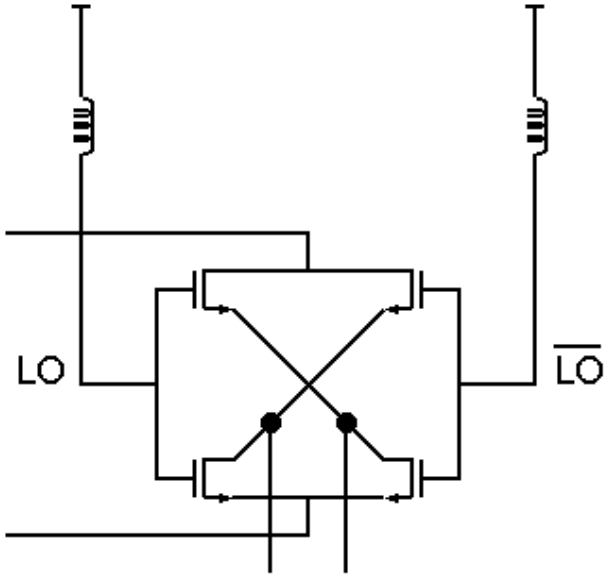


Frequency Conversion: Passive CMOS Mixer



Frequency Conversion: Passive CMOS Mixer

Local oscillator drives the gates which present a capacitive load ($C \propto W\,L$)



So, resonate the load to reduce power consumption

Frequency Conversion: Passive CMOS Mixer

Design Questions

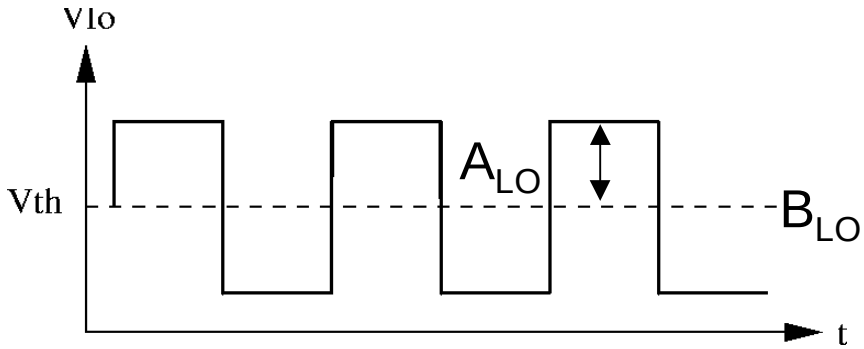
How to select W ?

- W_{max} is set by smallest on-chip spiral inductor
- noise $\propto$ 1 / W
- power $\propto$ W

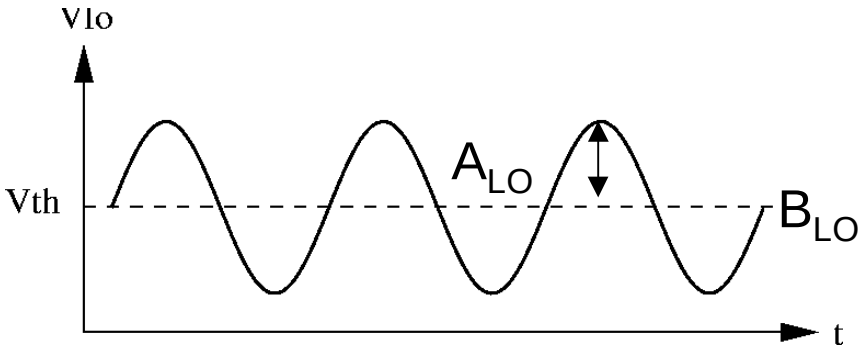
$\longrightarrow$ Decide LO power budget, then pick the inductor to meet this, and solve for W

Since it is necessary to resonate the gate capacitance, the LO drive will be sinusoidal, not square. A study of various sinusoidal drives and their effect on conversion gain is therefore important.

Frequency Conversion: Passive CMOS Mixer

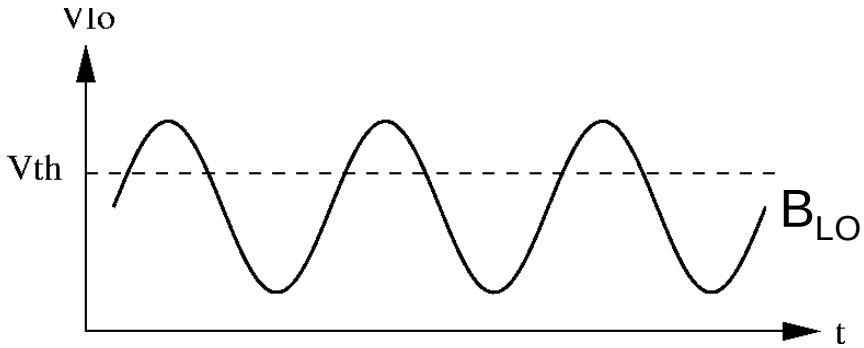


Square Wave Drive



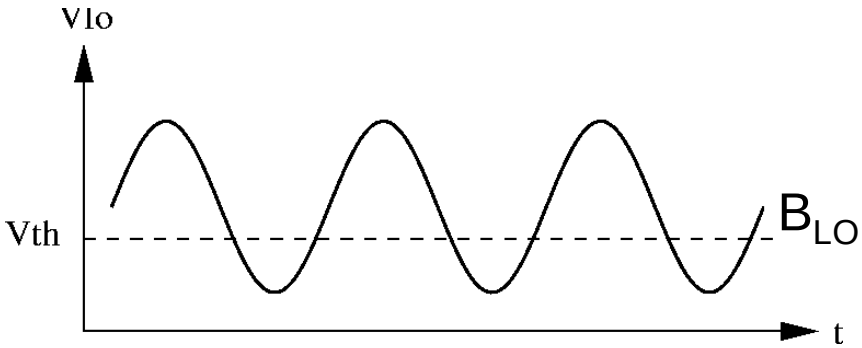
Sine Wave Drive

$B_{LO} = V_{th}$



Break-Before-Make Drive

$B_{LO} < V_{th}$

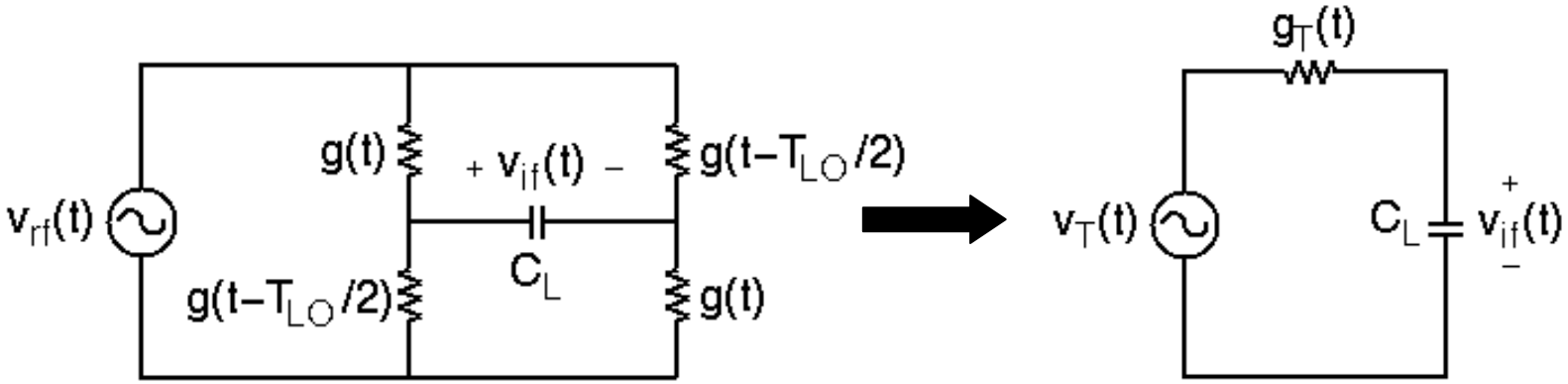


Make-Before-Break Drive

$B_{LO} > V_{th}$

Frequency Conversion: Passive CMOS Mixer

Model switches as time-varying conductances:



$$v_T(t) = \frac{g(t) - g(t - T_{LO}/2)}{g(t) + g(t - T_{LO}/2)} v_{rf}(t) = m(t) v_{rf}(t)$$

$$g_T(t) = \frac{g(t) + g(t - T_{LO}/2)}{2}$$

Frequency Conversion: Passive CMOS Mixer

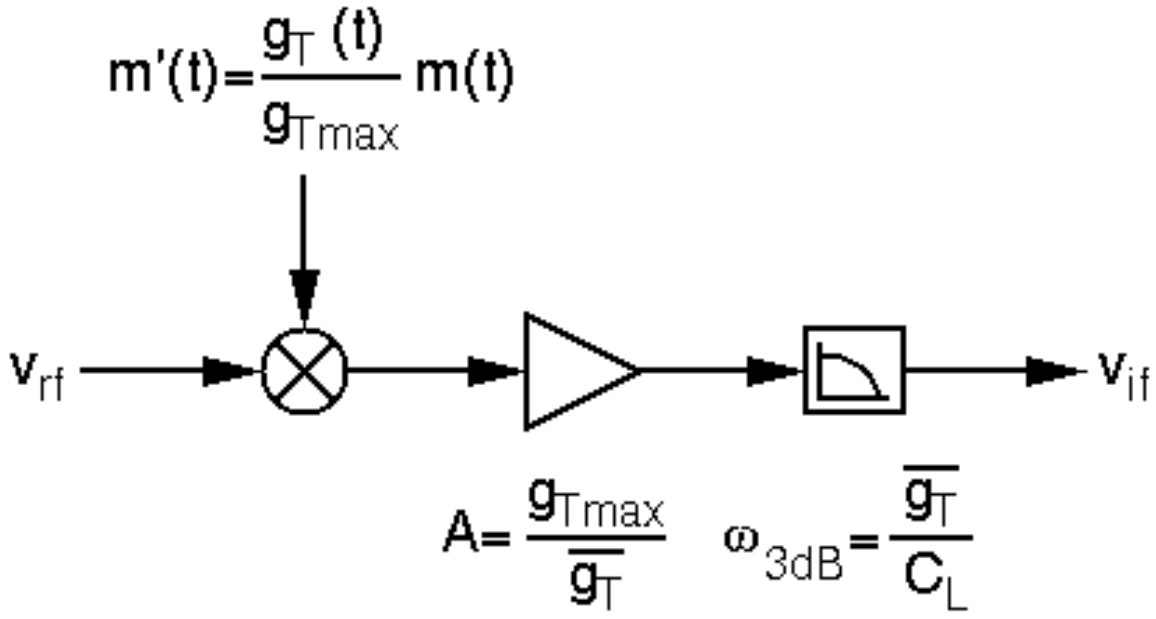
$|M(f_{LO})|$ FOR THE FOUR CASES

Square Wave Drive	$2/\pi$	
Sine Wave Drive	$2/\pi$	
Break-Before-Make	$(2/\pi)\sqrt{1-r^2}$	$0 \le r \le 1$
Make-Before-Break	$\dfrac{\sin^{-1}(r)/r + \sqrt{1-r^2}}{\pi}$	$0 \le r \le 1$
	$1/(2r)$	$1 \le r \le \infty$

$$r = \frac{|V_{th} - B_{LO}|}{A_{LO}}$$

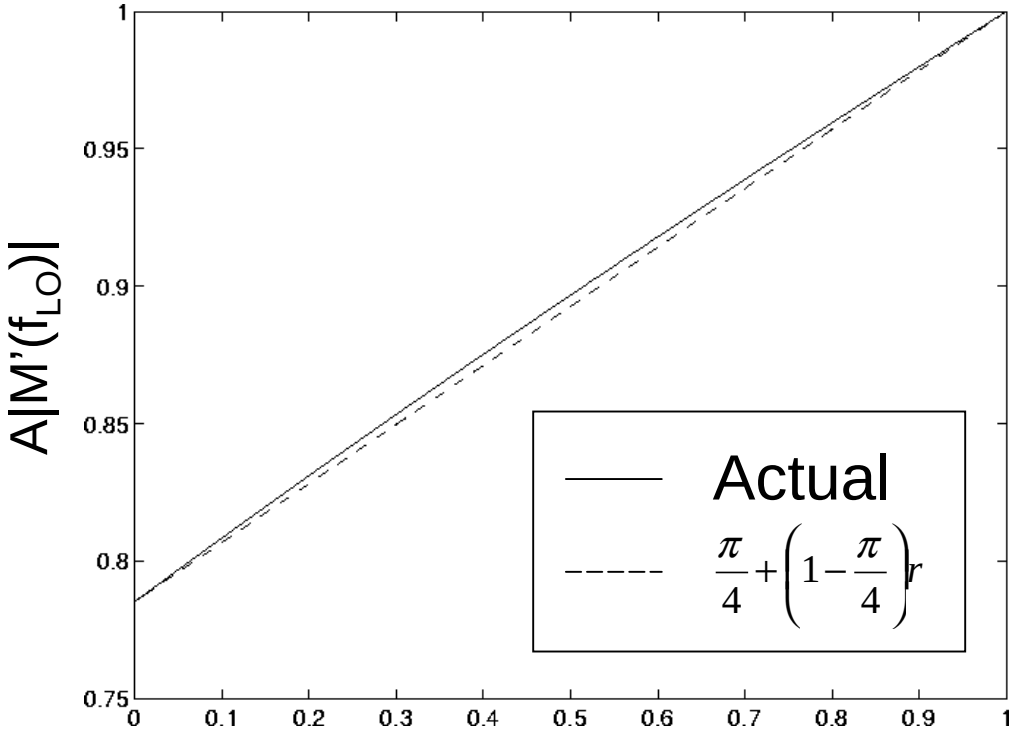
Frequency Conversion: Passive CMOS Mixer

Equivalent system for mixer conversion gain when $\overline{g_T} / C_L << 2\omega_{LO}$:

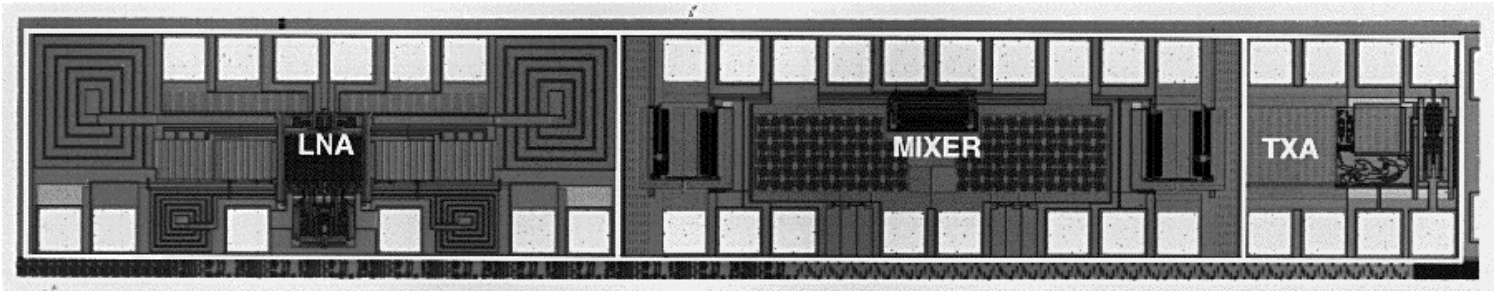


Frequency Conversion: Passive CMOS Mixer

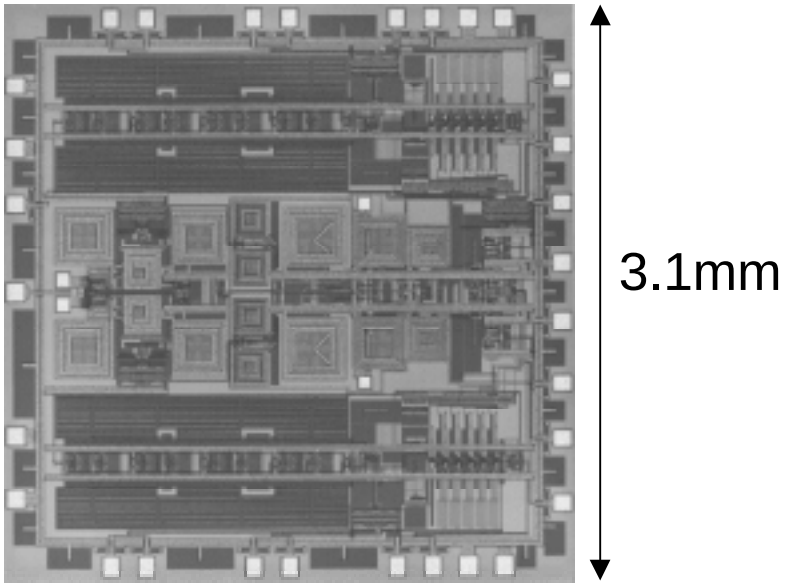
For a break-before-make sinusoidal drive, the conversion gain can approach unity.



Frequency Conversion: Die Photos

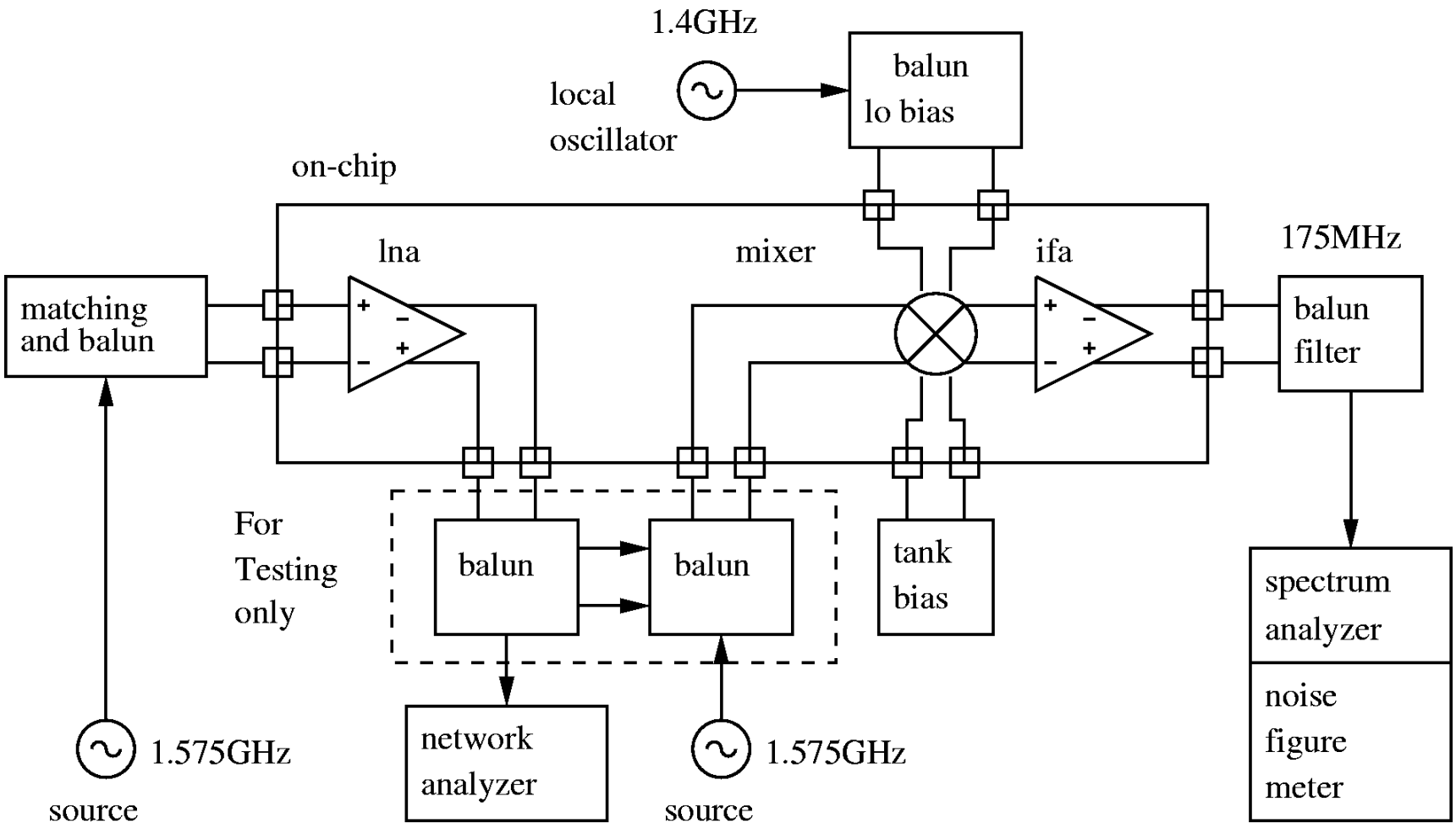


Fastlane: 0.35μm CMOS (0.84mm^2)

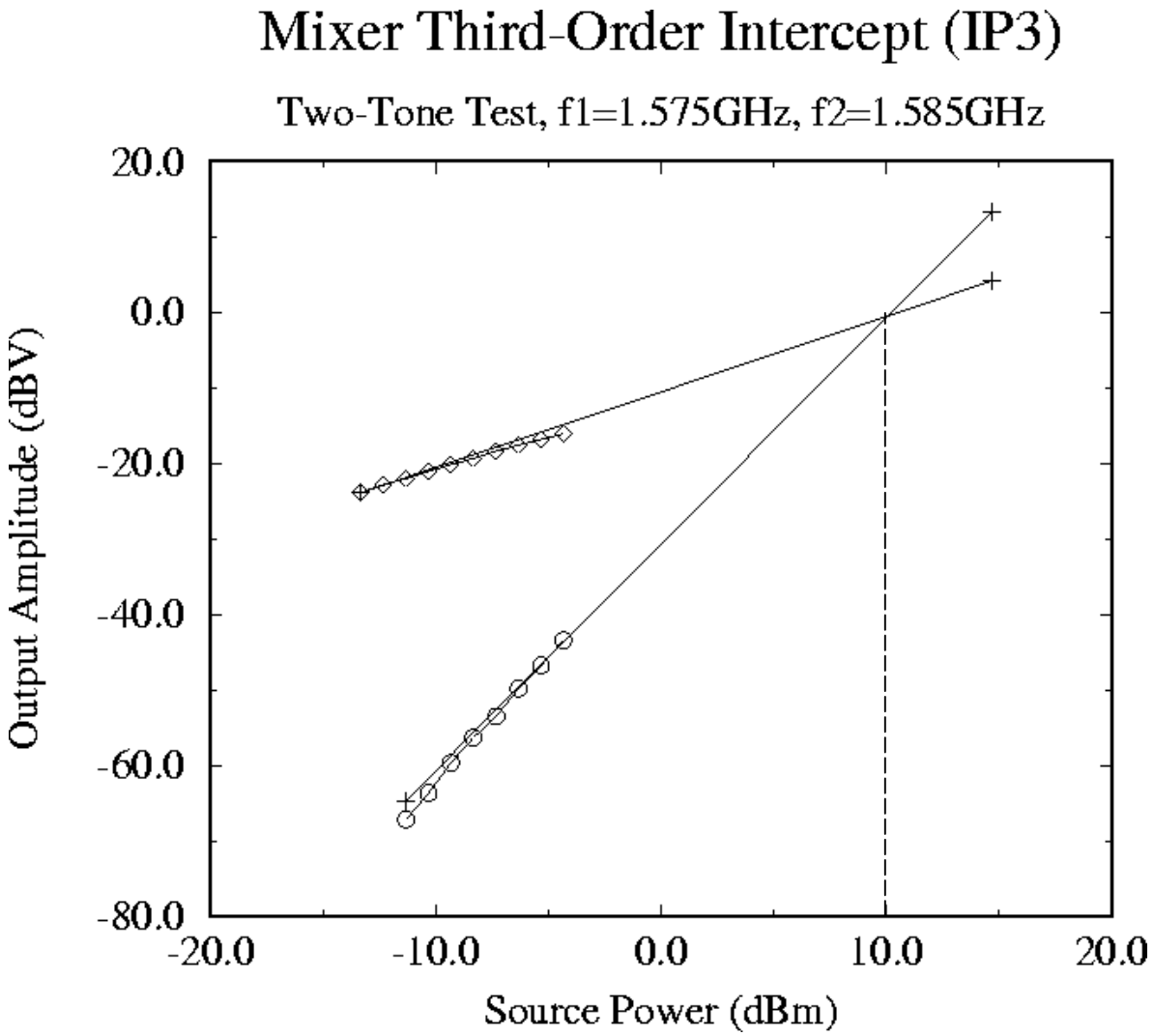


Waldo: 0.5μm CMOS (0.0084mm^2)

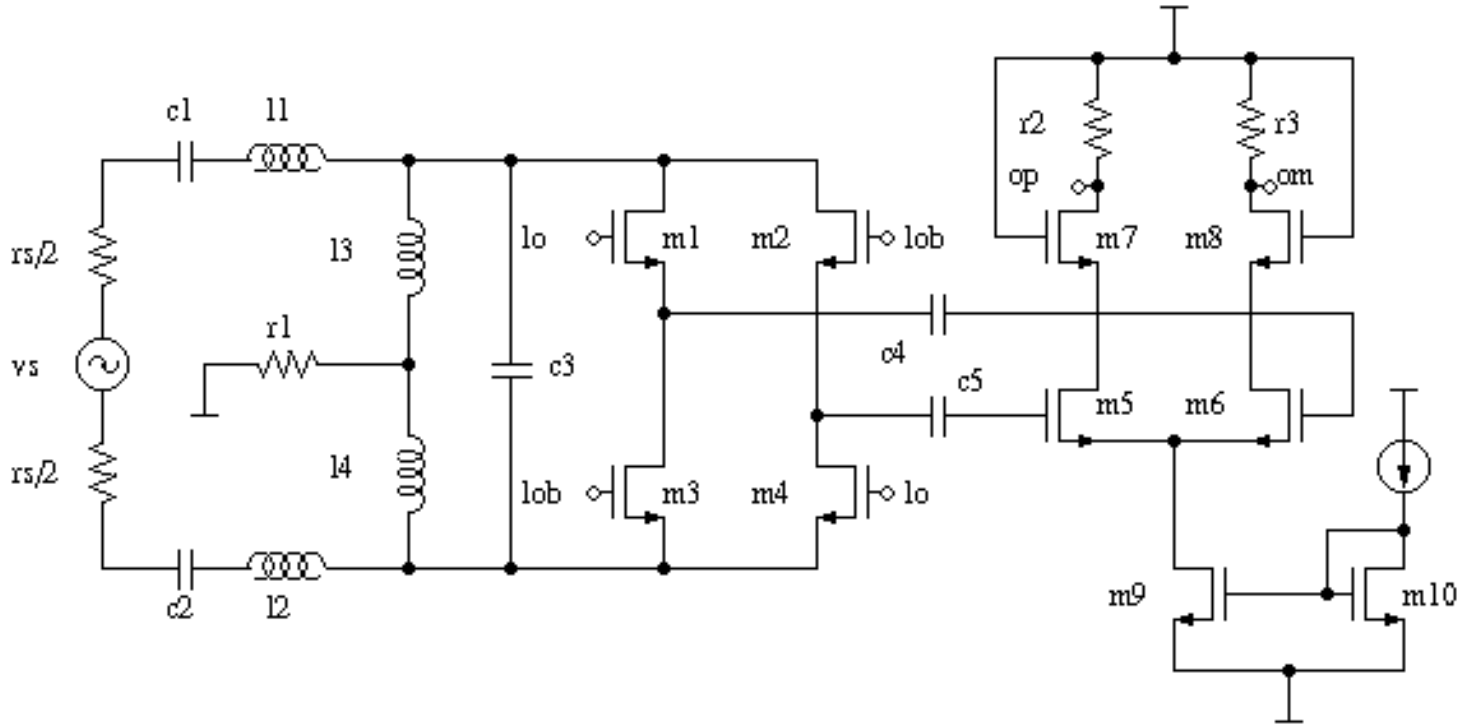
Frequency Conversion: Measurement Results



Frequency Conversion: Measurement Results



Frequency Conversion: Measurement Results

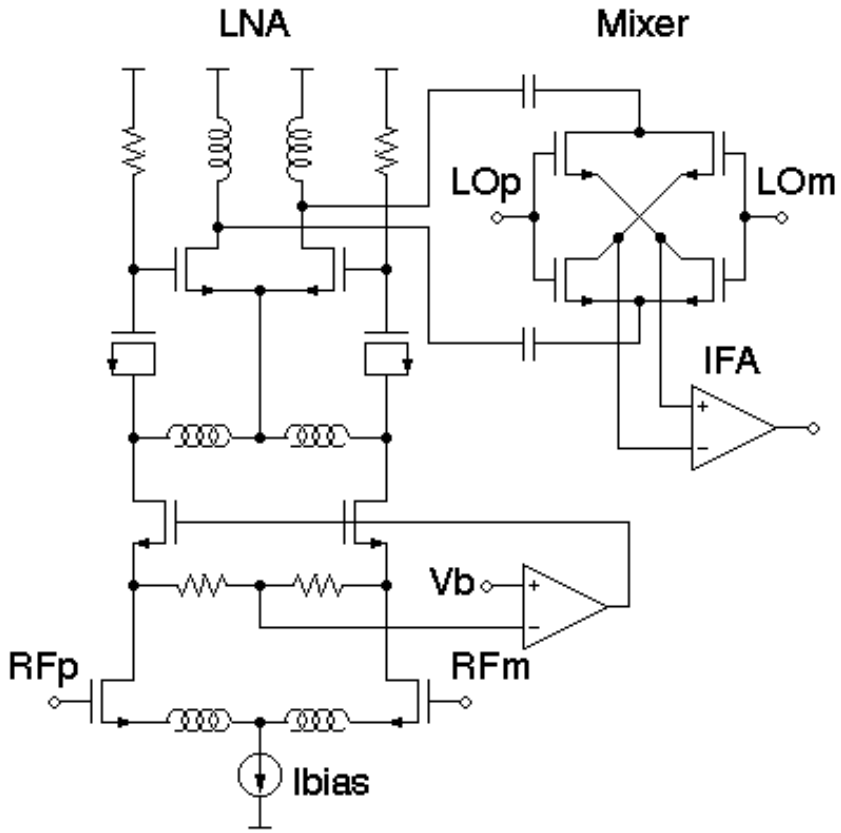


Fastlane mixer (simplified, biasing incomplete)

Frequency Conversion: Fastlane Results

LO Frequency	1.40042GHz
RF Frequency	1.57542GHz
IF Frequency	175MHz
LO Amplitude	300mV (~ -3.5dBm in 100Ω)
IP3 (Input)	10dBm
1dB Compression (Input)	-5dBm
Noise Figure (SSB)	10dB
Voltage Conversion Gain	-3.6dB
Supply Voltage	1.5V
Technology	0.35μm CMOS
Die Area	0.84mm^2

Frequency Conversion: Measurement Results



Waldo mixer

Frequency Conversion: Waldo Results

LO Frequency	1.57342GHz
RF Frequency	1.57542GHz
IF Frequency	2MHz
LO Amplitude*	2V (differential)
IP3 (Input)*	9dBm
Noise Figure (SSB)**	6dB
Voltage Conversion Gain*	-3dB
Supply Voltage	2.5V
Technology	0.5μm CMOS
Die Area	0.0084mm^2

* simulated

** inferred from measured results

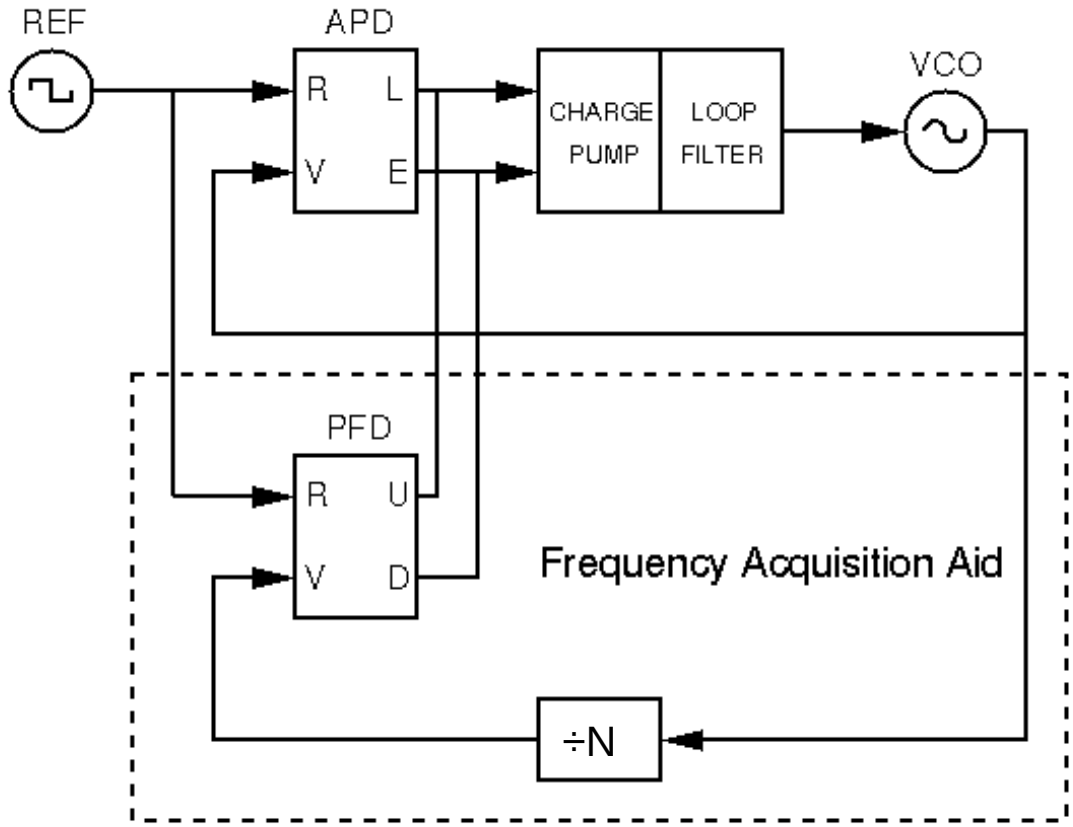
Frequency Synthesis

- Performance Metrics
- Architectures
- Aperture Phase Detector (APD)
  - Implementation
  - Modeling
- Die Photo + Measurement Results

Frequency Synthesis: Performance Metrics

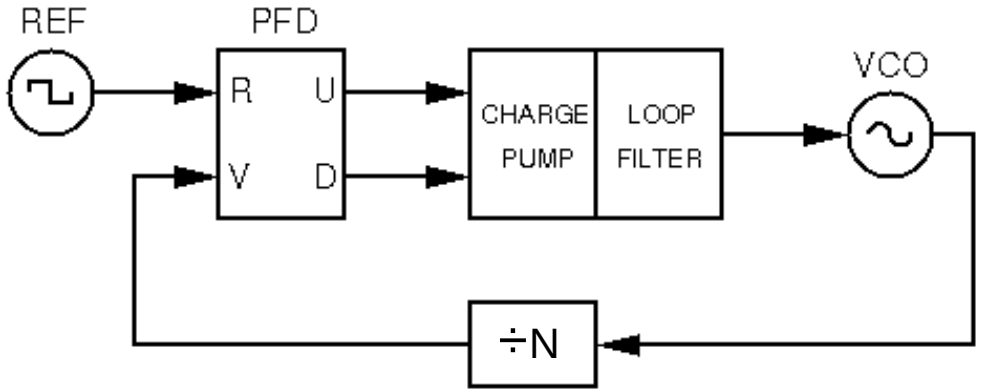
- Power
  - Achieve desired performance with minimum power consumption
- Phase Noise
  - Use a PLL based architecture with a crystal reference and design a wideband loop
- Amplitude and Frequency of Spurs
  - Convert undesired signals to the intermediate frequency

Frequency Synthesis: Architectures



- Aperture Phase Detector (APD) is a low power method for maintaining phaselock

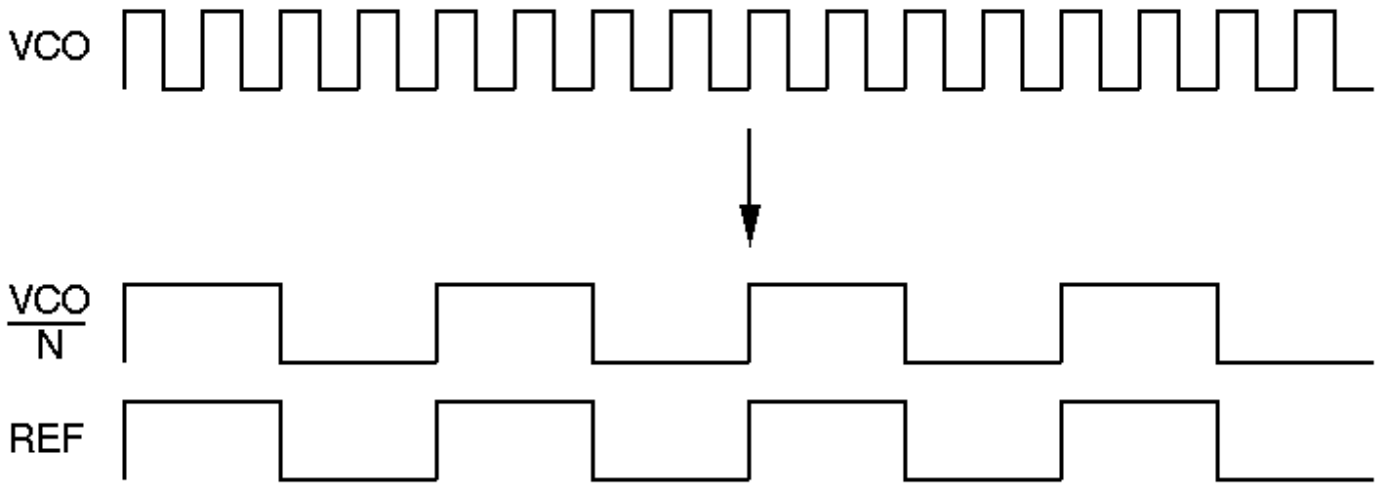
Frequency Synthesis: Architectures



Power	90mW (3V)
÷N	*22.5mW*
VCO	*36mW*
Synthesized Frequency	1.6GHz
Technology	0.6μm CMOS
Die Area	1.6mm^2

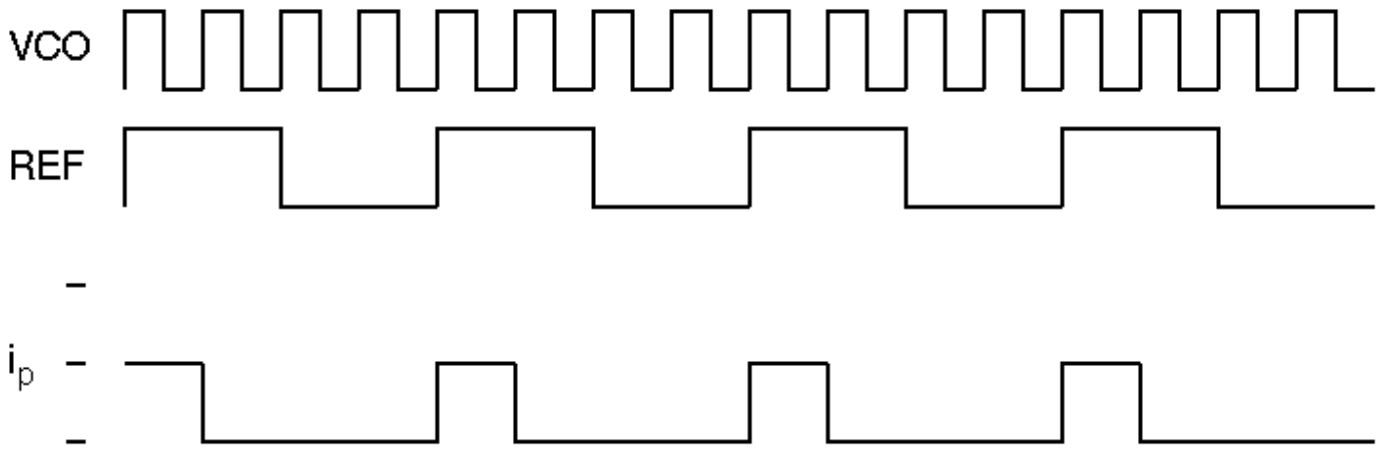
J.F. Parker and D. Ray, "A 1.6-GHz CMOS PLL with on-chip loop filter," *IEEE J. Solid-State Circuits*, vol. 33, pp. 337-343, Mar. 1998.

Frequency Synthesis: Architectures



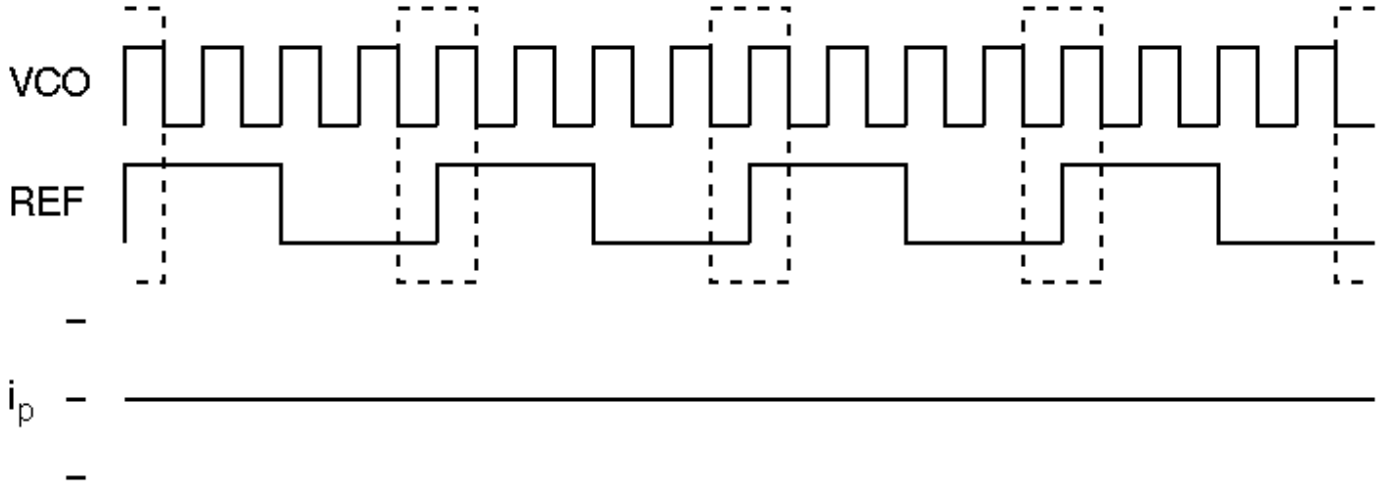
Signal waveforms in a PLL with a divide-by-N block and a Phase/Frequency Detector

Frequency Synthesis: Architectures



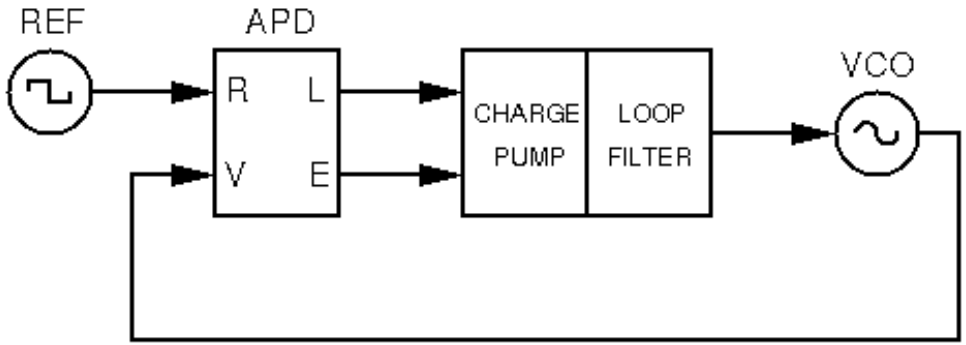
Signal waveforms in a PLL without the divide-by-N block using a Phase/Frequency Detector

Frequency Synthesis: Architectures



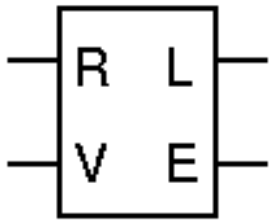
Signal waveforms in a PLL without the divide-by-N block using an Aperture Phase Detector

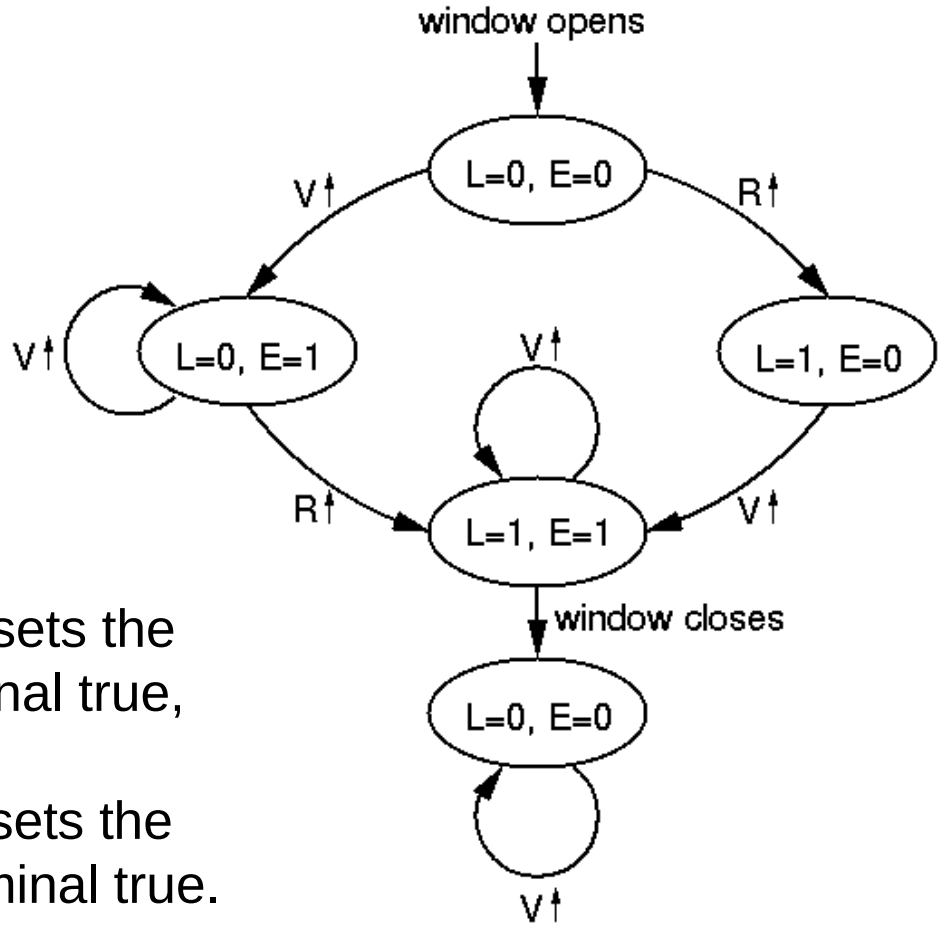
Frequency Synthesis: Architectures



Power	36mW (2.5V)
VCO	*26mW*
Synthesized Frequency	1.573GHz
Technology	0.5μm CMOS
Die Area	3.1mm^2

Frequency Synthesis: APD Implementation



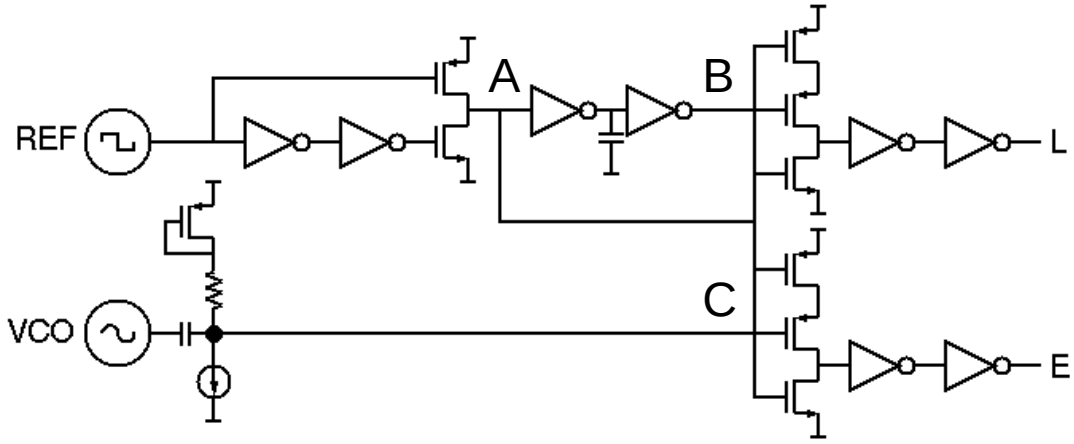


When the window opens, the phase detector becomes active:

the R-input rising edge sets the L (denoting “late”) terminal true,

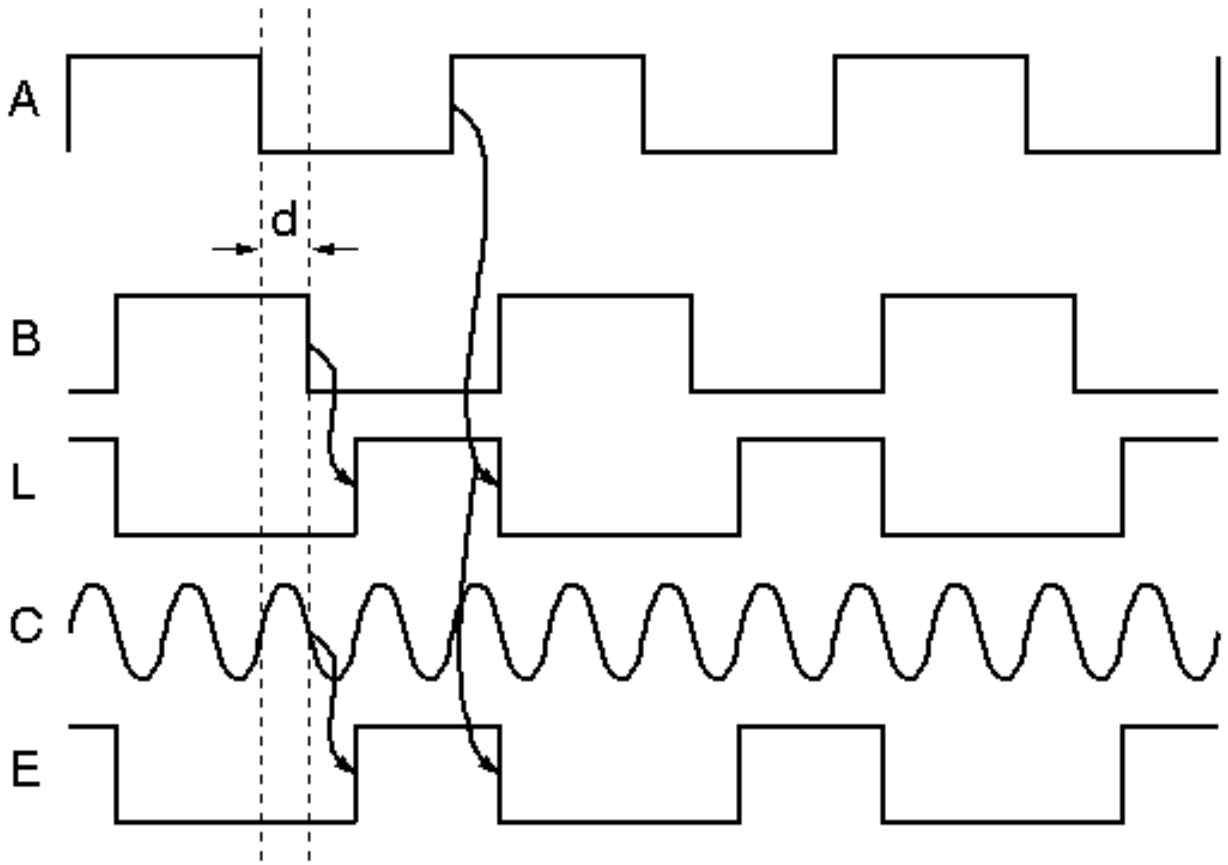
the V-input rising edge sets the E (denoting “early”) terminal true.

Frequency Synthesis: APD Implementation



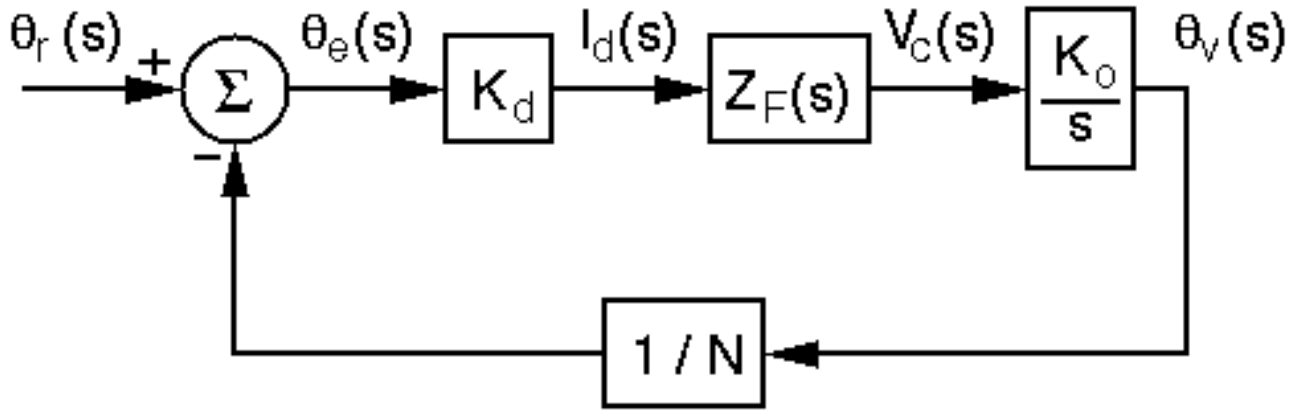
- Window is derived from the reference clock
  - fixed delay between window opening and reference edge
- Precharged gates only respond to first edge
  - subsequent VCO edges after first have no effect

Frequency Synthesis: APD Implementation



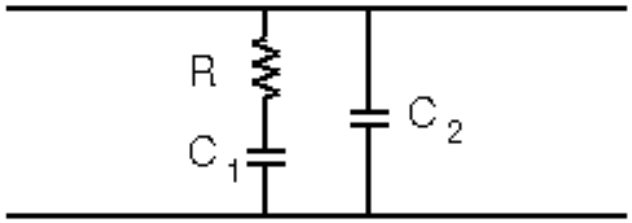
Frequency Synthesis: PLL Modeling

LTI model of PLL in lock



$$H(s) = \frac{\theta_v}{\theta_r} = \frac{NK_dK_oZ_F(s)}{Ns + K_dK_oZ_F(s)} \quad ; \quad K_d = \frac{I_p}{2\pi}$$

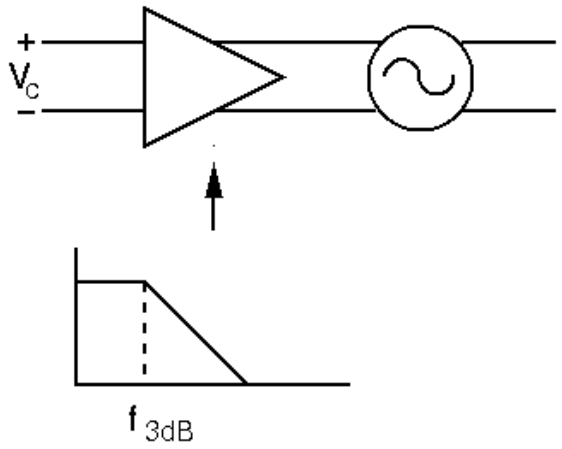
Frequency Synthesis: PLL Modeling



The loop filter contributes 2 poles and 1 zero to the forward path:

$$Z_F(s) = \frac{1 + sRC_1}{(C_1 + C_2)s\left(1 + s\dfrac{RC_1C_2}{(C_1 + C_2)}\right)}$$

Frequency Synthesis: PLL Modeling



The VCO contributes 2 poles to the forward path:

$$\frac{K_o}{s\left(1+\frac{s}{2\pi f_{3\,dB}}\right)}$$

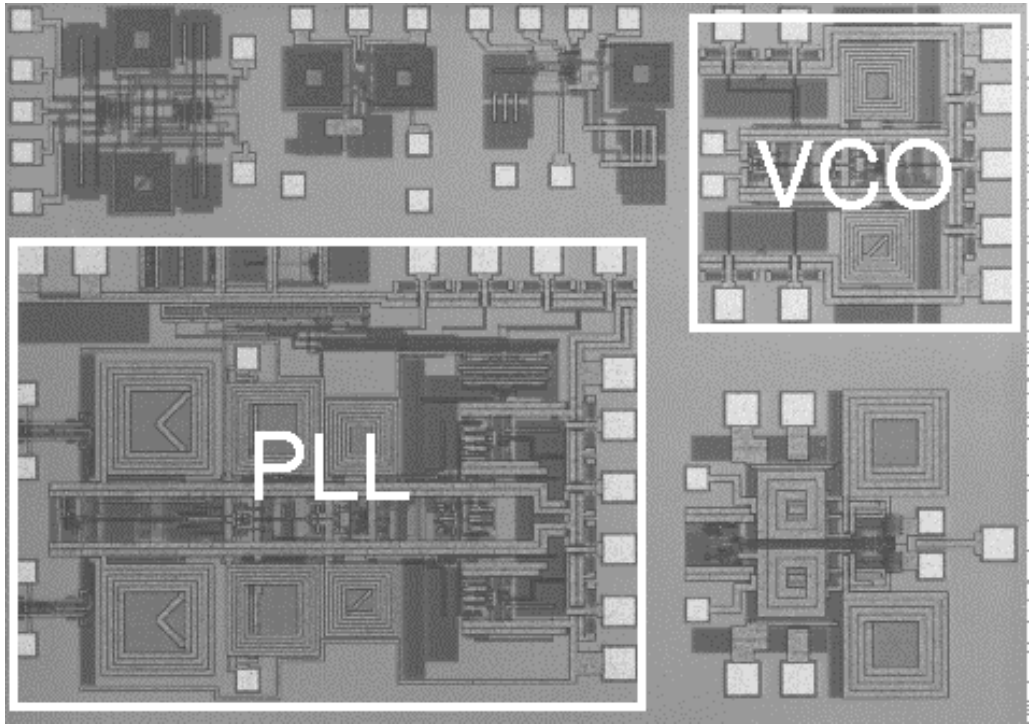
Frequency Synthesis: PLL Modeling

$$H(s) = \frac{NK_d K_o (1 + sRC_1)}{N(C_1 + C_2)s^2 \left(1 + \frac{s}{2\pi f_{3dB}}\right)\left(1 + \frac{sRC_1C_2}{C_1 + C_2}\right) + K_d K_o (1 + sRC_1)}$$

The loop has seven parameters

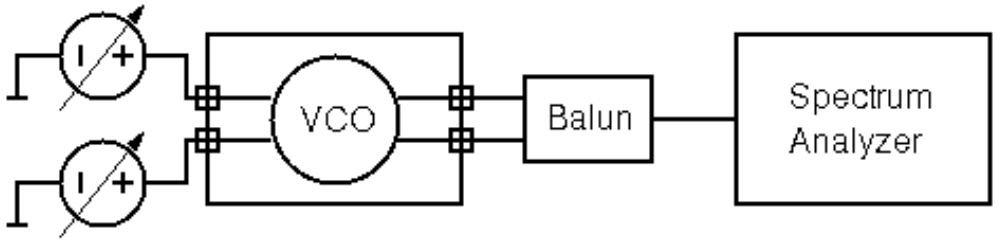
N	Frequency ratio
K_d	Phase detector gain constant
K_o	VCO gain constant
R	Loop filter
C_1	Loop filter
C_2	Loop filter
f_{3dB}	VCO preamp 3dB bandwidth

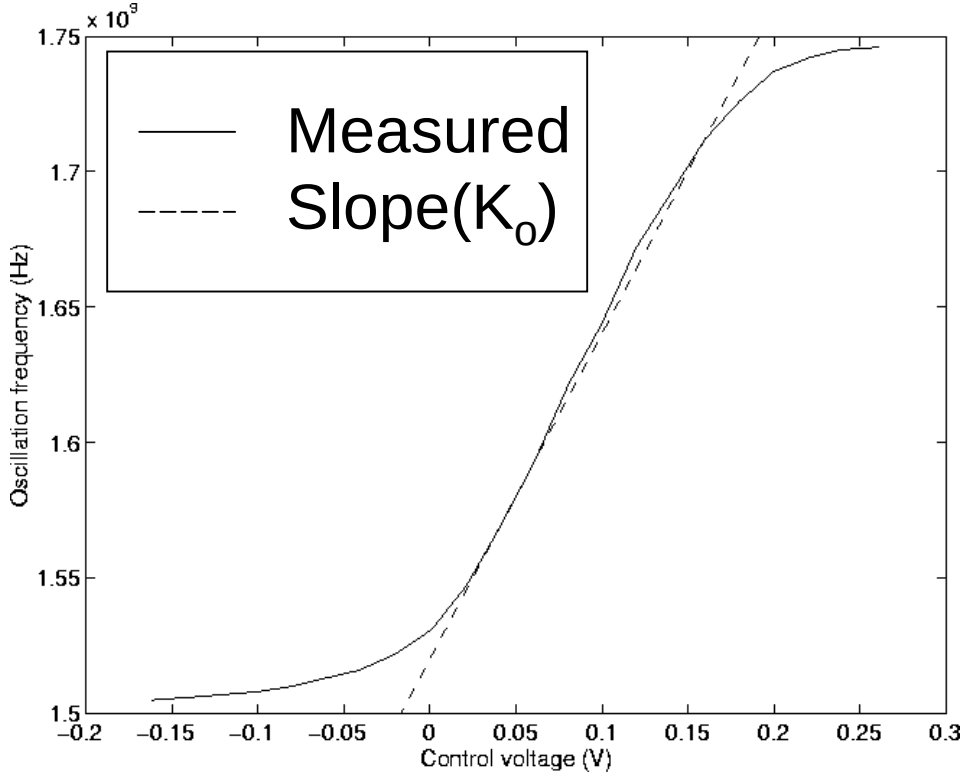
Frequency Synthesis: Die Photo



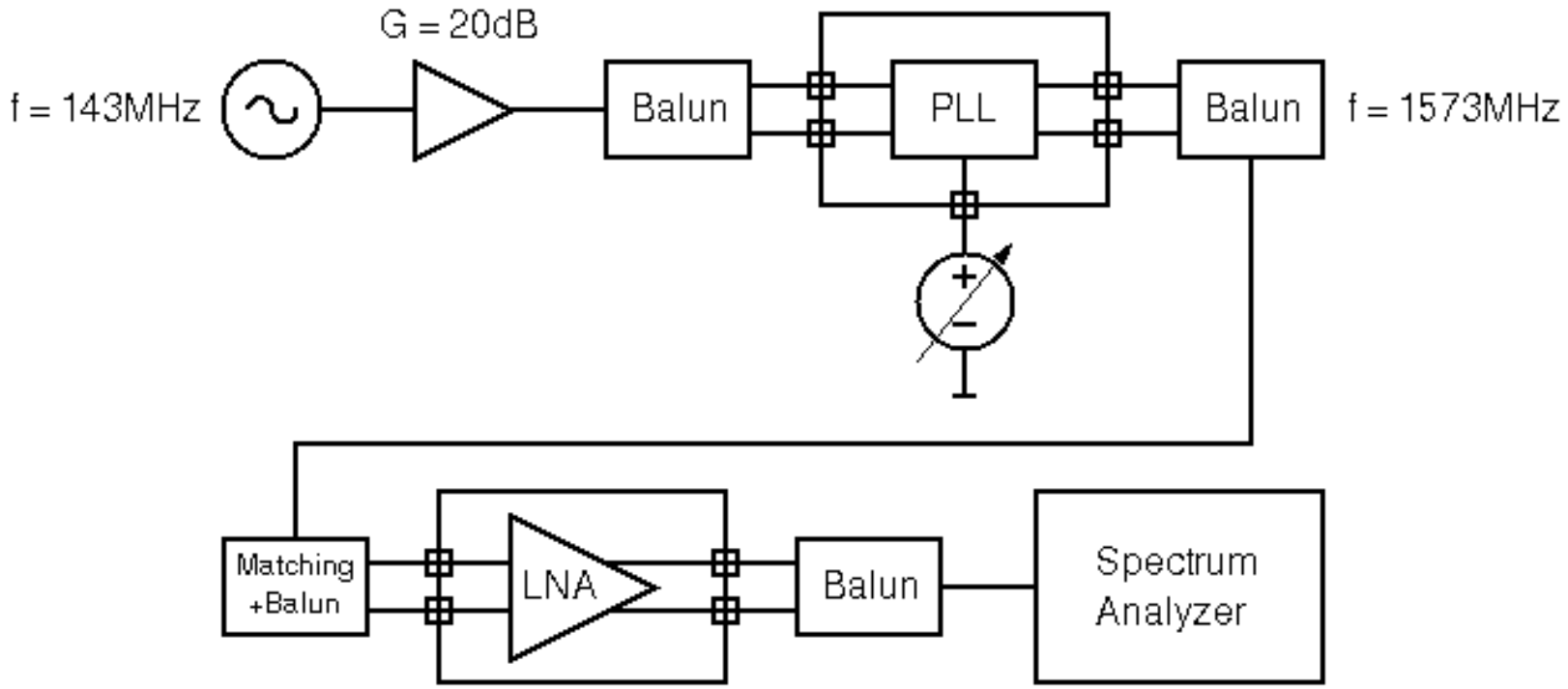
Waldo test chip: 0.5μm CMOS

Frequency Synthesis: Measurement Results

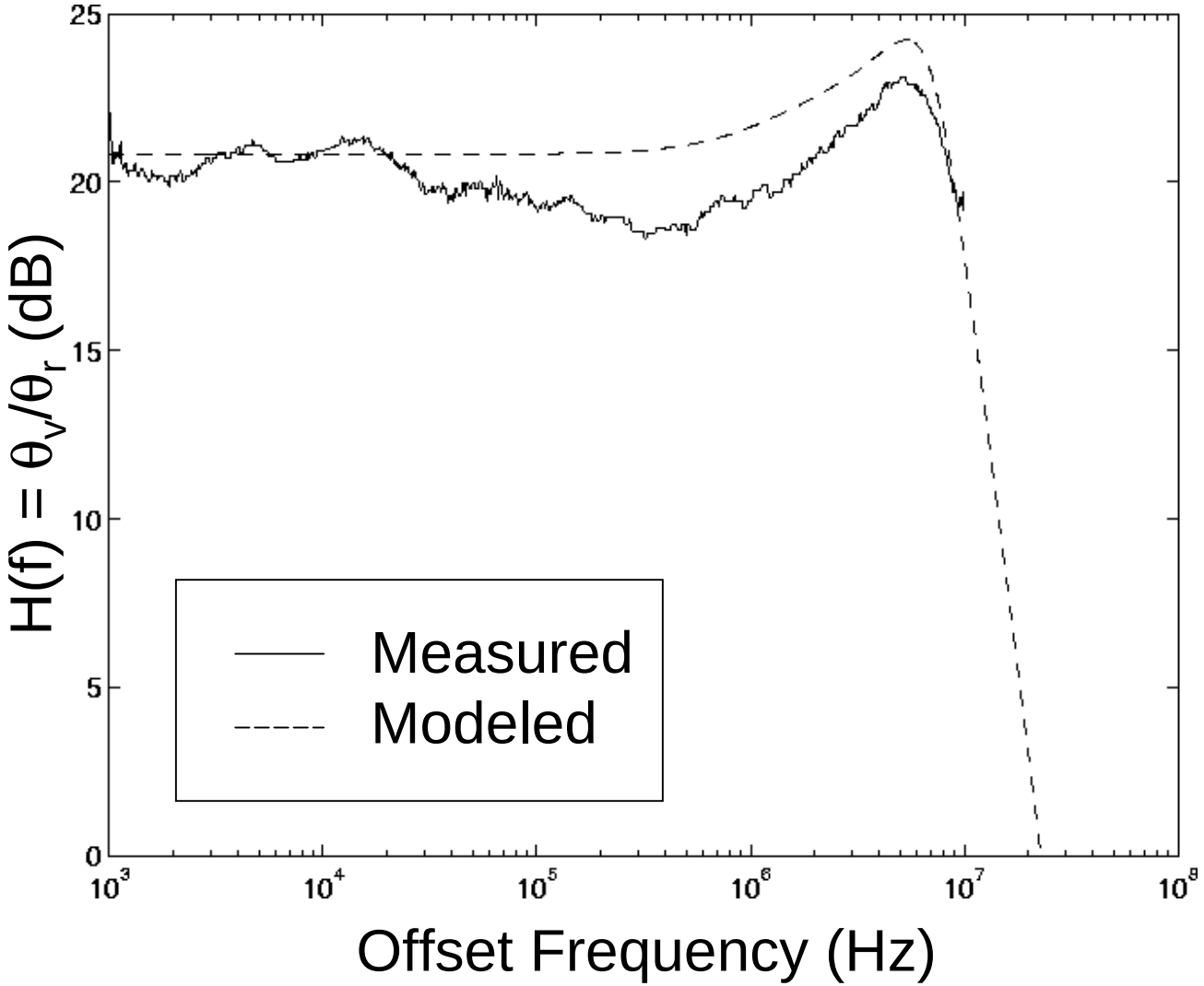




Frequency Synthesis: Measurement Results



Frequency Synthesis: Measurement Results



Frequency Synthesis: Measurement Results

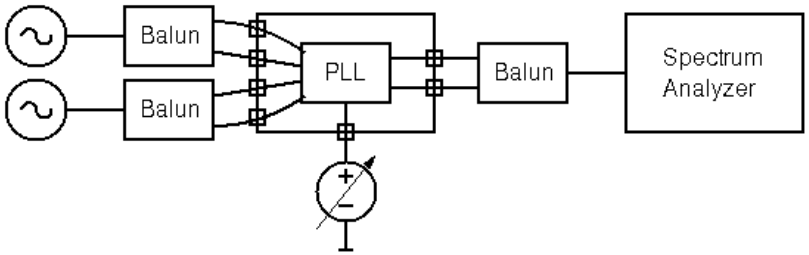
The loop has seven parameters: N, K_d, K_o, R, C_1, C_2, and f_{3dB}. These parameters are set as follows to generate the smooth curve on the previous slide:

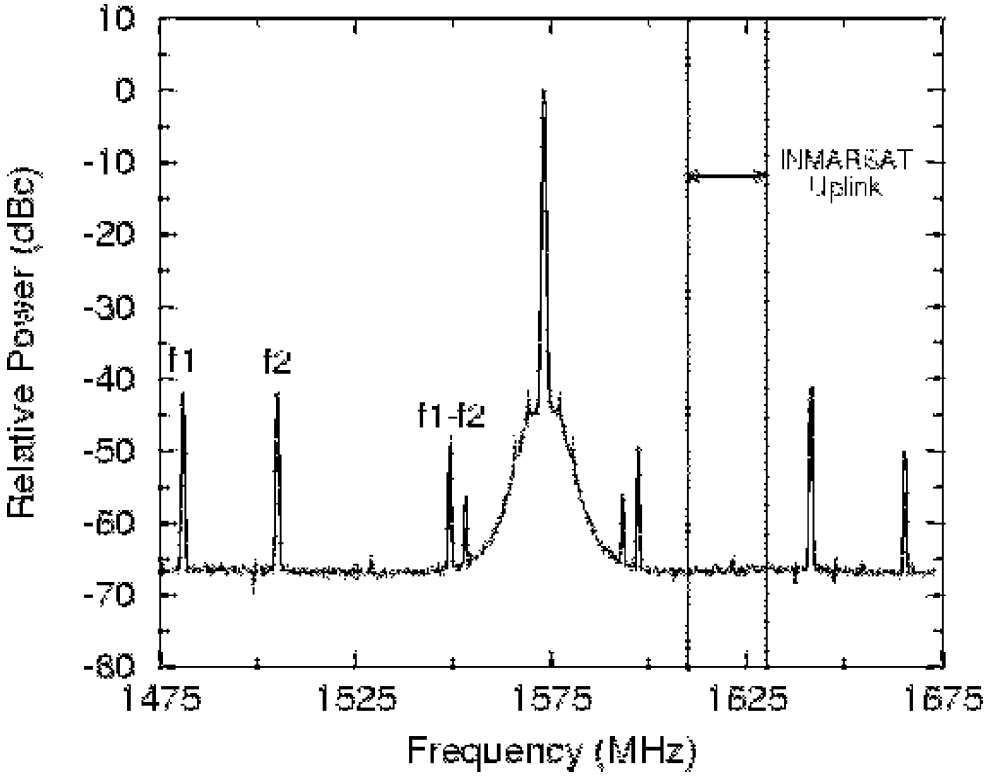
- N is known
- K_o is taken from measured data
- R, C_1, and C_2 are taken to be their designed values
- f_{3dB} and K_d are fit

	calculated from technology data	fit
f_{3dB}	15MHz	15MHz

	simulated	fit
K_d	7.4uA/rad	6.6uA/rad

Frequency Synthesis: Measurement Results





Frequency Synthesis: Measurement Results

PLL

Loop Bandwidth	6MHz
f_{ref1}, f_{ref2} spurious	≤ -40dBc
f_{ref1}-f_{ref2} spur	≤ -50dBc

VCO:

Gain Constant, K_o	$2\pi(1.2*10^9)$rad/s/V
Tuning Range	240MHz(±7.4%)
Phase Noise @ 35MHz	≤ -135dBc/Hz
Power Consumption	26mW

Total Power Consumption	36mW (2.5V supply)
Technology	0.5μm CMOS
Die Area	3.1mm^2

Conclusion: Contributions

- A new low power frequency conversion architecture that processes signals in the voltage domain
  - explored reactive terminations to improve mixer performance
  - a new understanding of the passive CMOS mixer
- A new low power frequency synthesis architecture eliminating the ÷N block for phaselock
  - new method of phase comparison
    - circuit implementation
    - modeling theory
- Incorporation of low power mixer and low power synthesizer into a low power, integrated CMOS GPS receiver front-end

Conclusion: Acknowledgements

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