A Fully-Integrated 5GHz CMOS Wireless-LAN Receiver

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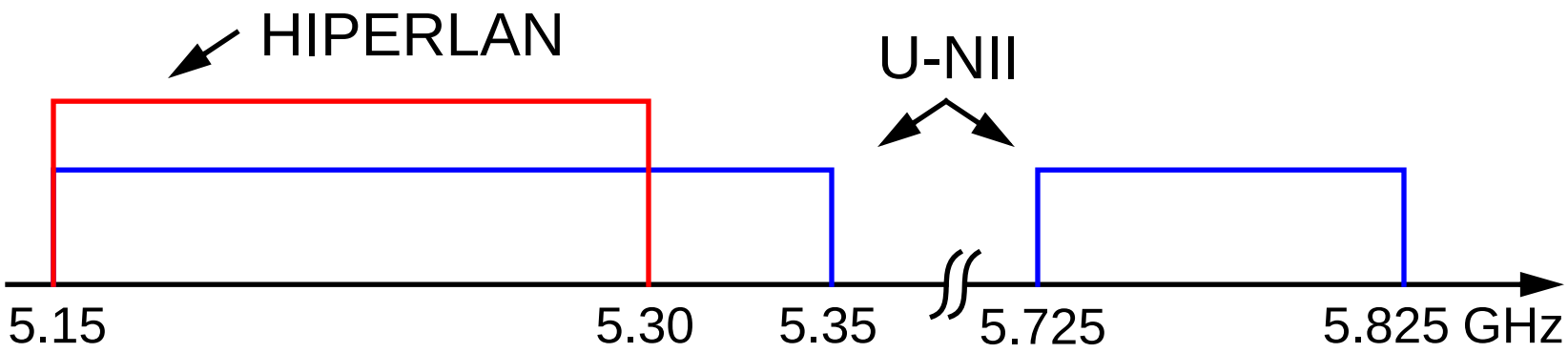
Outline

- Motivation
- Introduction to Wireless LAN
- Receiver Architecture
- Circuit Implementations
- Offset Cancellation Techniques
- Fractal Capacitors
- Measurements
- Conclusions

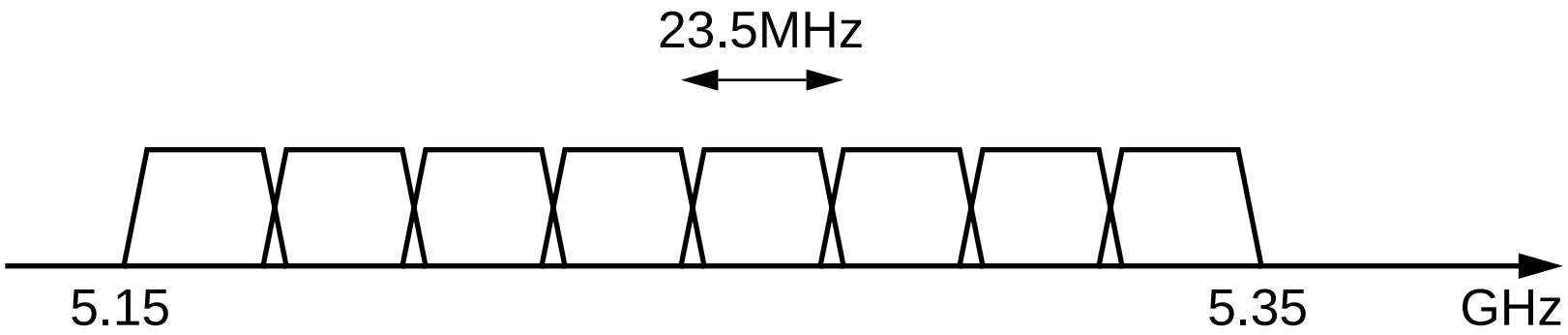
Motivation

- Demand for wideband wireless local area network (LAN)
  - High data rate (> 20Mb/s)
  - Low cost (CMOS)
  - Low power
- New released frequency band in US
  - Unlicensed national information infrastructure (U-NII) band
- Existing frequency band in Europe
  - High performance radio LAN(HIPERLAN) band

Available Frequency Bands



- U-NII and HIPERLAN frequency bands.



- Proposed channel allocation for a U-NII band WLAN system.
  - Compatible with HIPERLAN.

HIPERLAN Receiver Requirements

Modulation	GMSK
Maximum signal level	-25dBm
Sensitivity	-70dBm
Channel bandwidth	23.5MHz
Spurious emissions 30MHz-1GHz 1GHz-25.5GHz	 -57dBm -47dBm

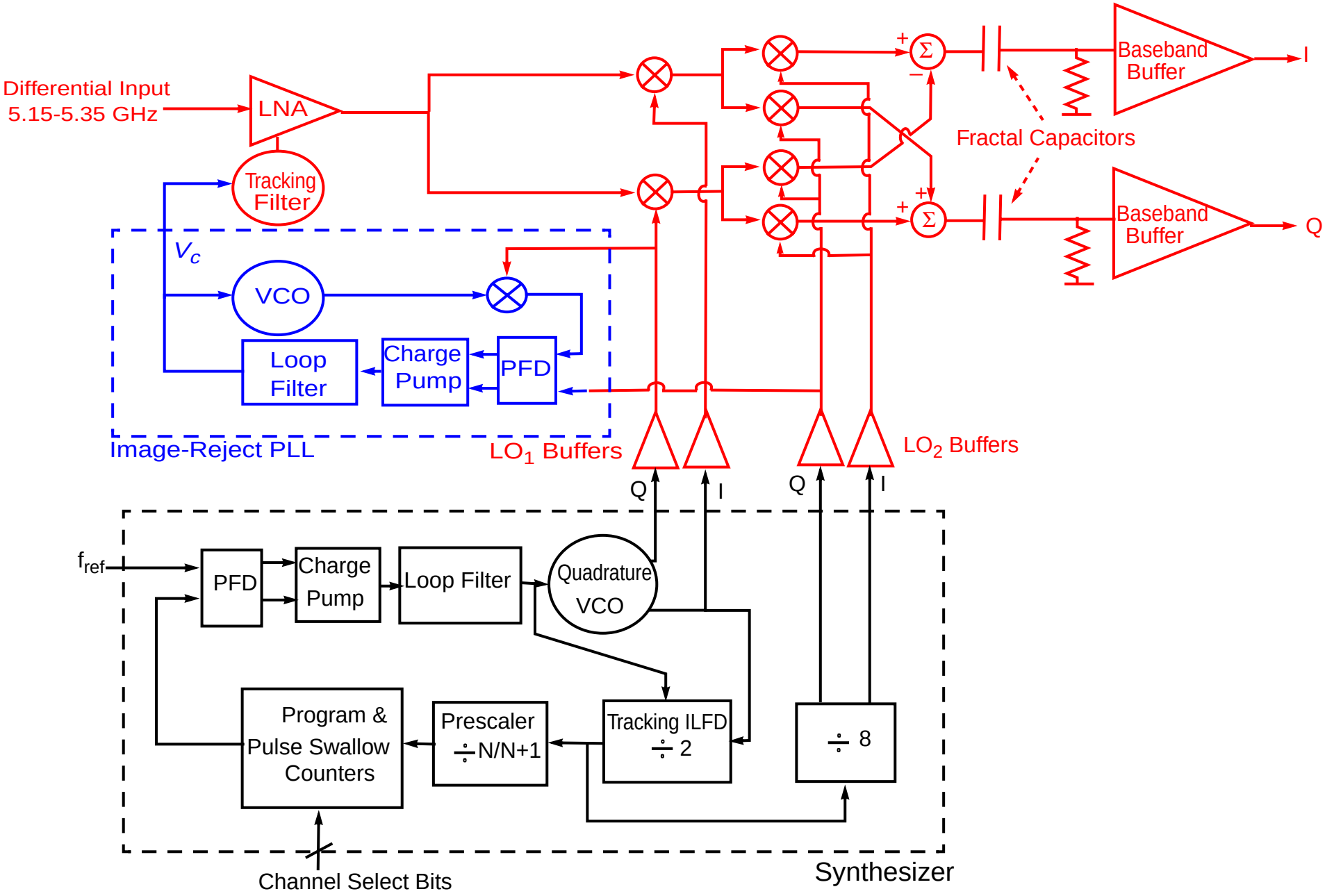
$$NF < -143.7\text{dBm/Hz} - 12\text{dB} - (-174\text{dBm/Hz}) = 18.3\text{dB}$$

Sensitivity
(-70dBm)/(23.5MHz)

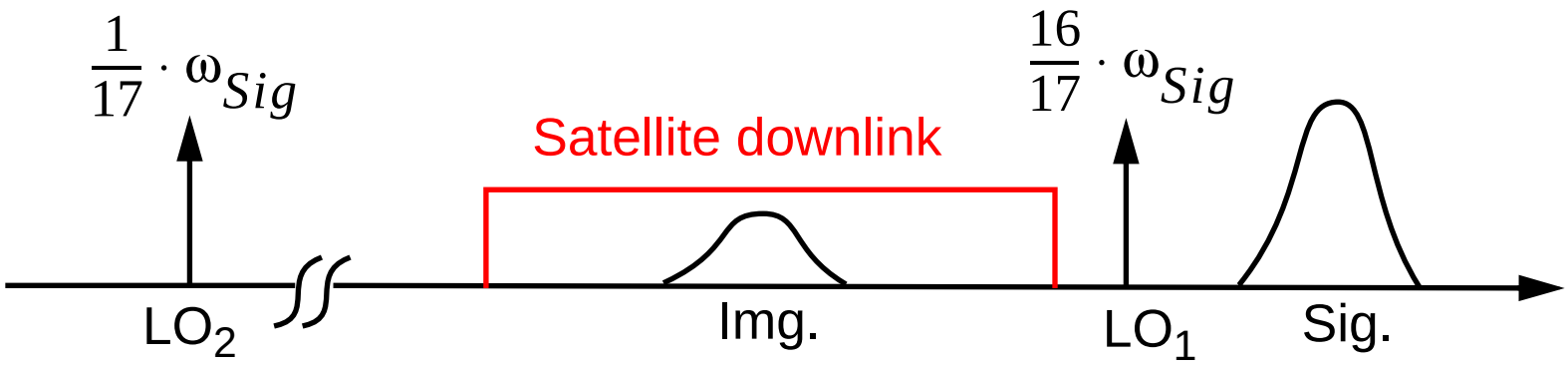
Pre-detection SNR

Available noise power of the antenna

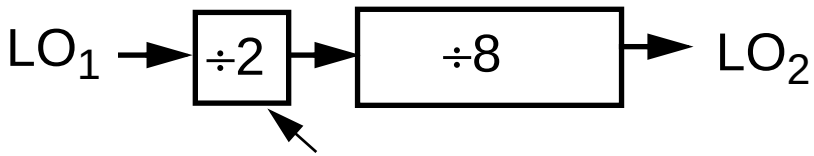
Receiver Architecture



LO Frequencies



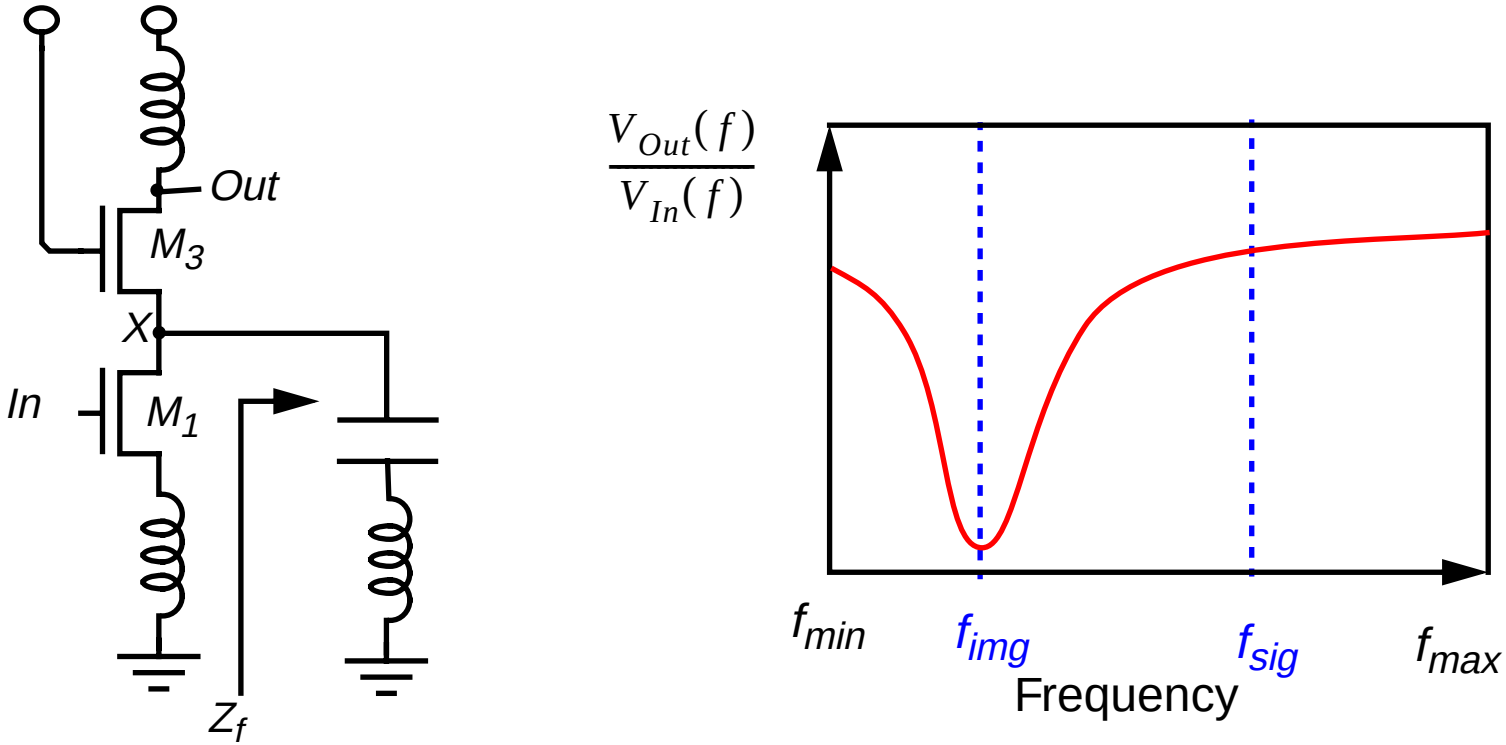
- Image signal is small.



Low-power injection-locked frequency divider

- LO_2 easily obtained from LO_1.

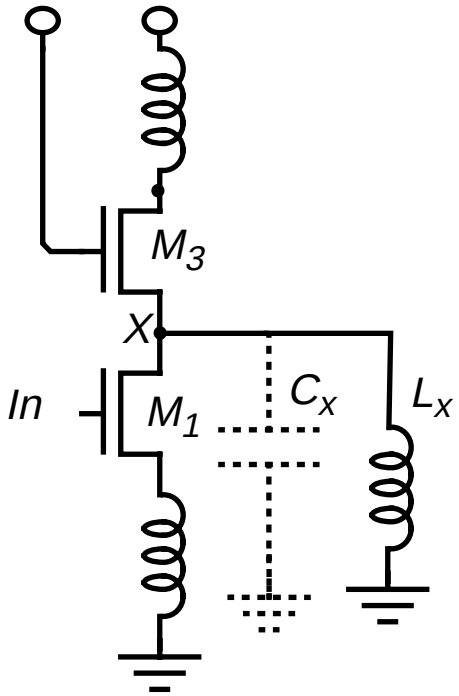
Image Rejection

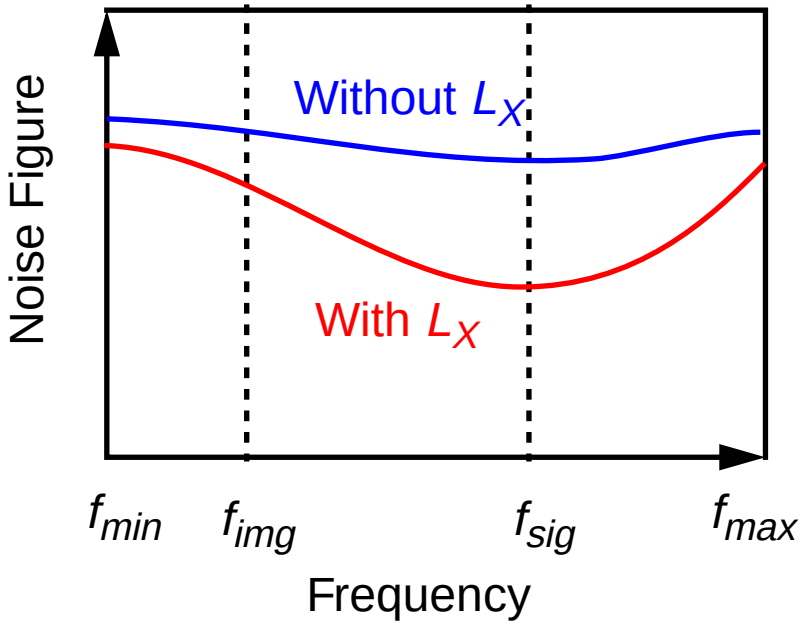


- Series resonance @f_{Img}→ improves image rejection

Noise Rejection

Parasitic capacitance C_X degrades the noise performance.





- Parallel resonance @f_{Sig}→ improves noise figure

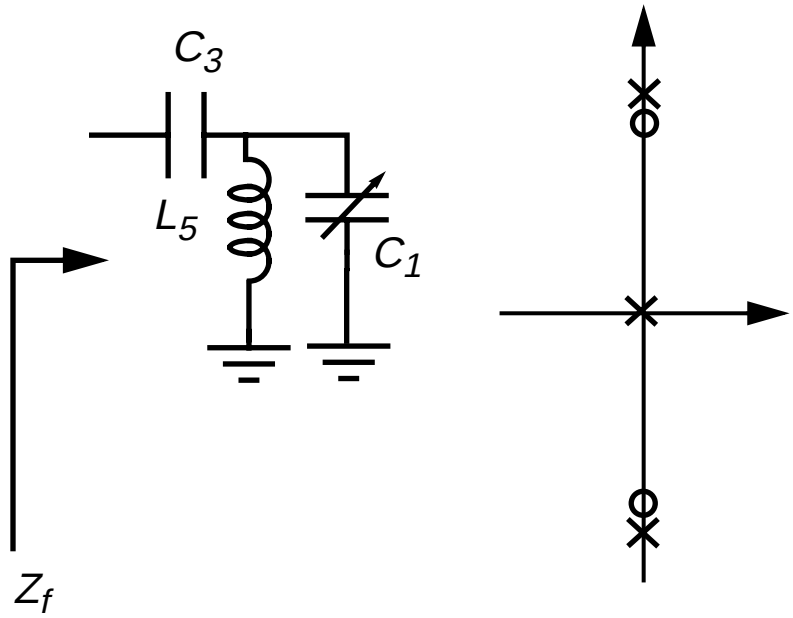
Solution: Third-Order Filter

$$Z_f(s) = \frac{L_5 \cdot (C_3 + C_1) \cdot s^2 + 1}{C_1 \cdot C_3 \cdot L_5 \cdot s^3 + C_3 \cdot s}$$

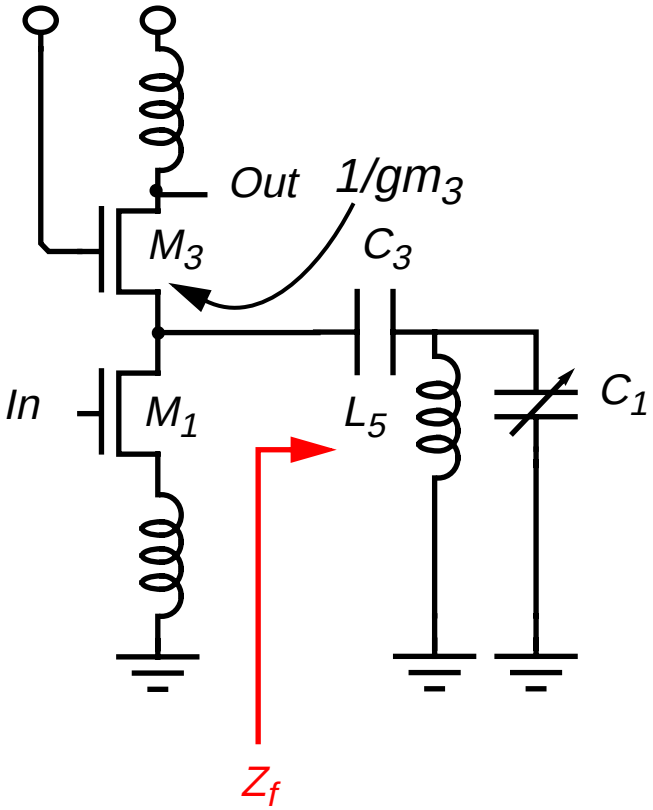
$$\omega_p = 0$$

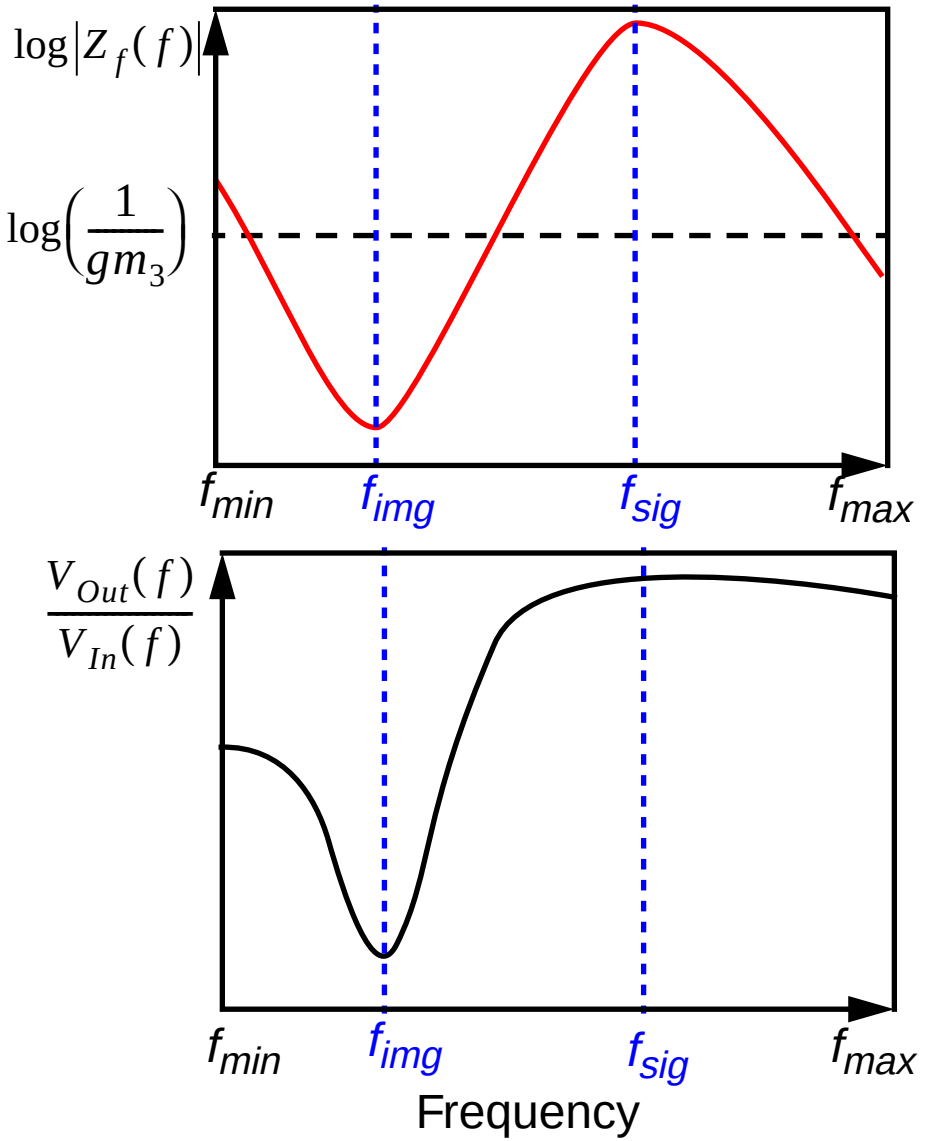
$$\omega_p = \pm \frac{1}{\sqrt{L_5 \cdot C_1}}$$

$$\omega_z = \pm \frac{1}{\sqrt{L_5 \cdot (C_3 + C_1)}}$$

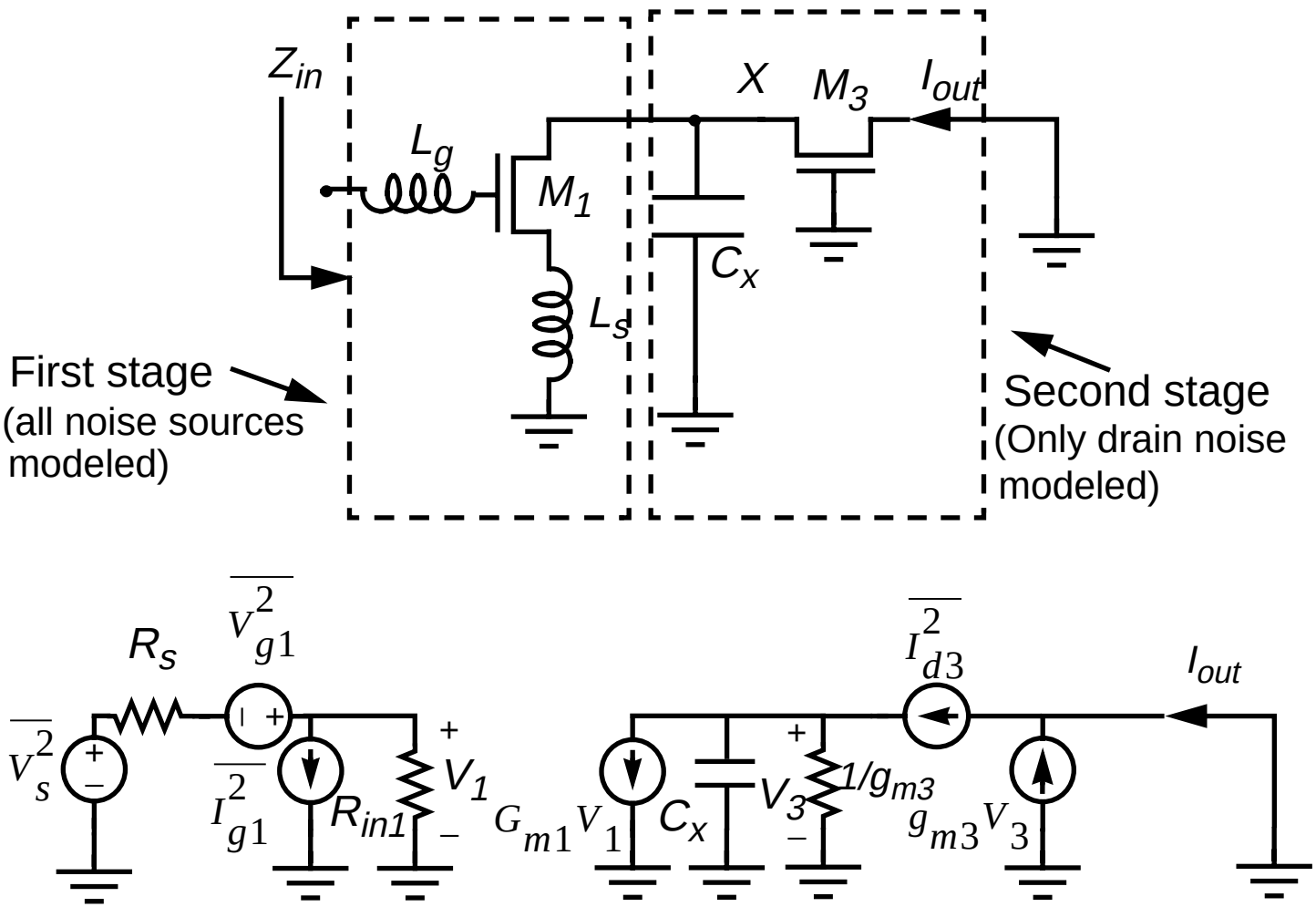


LNA/Filter Transfer Function

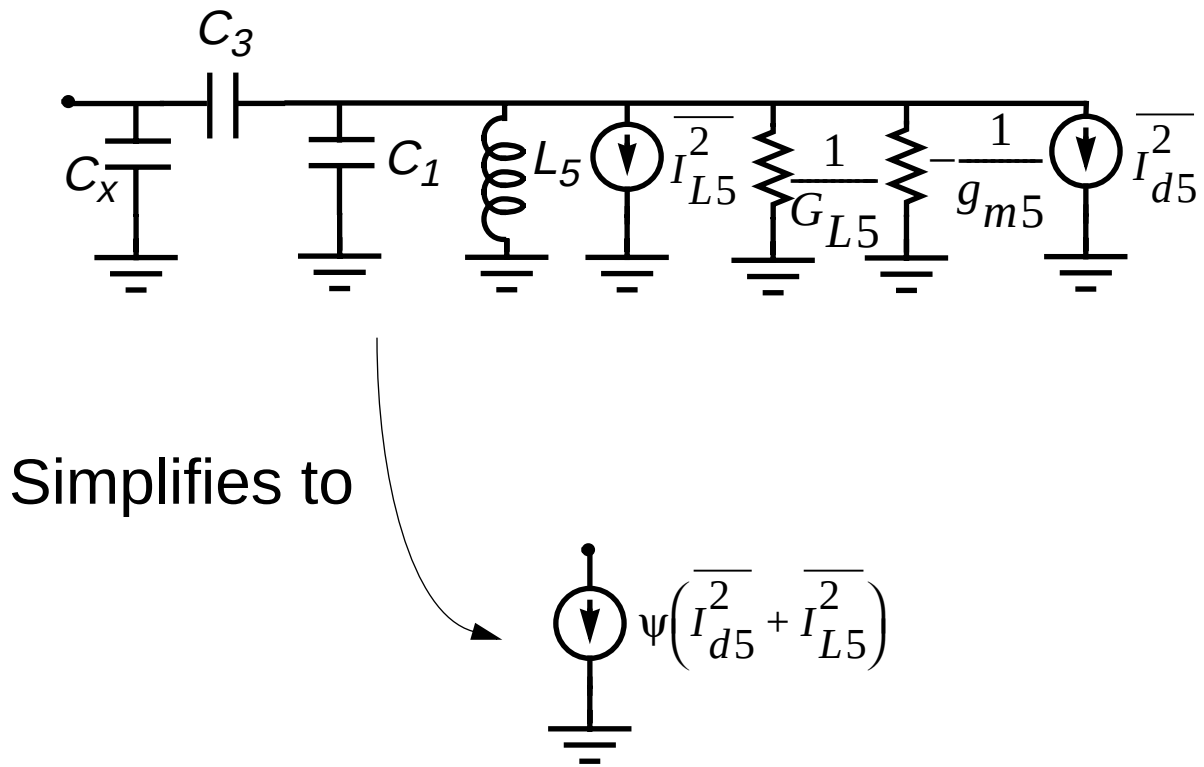




Equivalent Noise Circuit for the LNA



Filter Noise Model



Noise Formulas

$$F_{no-filter} = F_1 + 4R_s\gamma_3 g_{do3}\left(\frac{\omega_0^2}{\omega_T^2}\right)\left(\frac{C_x^2}{g_{m3}^2}\omega_0^2\right)$$

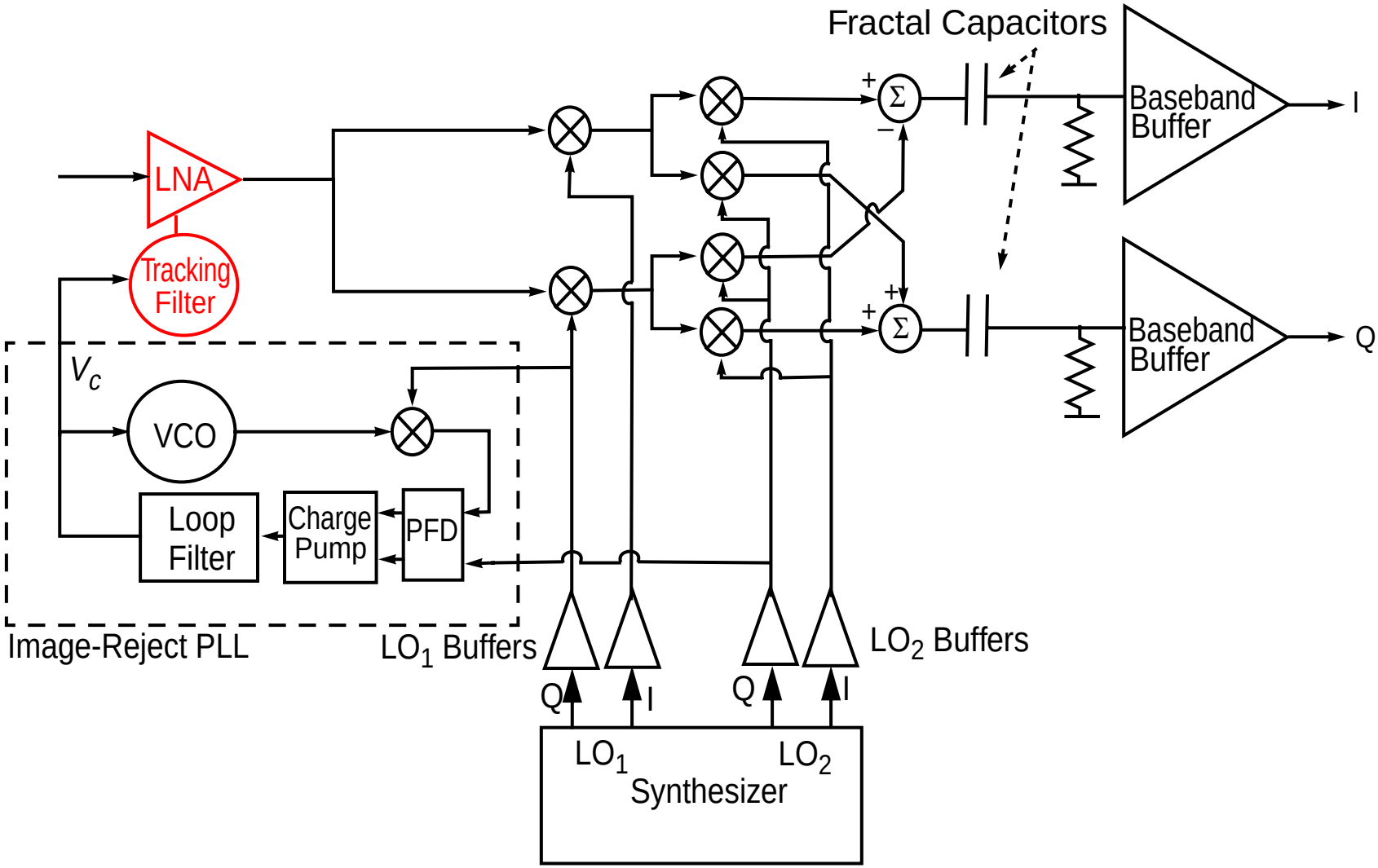
$$F_{with-ideal-filter} = F_1$$

$$F_{tot} = F_1 + \psi \cdot 4R_s(\gamma_5 g_{do5} + G_{L5})\left(\frac{\omega_0^2}{\omega_T^2}\right)$$

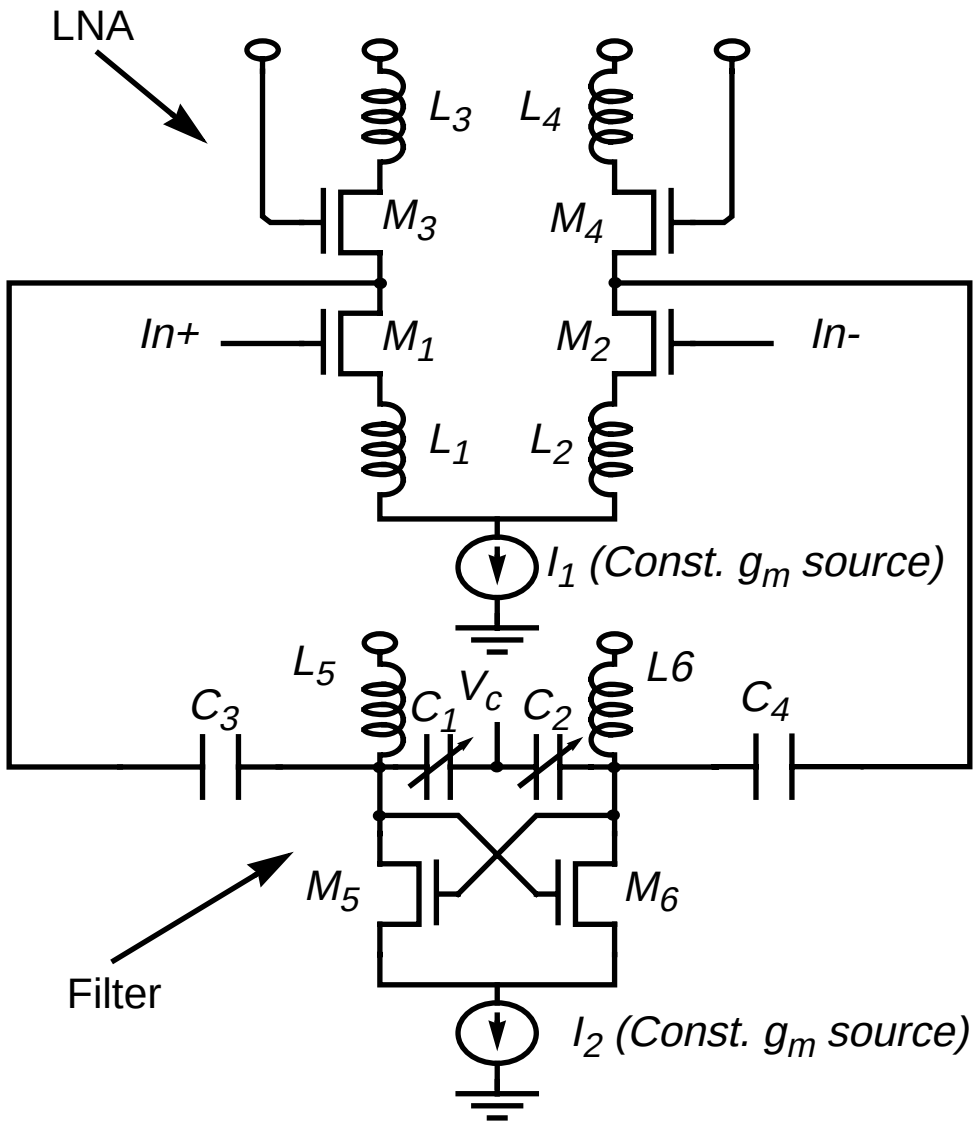
Where $\Psi = \dfrac{C_3^2 \cdot \omega_0^2}{\left(\dfrac{C_3^2}{C_x + C_3}\right)^2 \cdot \omega_0^2 + (G_{L5} - g_{m5})^2}$,

and F_1 is the noise figure of the first stage defined in: D. Shaeffer and T. Lee, “A 1.5V, 1.5 GHz CMOS Low Noise Amplifier”, *IEEE Journal of Solid-State Circuits*, May 1997, pp. 745-759.

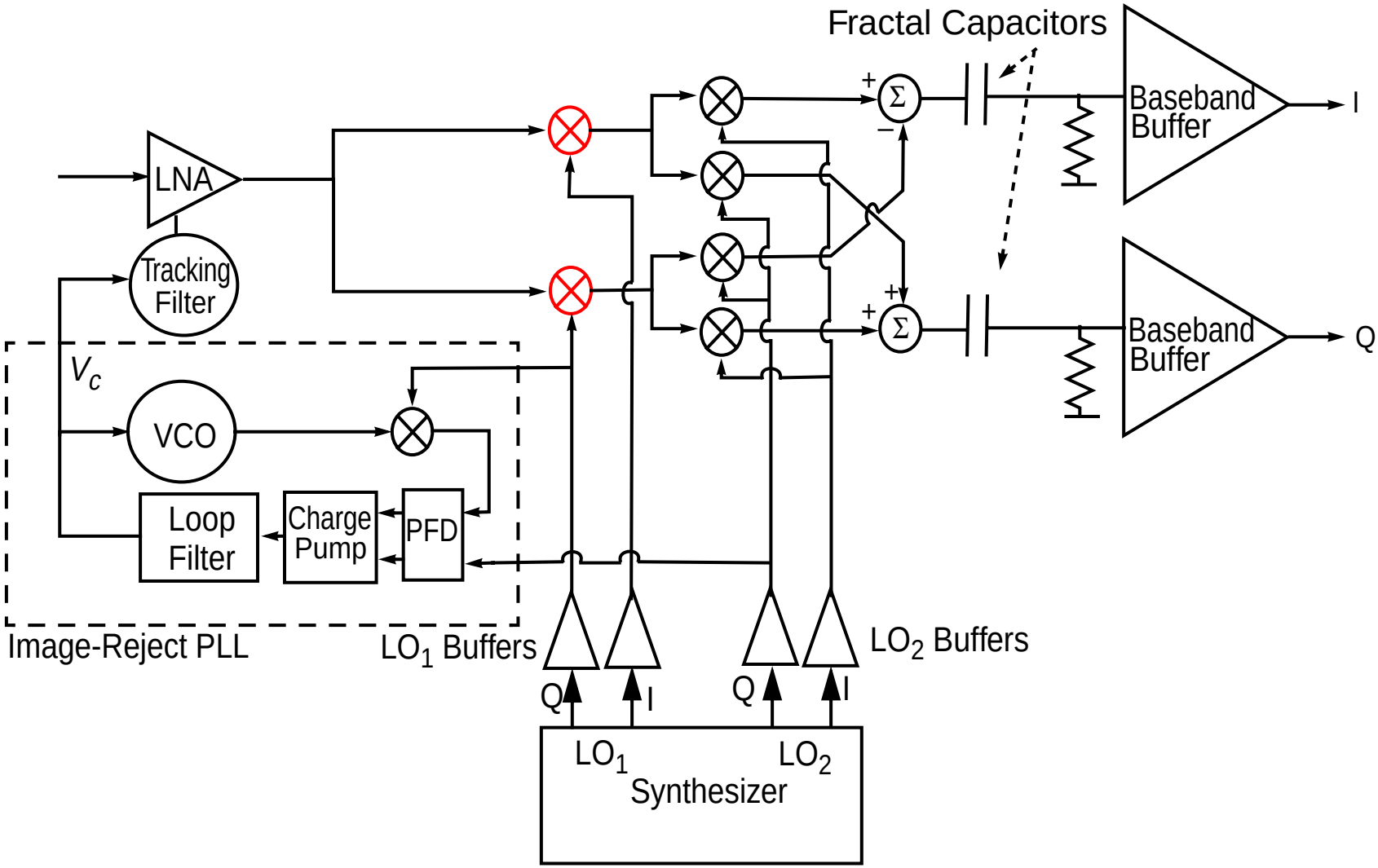
Receiver Architecture



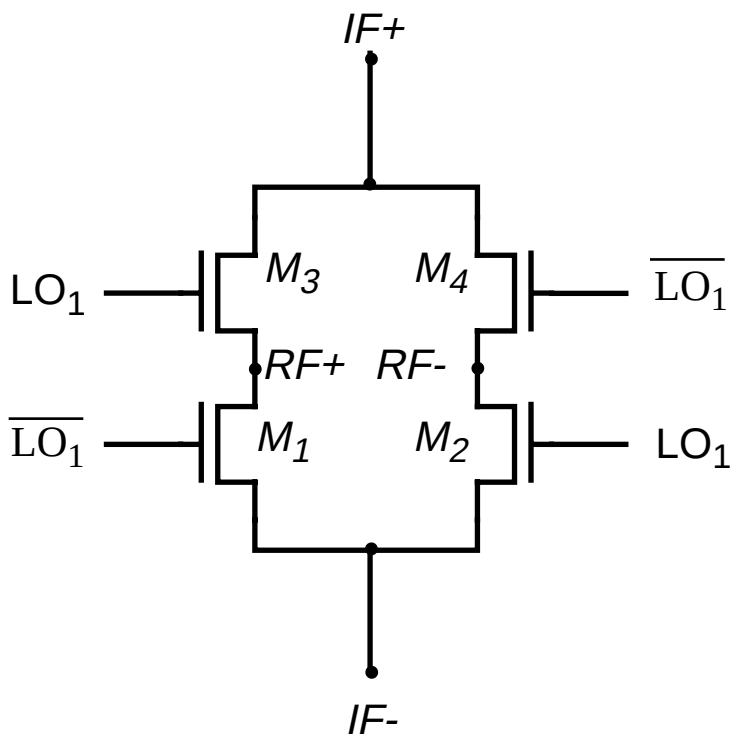
Circuit Implementation: LNA and filter



Receiver Architecture

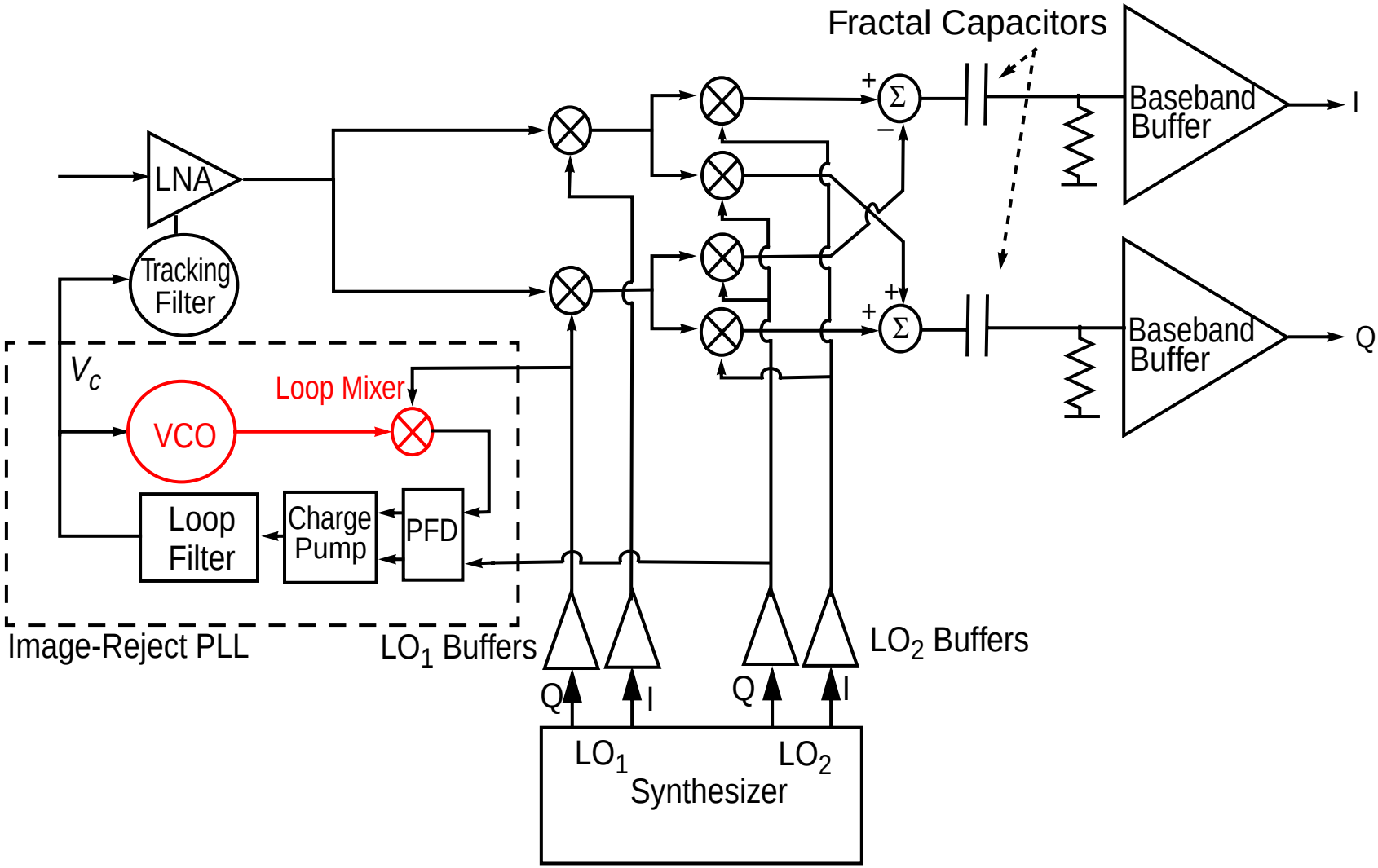


Circuit Implementation: First Mixers

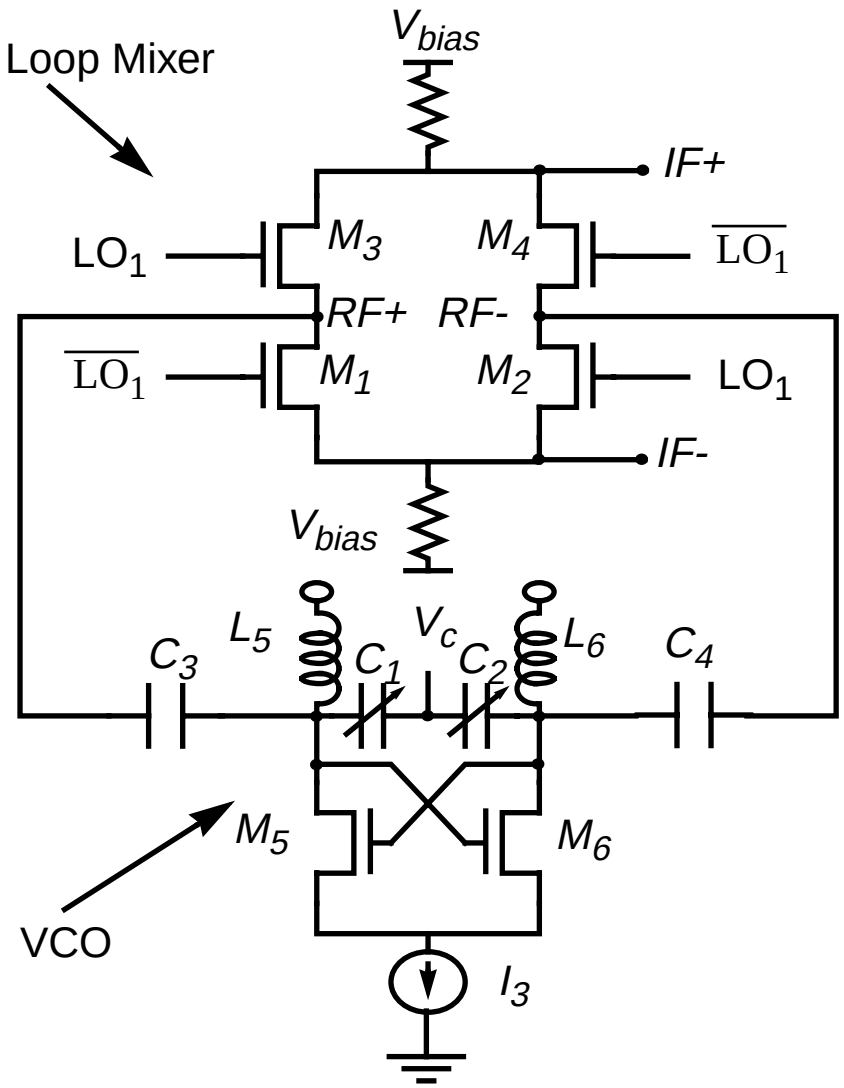


- A. Shahani, et al, “A 12-mW wide dynamic range front-end for a portable GPS receiver,” *IEEE J. Solid-State Circuits*, vol. 32, pp. 2061-2070, Dec. 97.

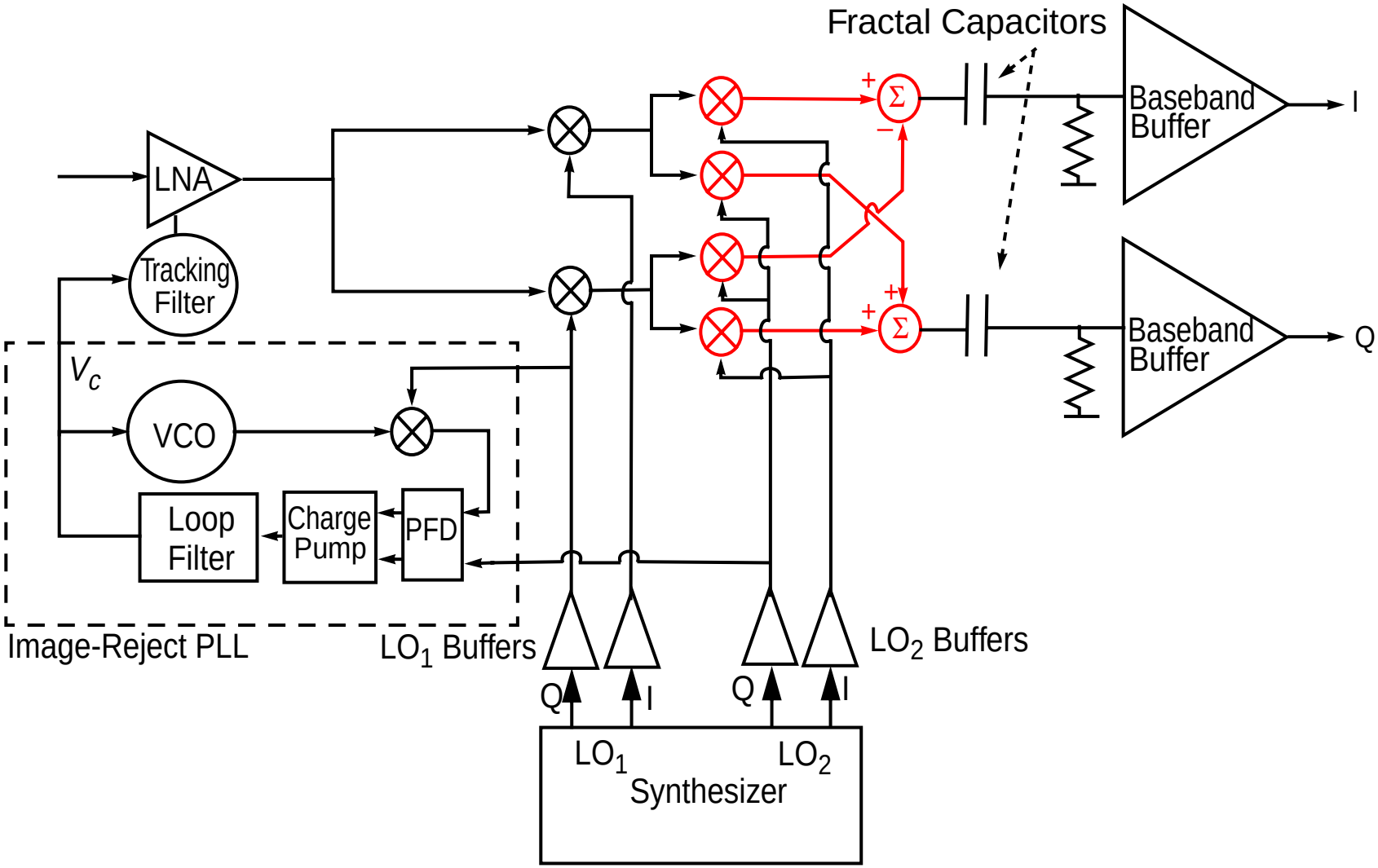
Receiver Architecture



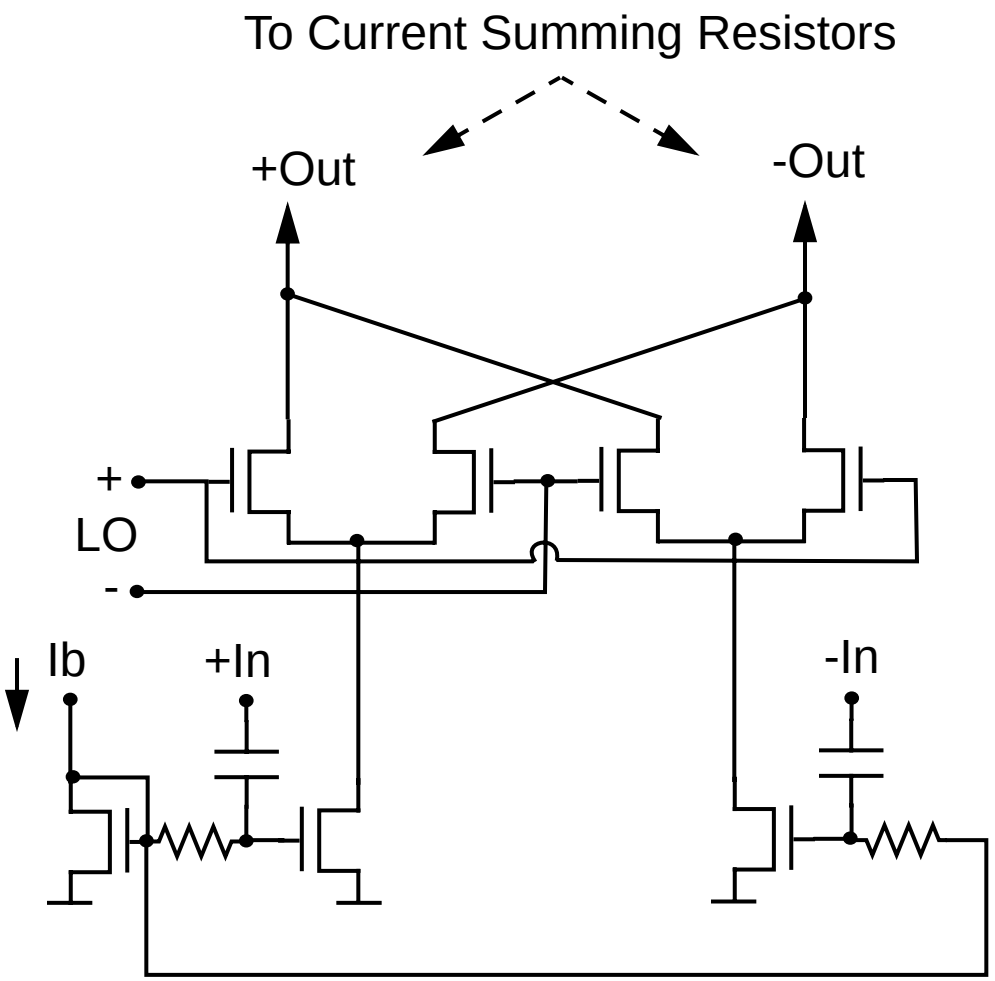
Circuit Implementation: VCO and Loop Mixer



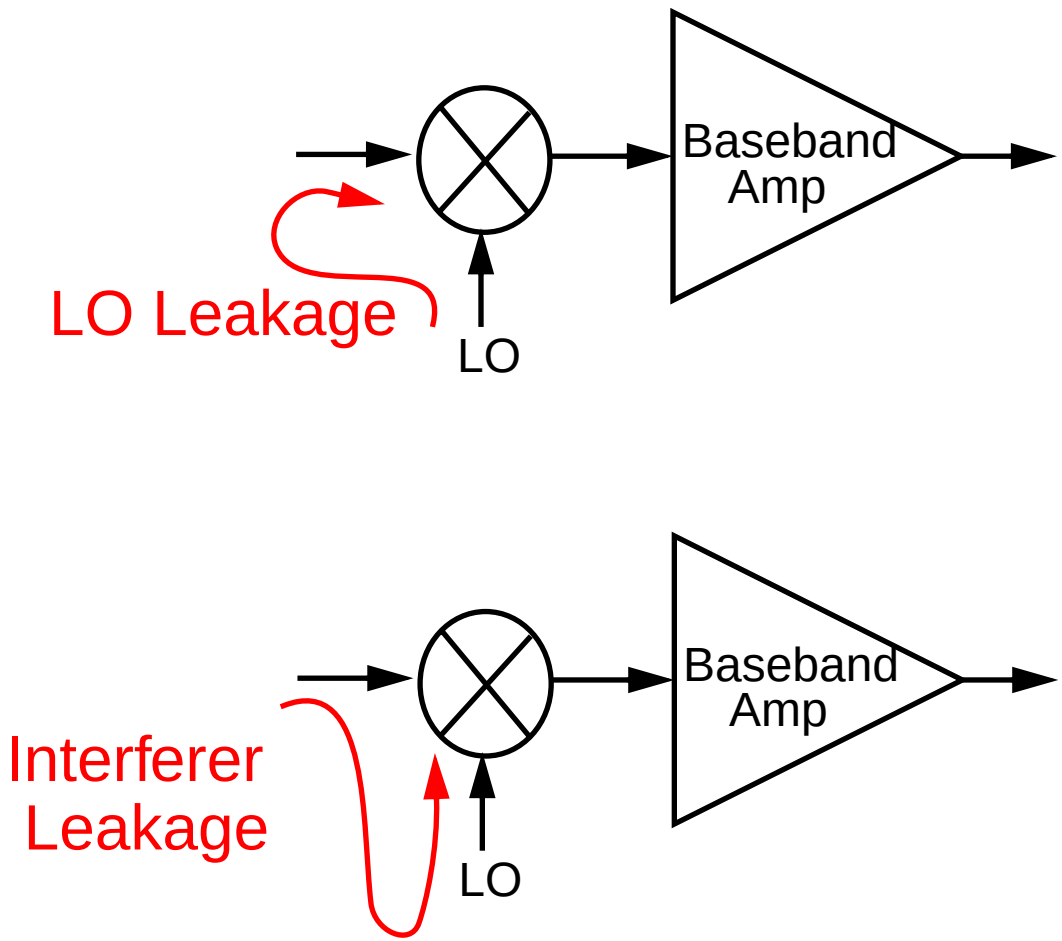
Receiver Architecture



Circuit Implementation: Second Mixers



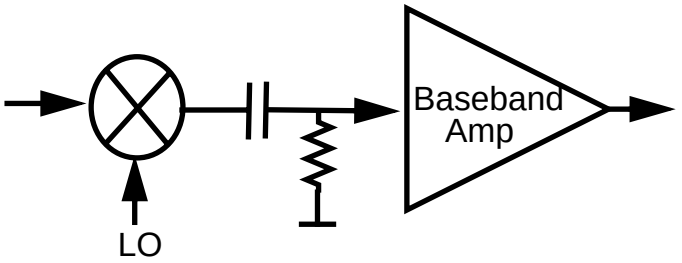
DC Offsets


Baseband
Amp
LO Leakage
LO
Baseband
Amp
Interferer
Leakage
LO

DC Offset Cancellation Techniques

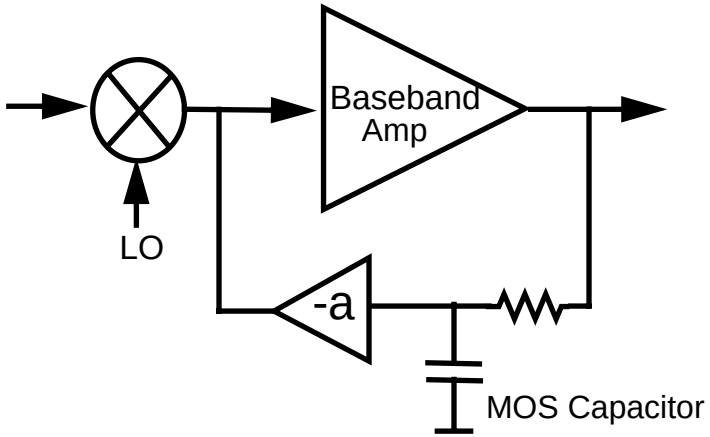
- Capacitive Coupling

  - Requires a large capacitor



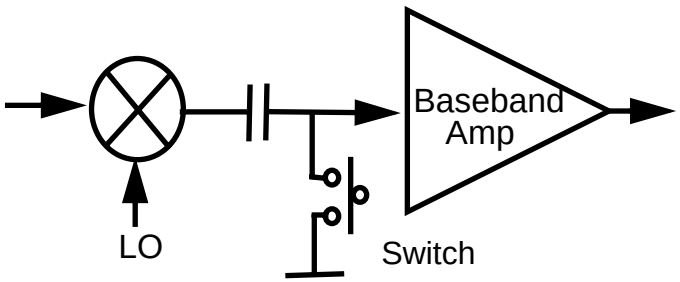
- Negative Feedback

  - Nonlinear



- TDMA offset Cancellation

  - Requires a large capacitor

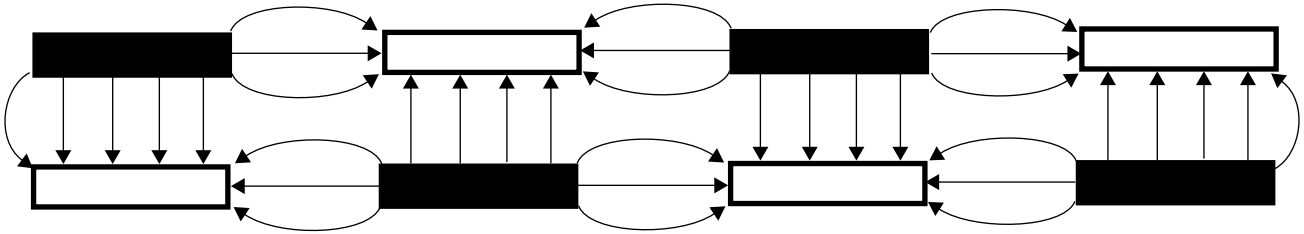


Traditional Capacitors

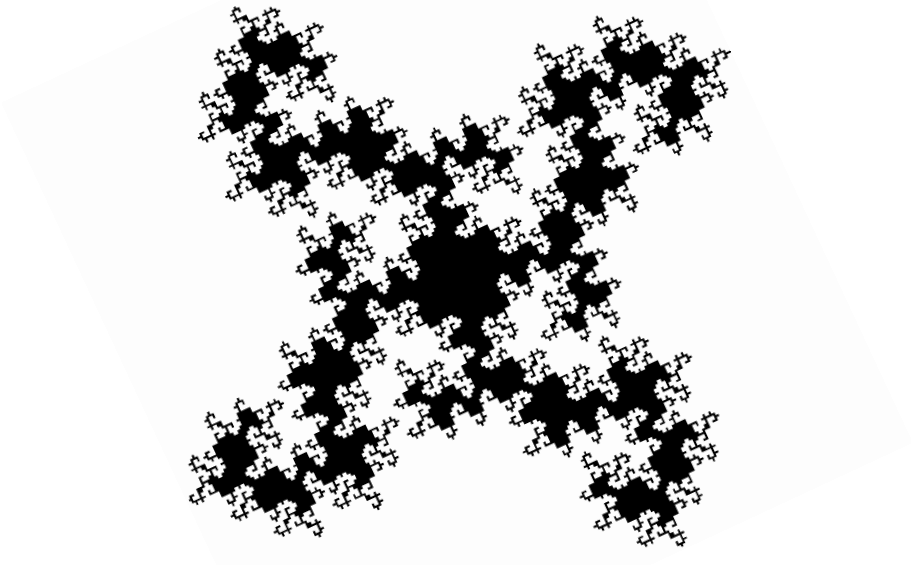
- Gate Capacitance:
  - High capacitance per unit area
  - Nonlinear
  - Requires DC bias voltage
  - Low breakdown voltage
  - Medium Q
- Junction Capacitance:
  - Highly nonlinear
  - Requires DC bias voltage
  - Sensitive to process variations
  - Low Q
  - Large temperature variation
- Metal to Metal / Poly Capacitance:
  - Linear
  - High Q
  - Small temperature variation
  - Low capacitance per unit area
- Thin-Insulator Capacitors:
  - Linear
  - Expensive
  - Not available in standard CMOS

Improving Capacitance Density

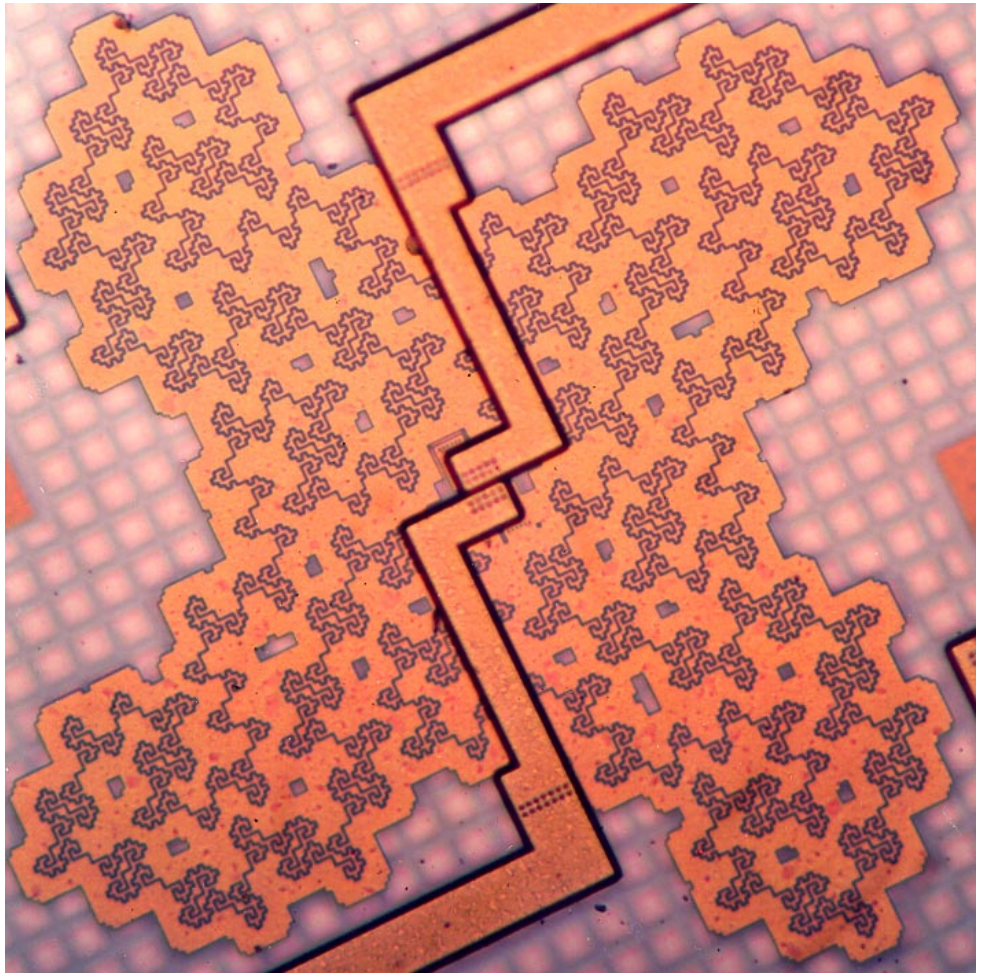
- Lateral flux improves capacitance density.



- Structures with large periphery are desirable.
- Some fractals have finite area but infinite perimeter.



Fractal Capacitor



# of cross-connected layers=4

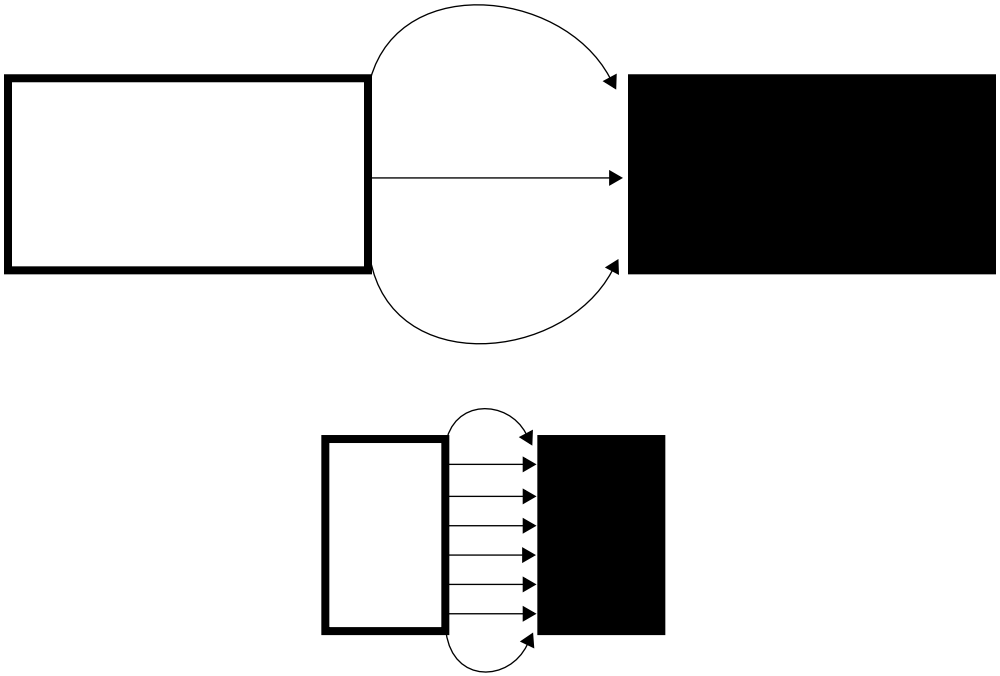
Horizontal spacing=0.6μm

Vertical spacing=0.8μm

Capacitance boost factor=2.3

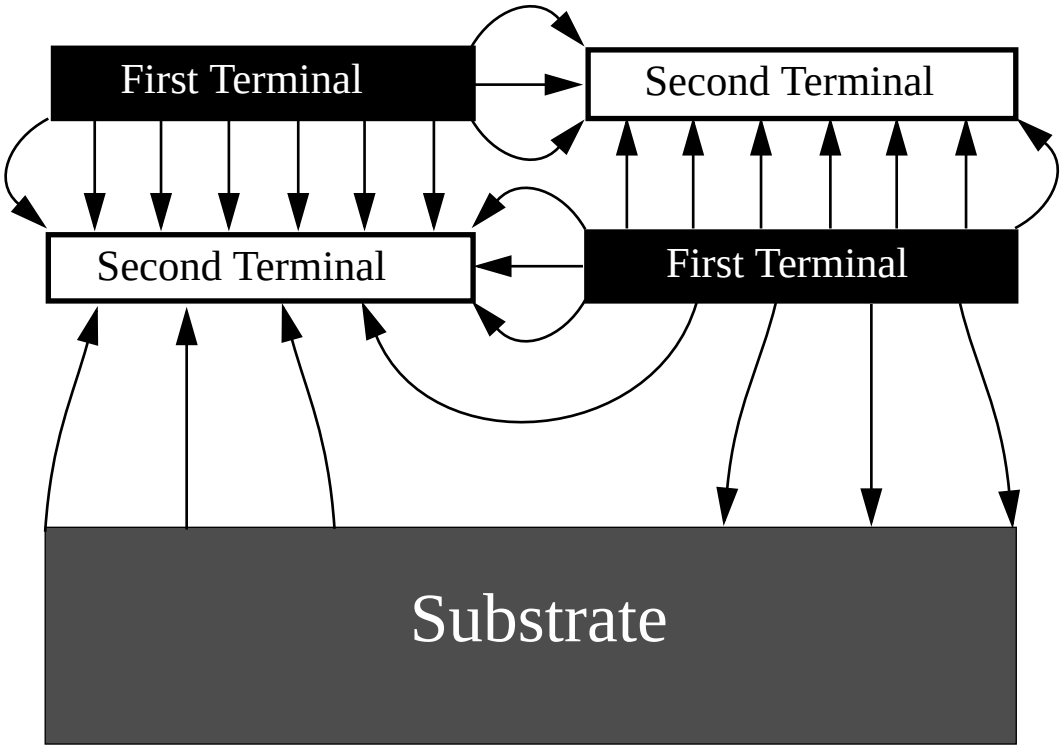
Scalability

- Unlike conventional parallel-plate structures, the capacitance per unit area increases as the process technologies scale.

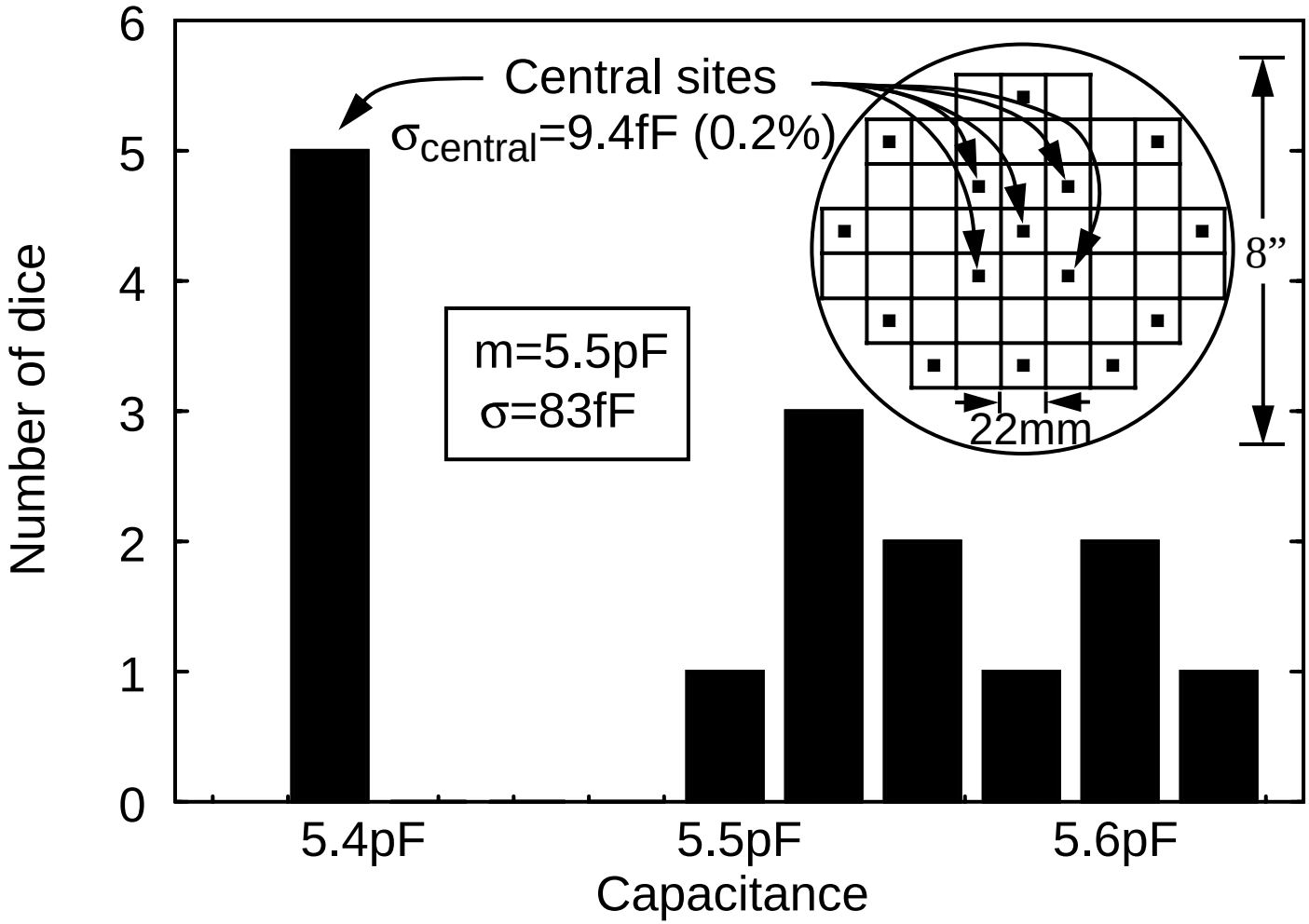


Reduction of the Bottom-Plate Capacitance

- Area is smaller.
- Some of the field lines terminate on the adjacent plate instead of the substrate.

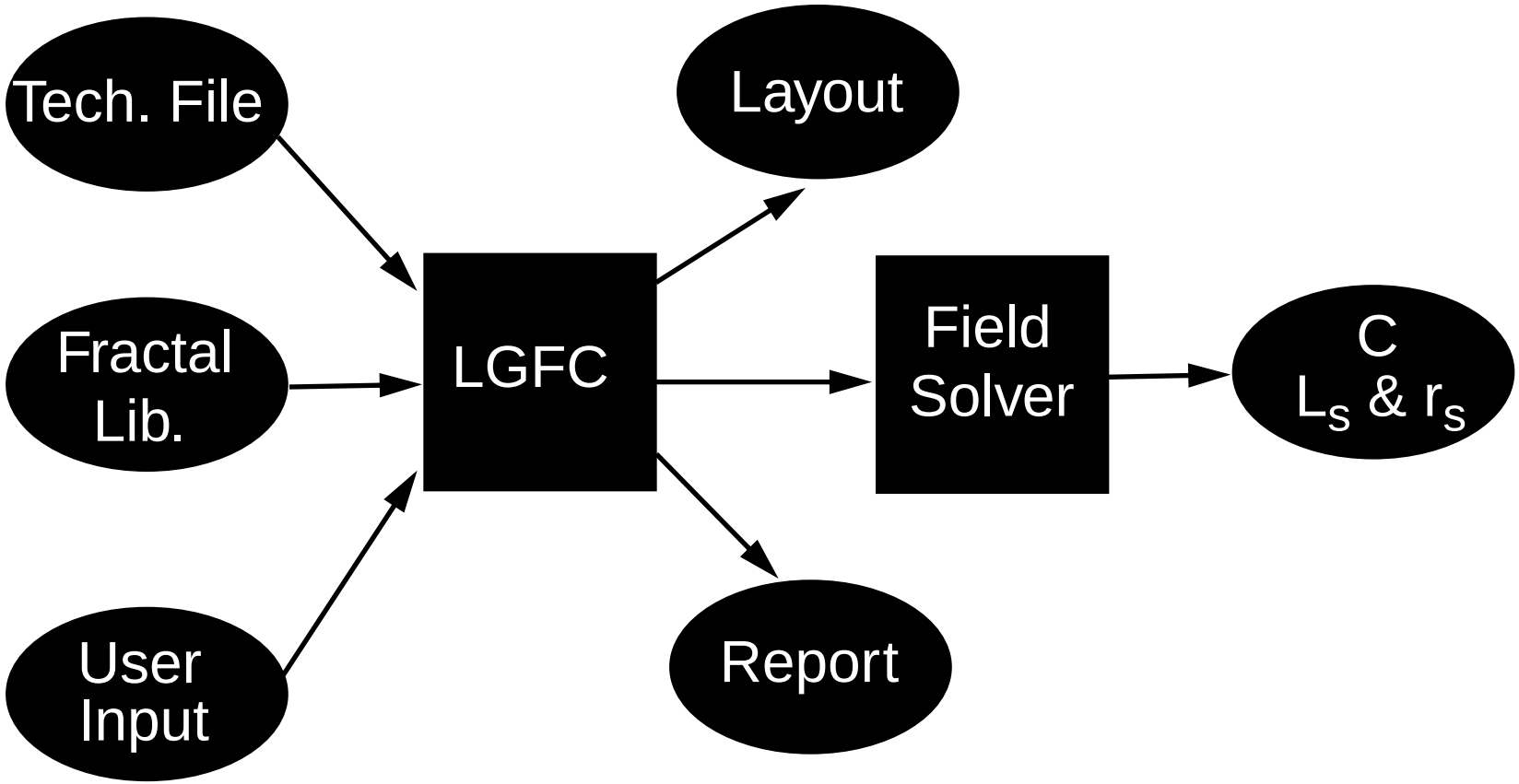


Improved Matching



Capacitance distribution across the wafer

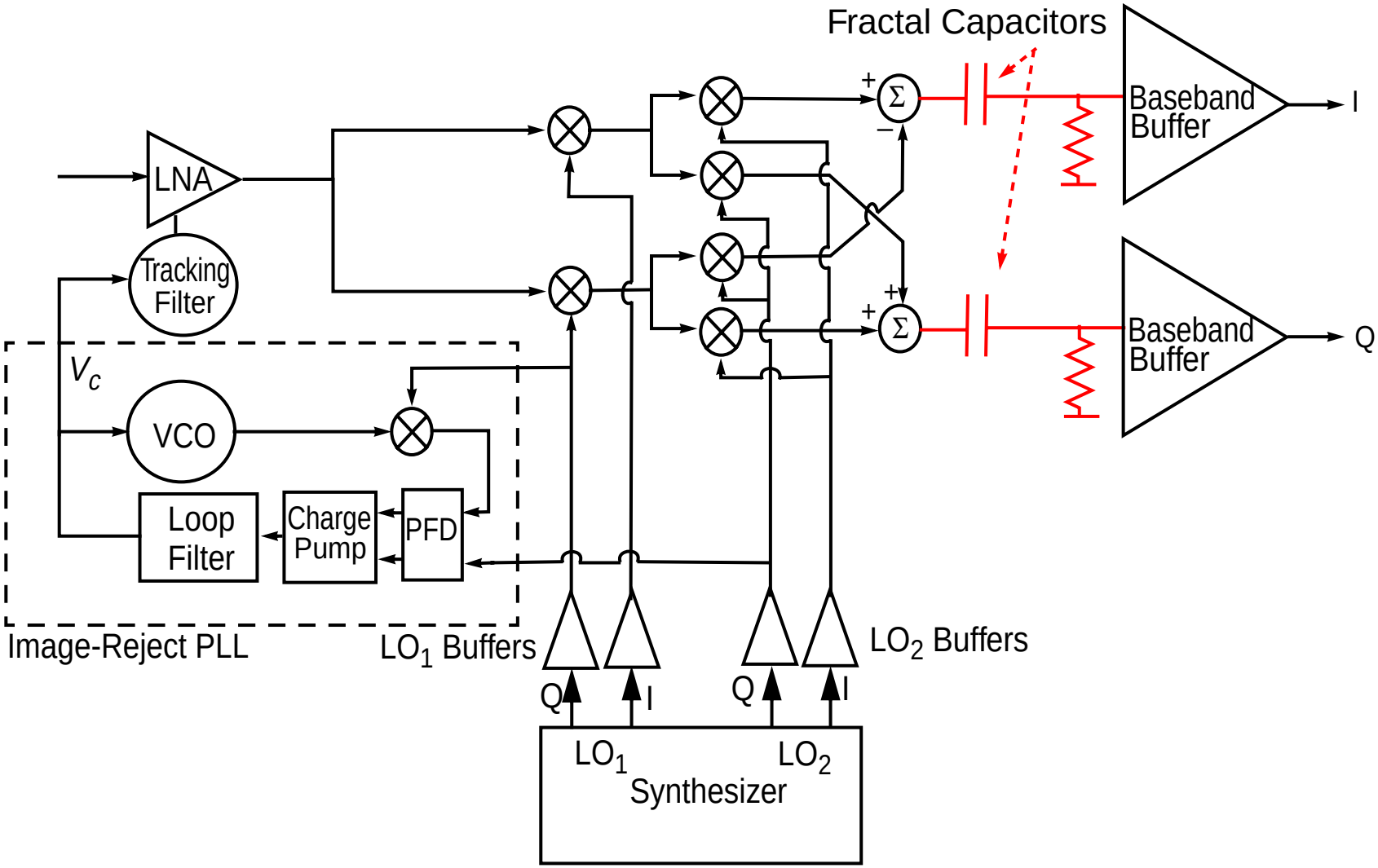
CAD Tool



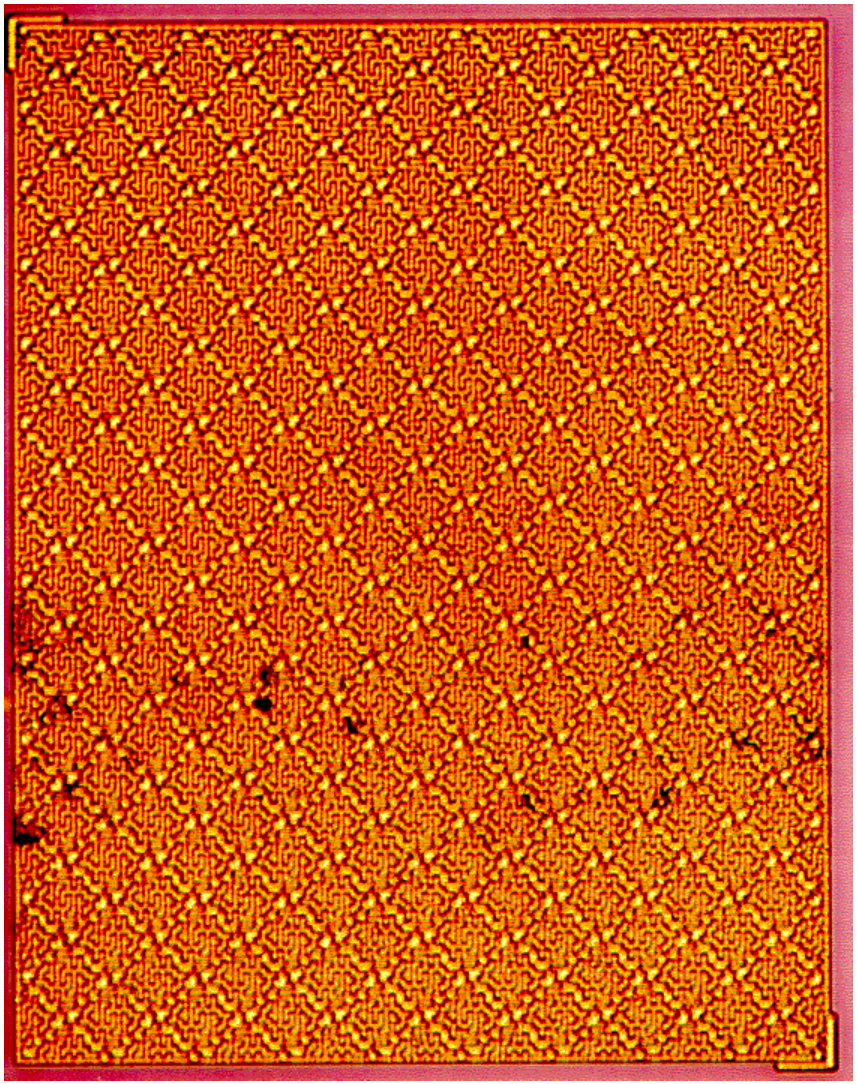
LGFC

Layout Generator for Fractal Capacitors

Receiver Architecture



Offset Cancellation Circuit

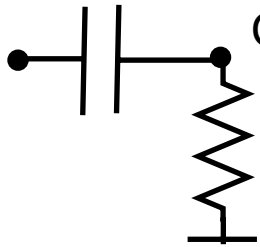


Capacitor

Area:131x165μm
Capacitance value:15pF
Bottom-plate capacitance/terminal:1.2pF
Self-resonance frequency:11.3GHz
Capacitance density: 700aF/μm^2
Capacitance boost factor:3.5

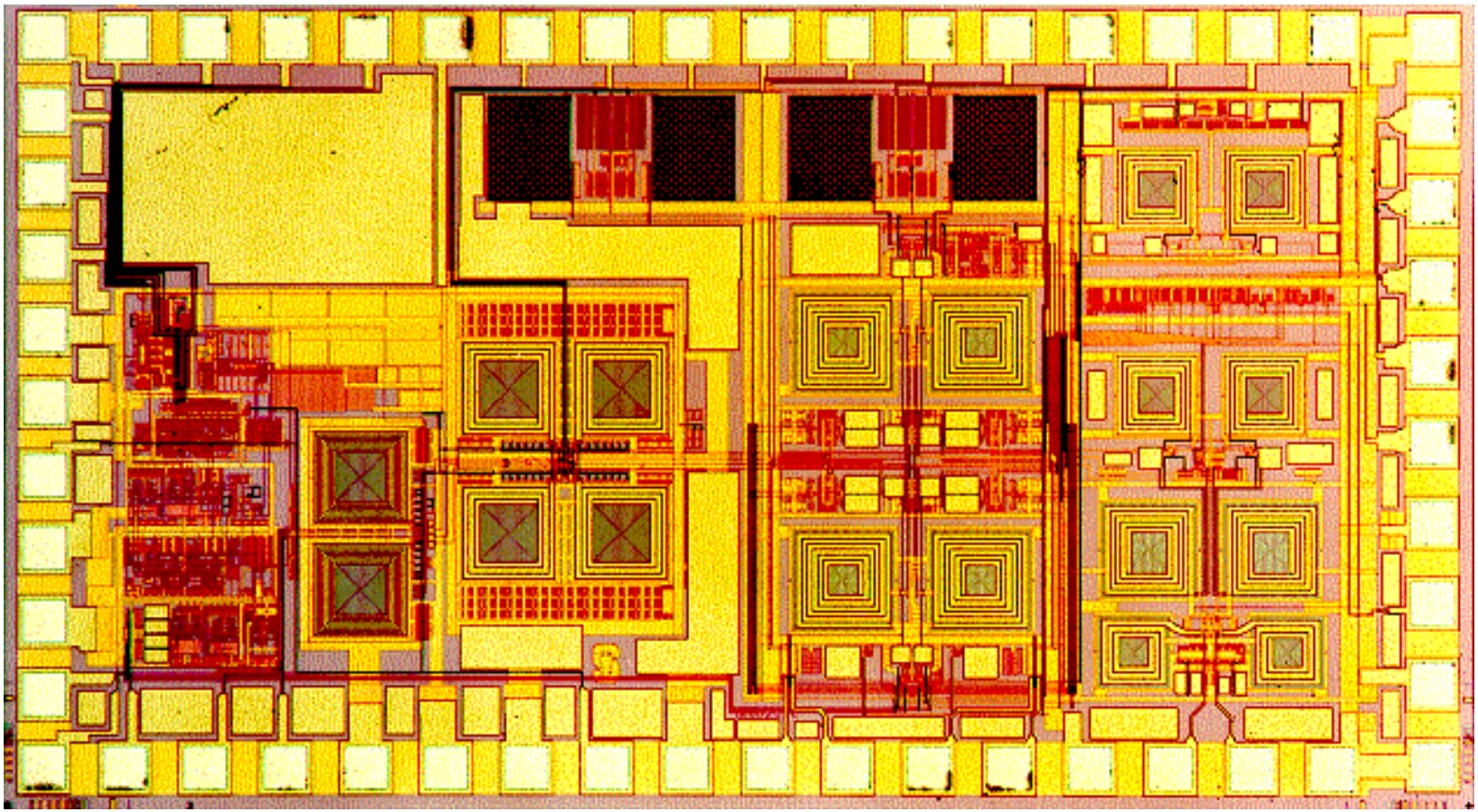
Resistor

Area: 103x61mm
Resistance value:2.1MΩ
Bottom-plate capacitance/terminal:0.3pF



Corner frequency
5kHz

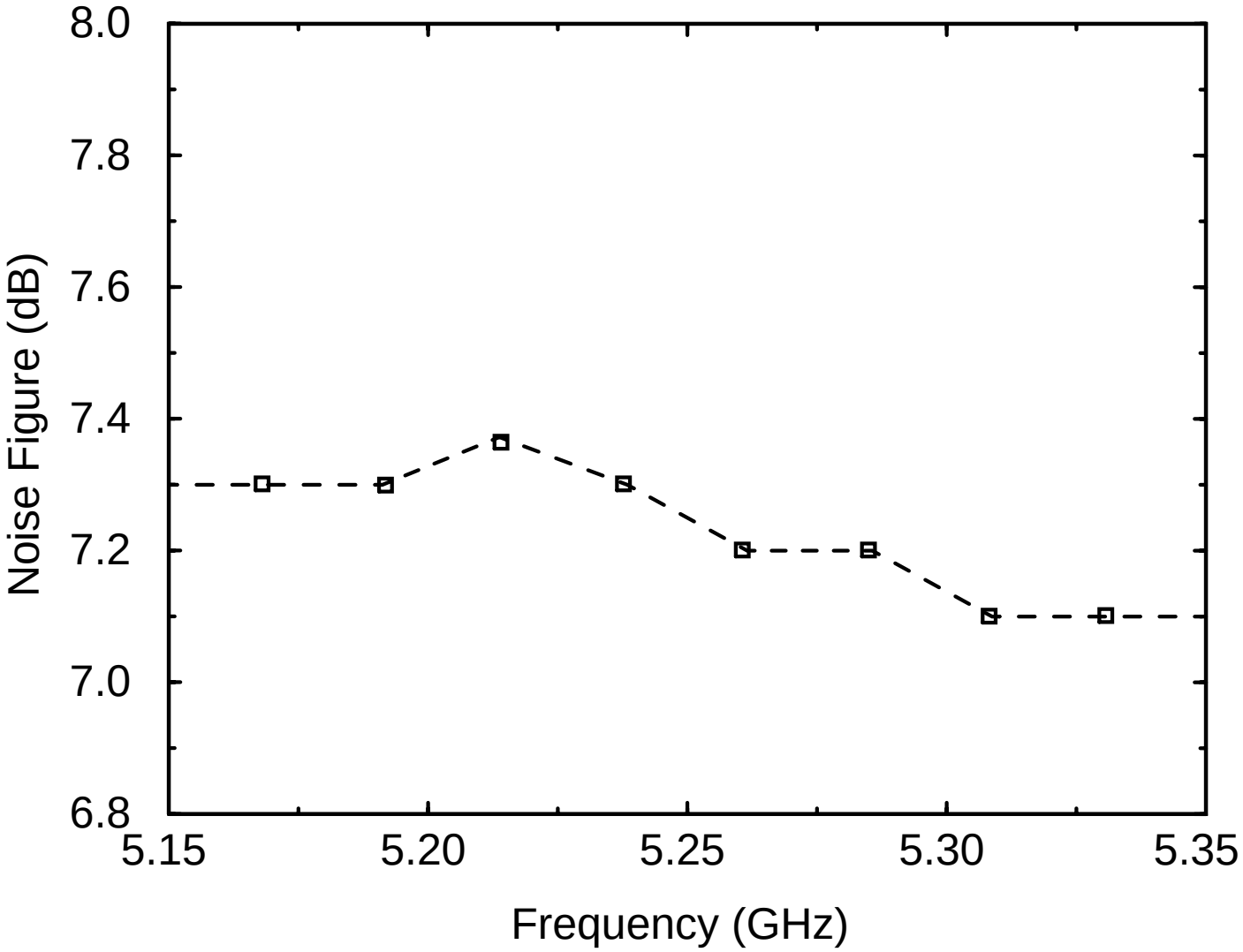
Die Micrograph



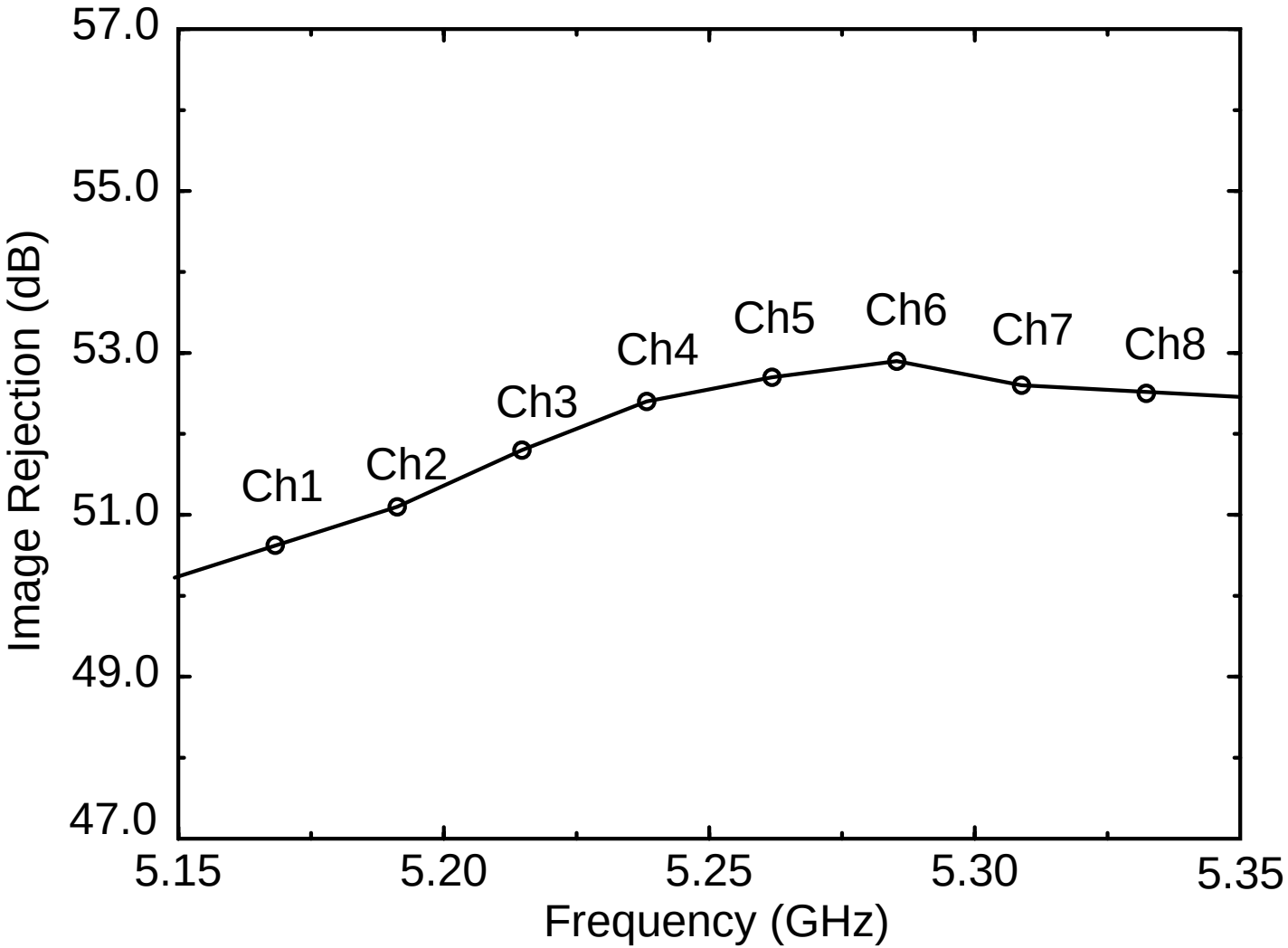
Die Area:4mm^2

Technology:0.24-μm CMOS

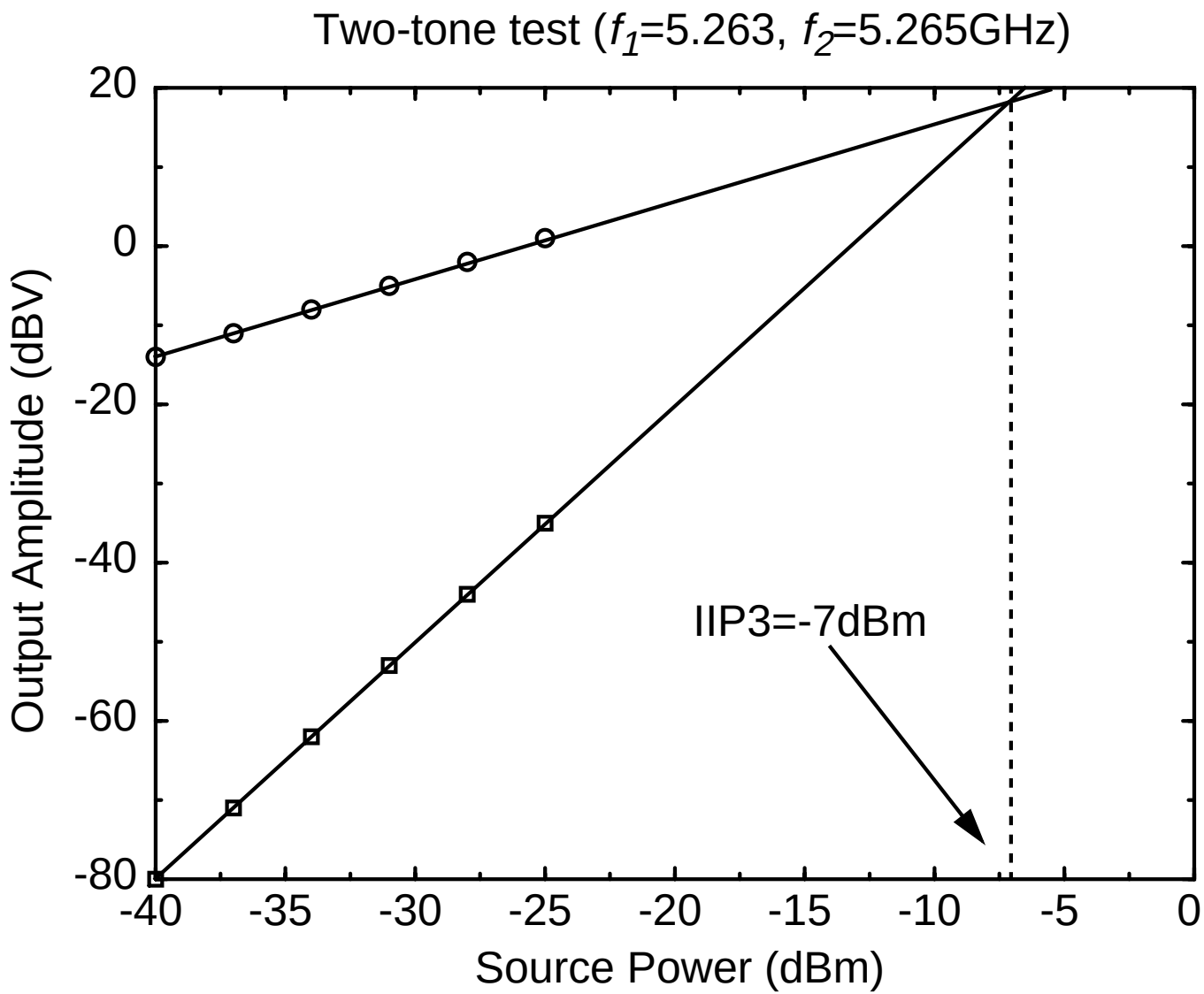
Measured Receiver NF



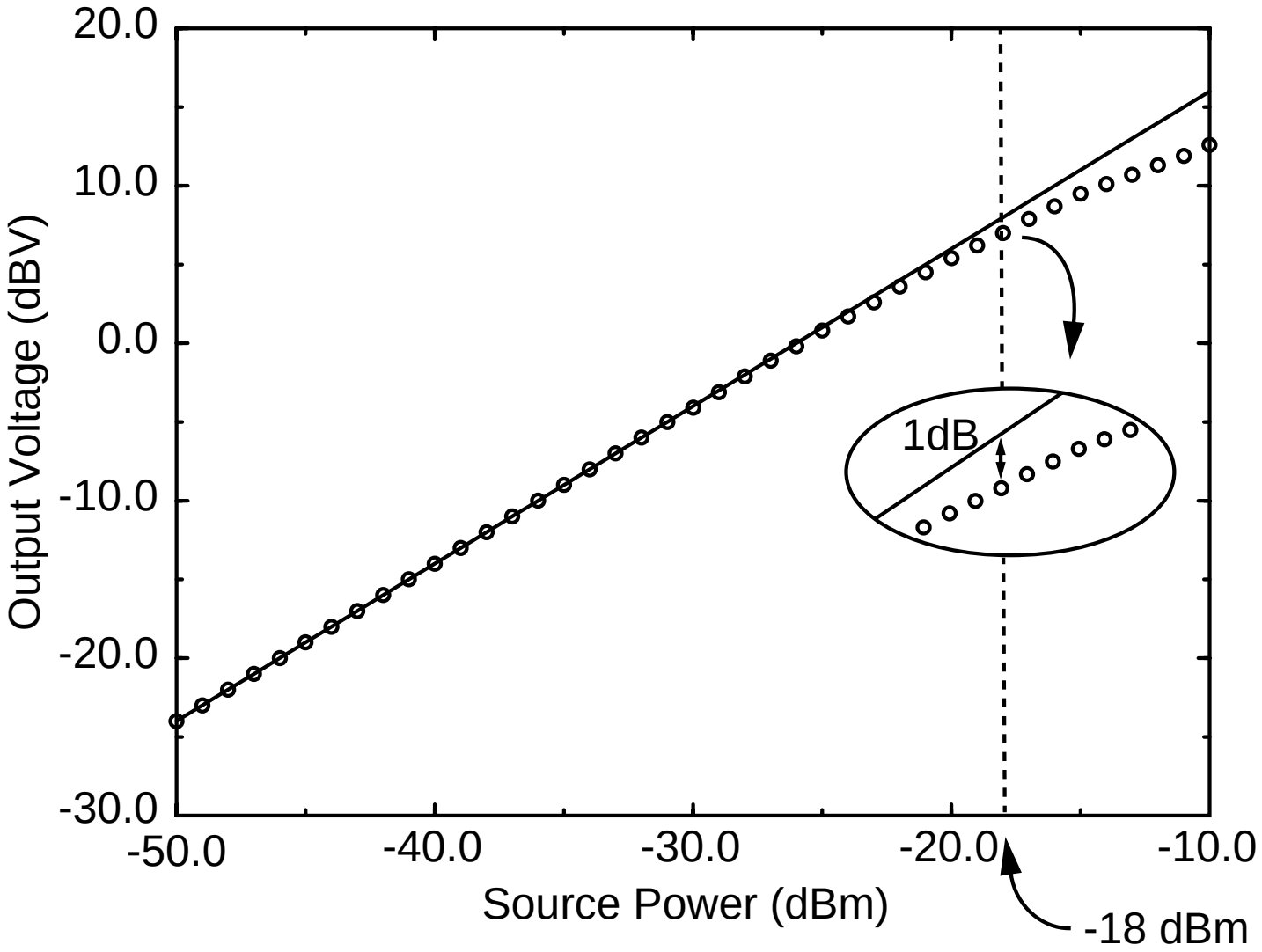
Measured Image Rejection



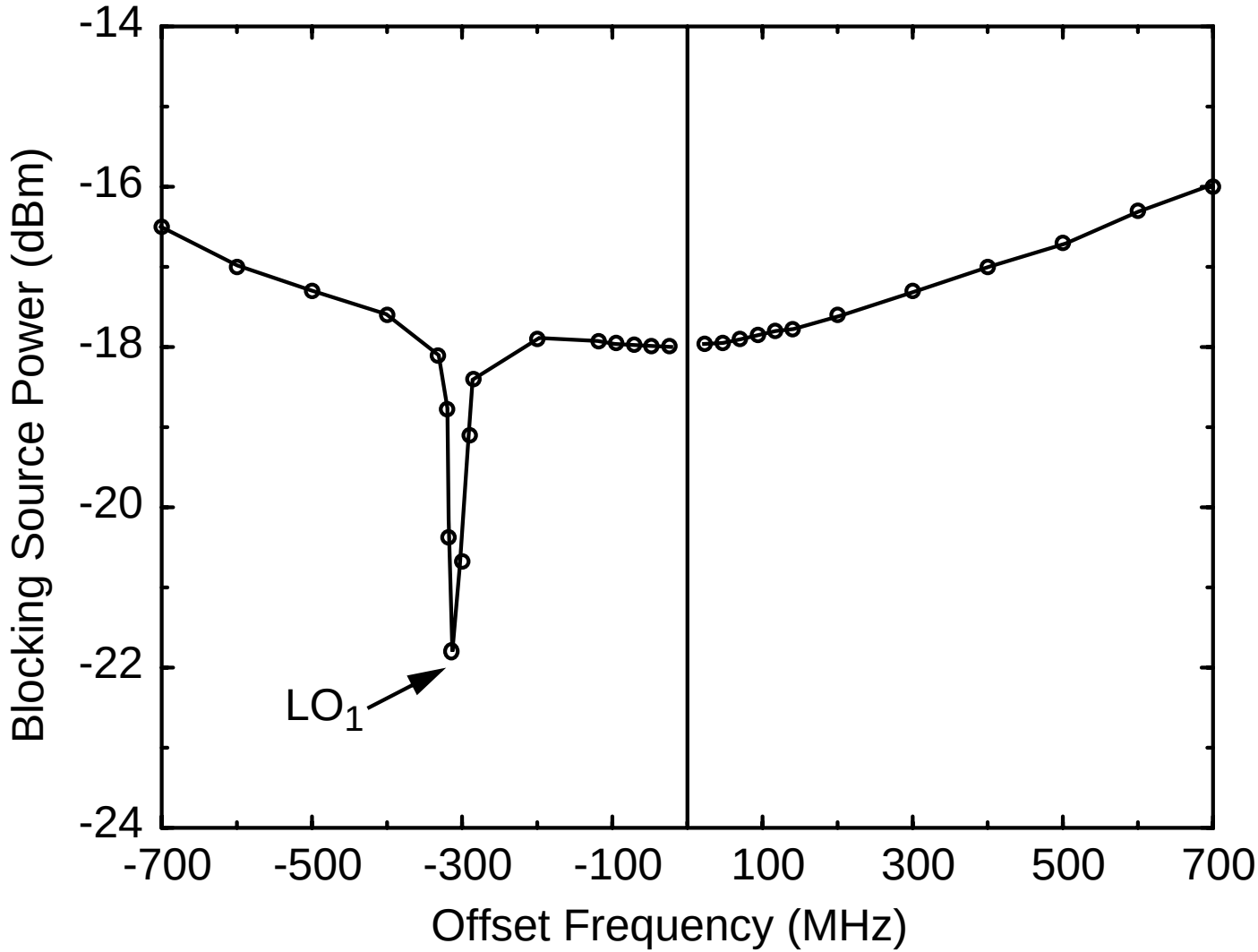
IP3 Measurement Results



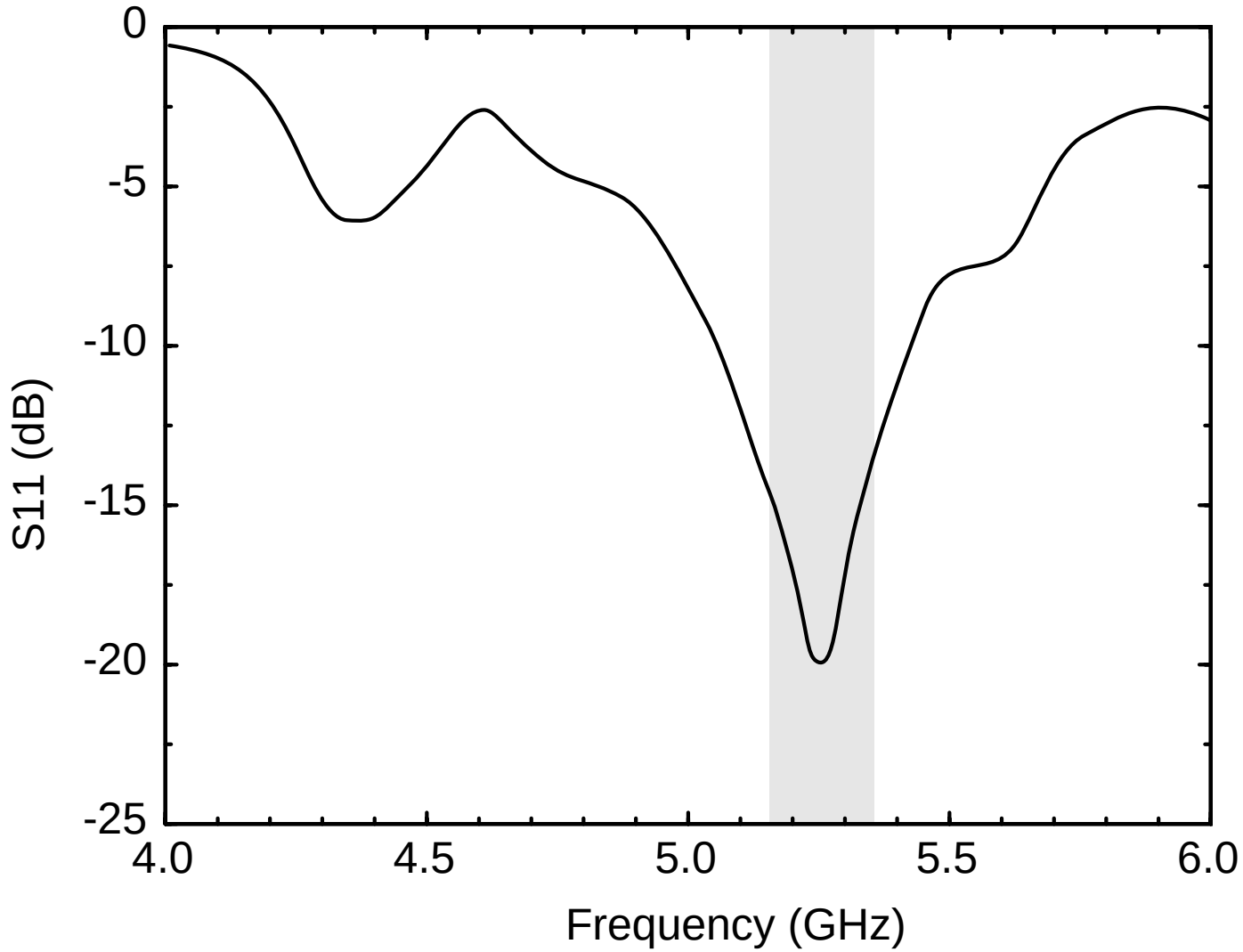
1-dB Compression-Point Measurement



1-dB Blocking Desensitization Point



Measured S11 of the Receiver



Measured Performance Summary

Signal path performance	**Achieved**	**Required**
Noise figure	7.2dB	18.3dB
Voltage gain	26dB	
S_{11}	< -14dB	
Image rejection (filter only)	16dB	
Image rejection (total)	53dB	
Input-referred IP3	-7dBm	
1-dB compression point	-18dBm	-21dBm
LO_1 Leakage to RF	-87dBm	-47dBm
LO_2 Leakage to RF	-88dBm	-57dBm
Power dissipation		
Synthesizer	25.3mW	
Divide-by-8 (for LO_2)	6.0mW	
Signal path	18.5mW	
Image-reject PLL	3.1mW	
LO buffers	5.0mW	
Biasing	0.9mW	
Total power	58.8mW	
Supply voltage	1.8V	
Implementation		
Die area	$4mm^2$	
Technology	0.24-μm CMOS	
Package	32-pin ceramic flat pack	

Contributions

- Implementing the first 5GHz CMOS wireless-LAN receiver.

  The receiver is:

  - highly integrated
  - low power
  - highly linear and tolerates large blockers

- Developing a novel RF filter topology that:

  - rejects the image signal
  - improves the LNA noise figure

- Demonstrating the feasibility of automatic tuning techniques at RF frequencies using a low power image-reject PLL.

Contributions

- Implementing a novel capacitor structure using fractal geometries.
- Demonstrating the benefits of fractal capacitors including:
  - area efficiency
  - linearity
  - scalability
  - reduced bottom-plate capacitance
  - improved matching characteristic
- Developing a CAD tool to automatically generate custom fractal layouts.