A CMOS Frequency Synthesizer with an Injection-Locked Frequency Divider for a 5 GHz Wireless LAN Receiver

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OUTLINE

- Motivation
- Introduction to wireless LAN
- Synthesizer architecture
- Synthesizer building blocks
- Summary and conclusion

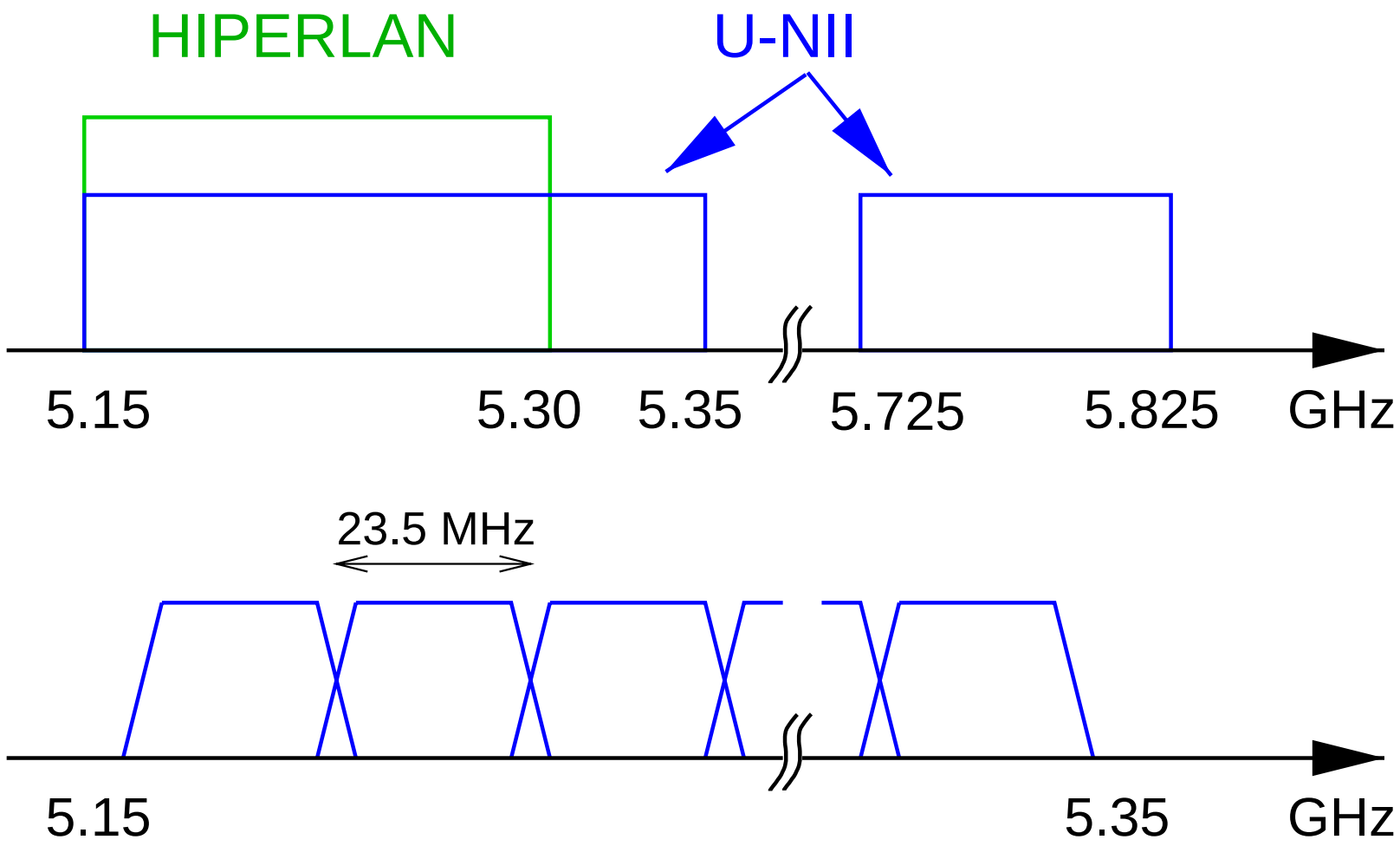
MOTIVATION

- Large demand for wideband wireless LAN systems
  - 20+ Mb/s data rate
  - Low cost
  - Low power
- New released frequency band
  - Unlicensed national information infrastructure (U–NII) band

GOAL

- Design a 5 GHz frequency synthesizer for a U–NII band wireless–LAN receiver (HIPERLAN compatible).
- Implement in CMOS.
- Minimize power consumption.

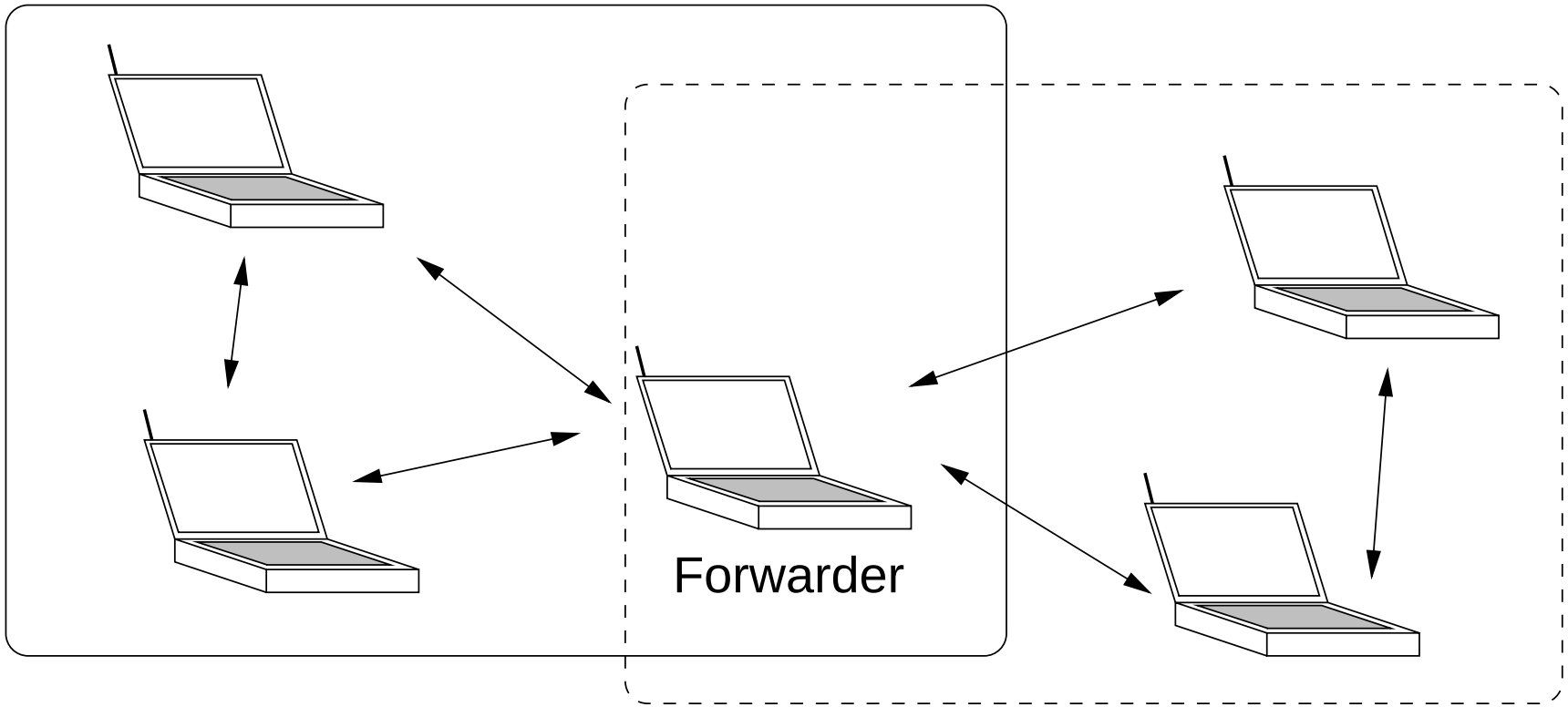
FREQUENCY OF OPERATION



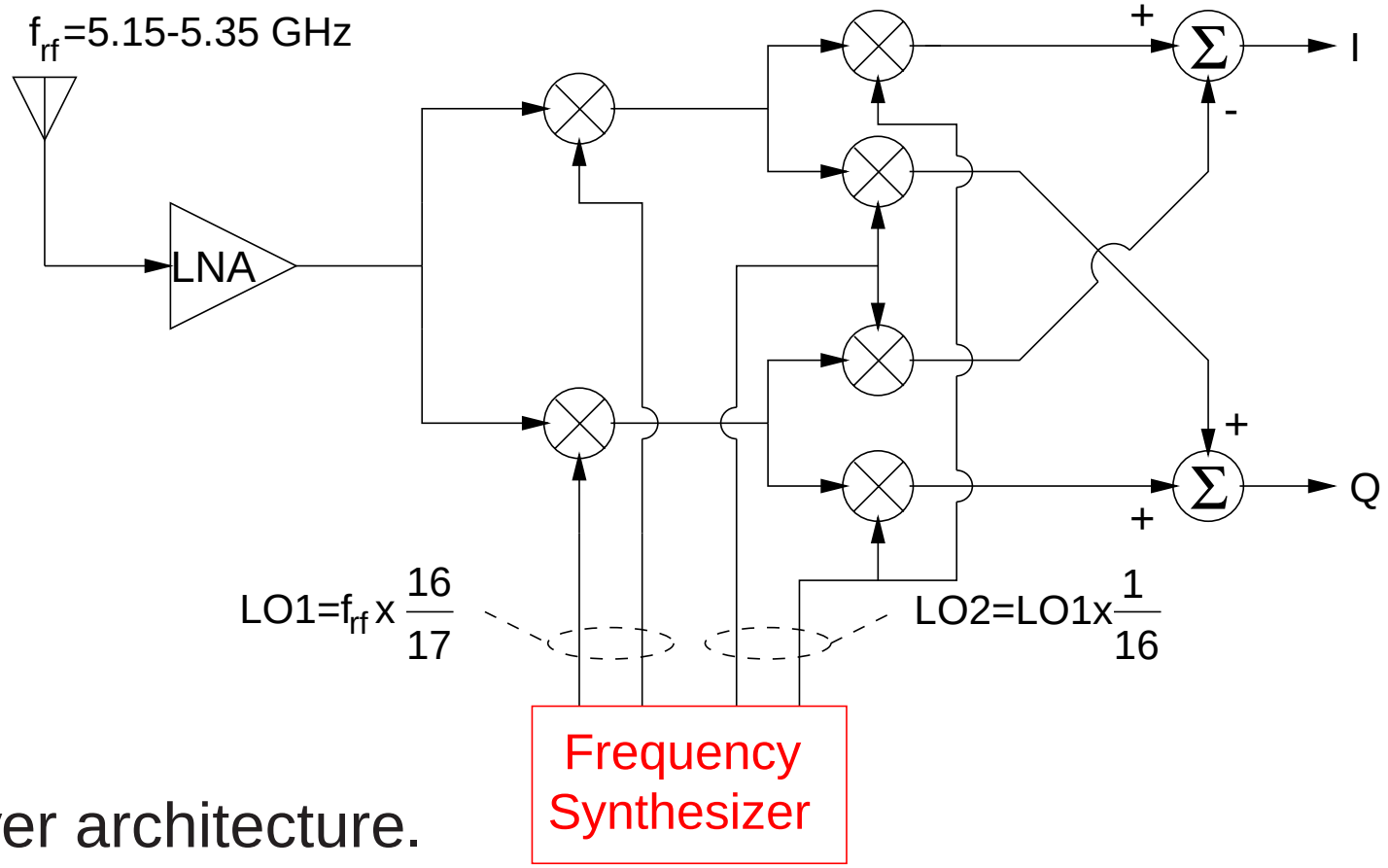
HIPERLAN/1 STANDARD

	Class A	Class B	Class C
Transmitter power	+10 dBm	+20 dBm	+30 dBm
Receiver sensitivity	-50 dBm	-60 dBm	-70 dBm
Maximum signal level	-25 dBm		
Modulation	GMSK (BT=0.3)		
Data rate	20 Mb/s		
Topology	multihop *ad hoc*		
Carrier switching time	$\leq$ 1 ms		
Channel bandwidth	23.5 MHz		

HIPERLAN MULTIHOP *ad hoc topology*

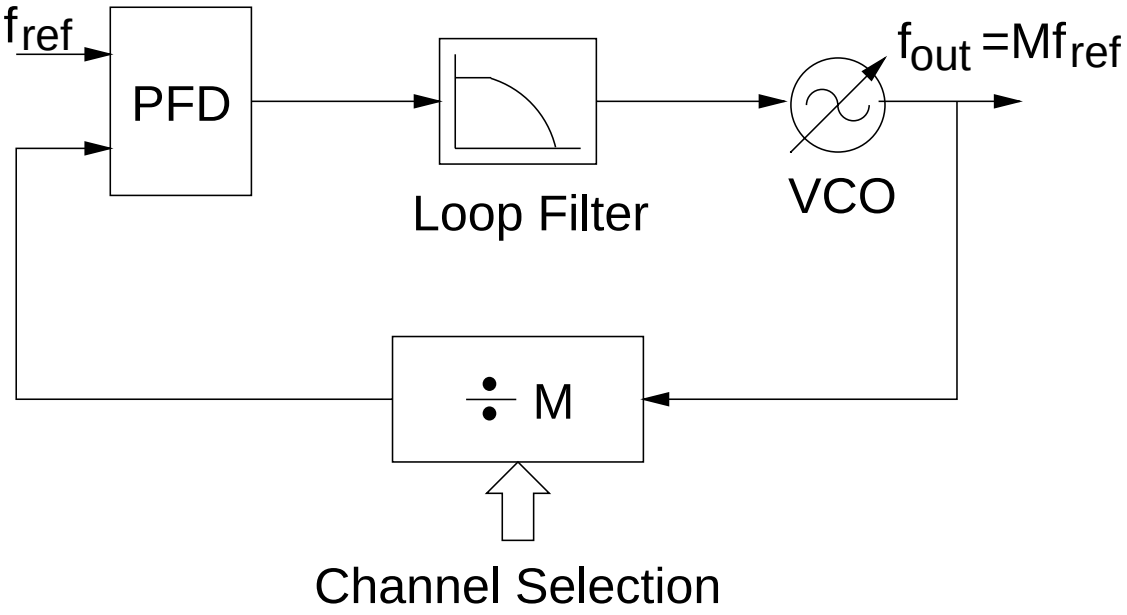


RECEIVER ARCHITECTURE



- Weaver architecture.
- Requires quadrature LO's to reject the image signal.

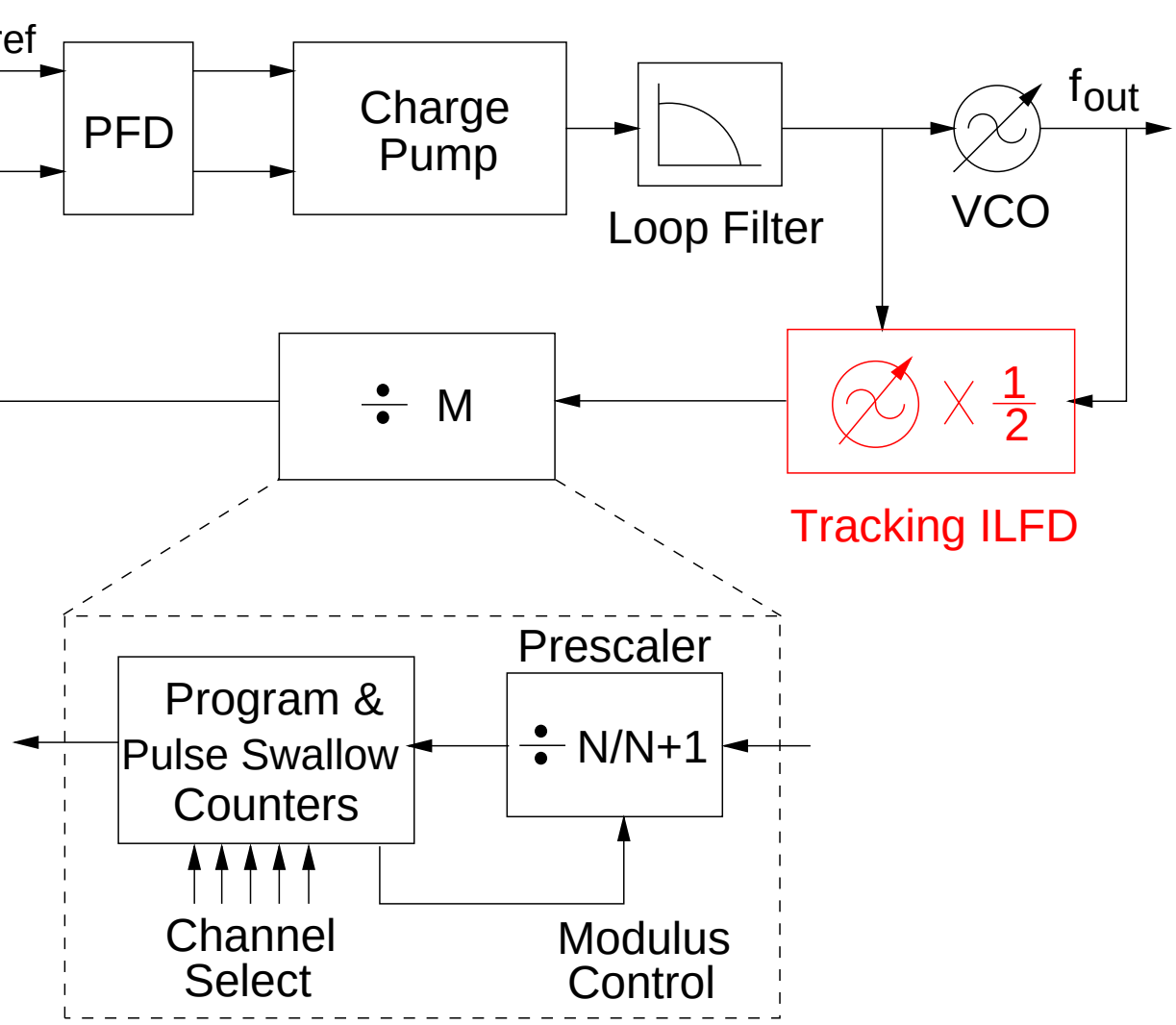
TYPICAL PLL–BASED FREQUENCY SYNTHESIZER



- Reference is a crystal oscillator.
- $f_{out} = \mathrm{M} \times f_{ref}$
- Multiple LO frequencies are generated by changing M.
- Frequency dividers are power hungry.
  - Their power consumption increases with frequency.

Proposed PLL architecture

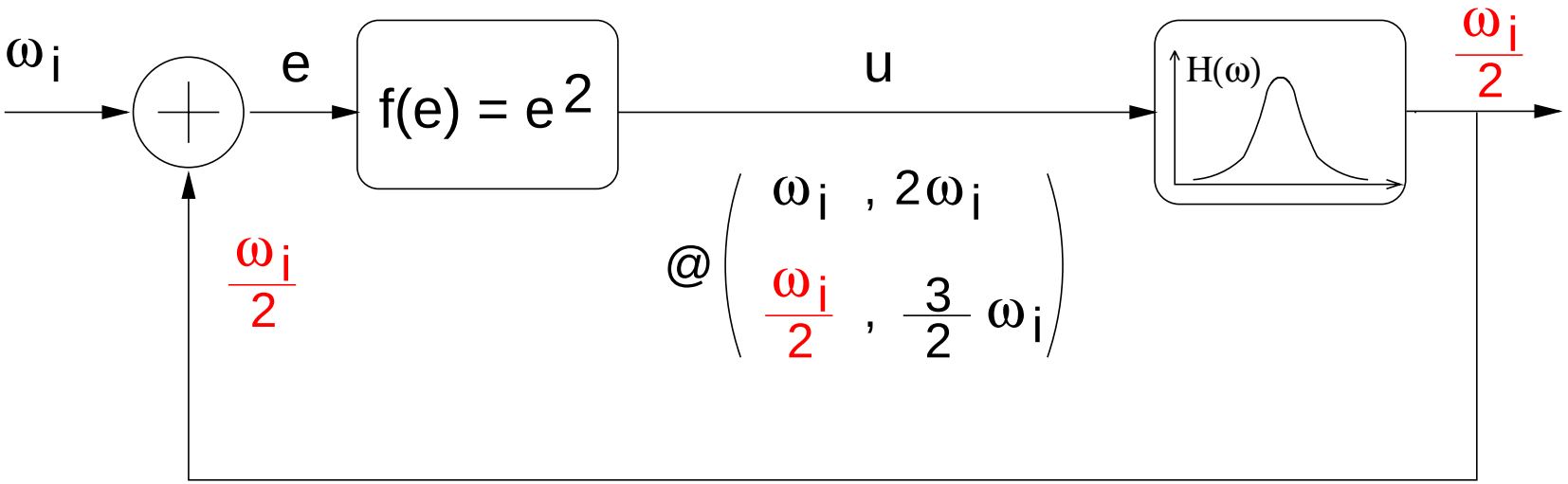
- f_{ref}=11 MHz
- f_o=4.840–4.994 GHz
- 8 channels
- M=220–227
- N=8



INJECTION LOCKING

- By impressing an oscillator with an external (incident) signal, frequency locking can be achieved.
  - First-harmonic injection locked oscillators ($\frac{f_i}{f_o} = 1$).
  - Subharmonic injection locked oscillators ($\frac{f_i}{f_o} = \frac{1}{N}$).
  - Superharmonic injection locked oscillators ($\frac{f_i}{f_o} = N$). Injection–locked frequency dividers (ILFDs).

ILFD SIMPLIFIED PICTURE



- Intermodulation of the input and output is the base of frequency division in an ILFD.
- An ILFD is an oscillator with perturbed oscillation.
  - Oscillation conditions should be satisfied in the presence of the incident signal.

Special case (divide–by–two)

$$f(e) = a_0 + a_1 e + a_2 e^2 + a_3 e^3$$

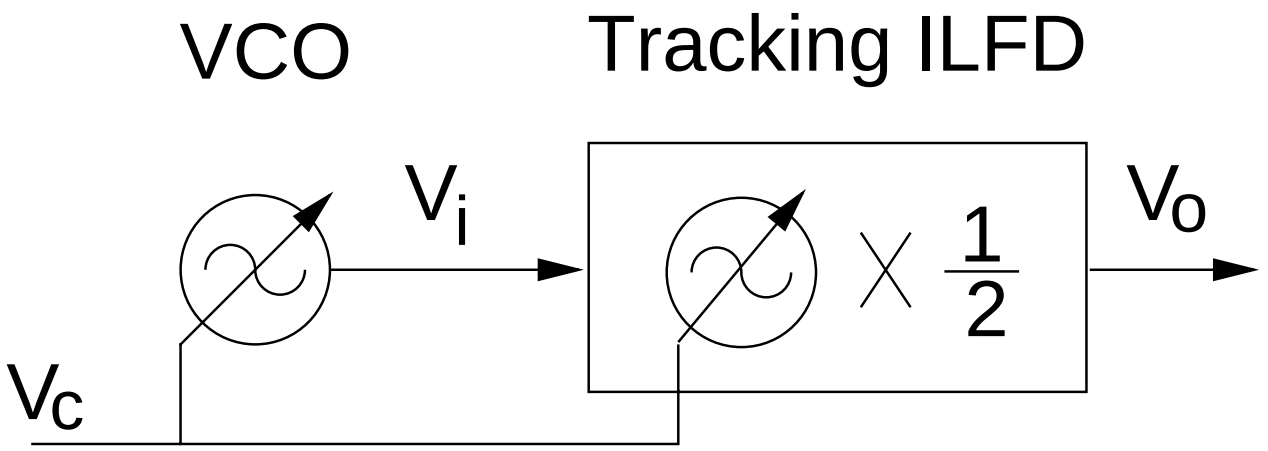
- Condition 1:

$$|\frac{\Delta\omega}{\omega_r}| < |\frac{H_0 a_2 V_i}{2Q}| \qquad , \qquad \frac{H_0}{Q} = \frac{LQ\omega_r}{Q} = L\omega_r$$

- Condition 2:

$$H_0(a_1 + \frac{3}{2}a_3 V_i^2 + a_2 V_i \cos(\phi)) < 1$$

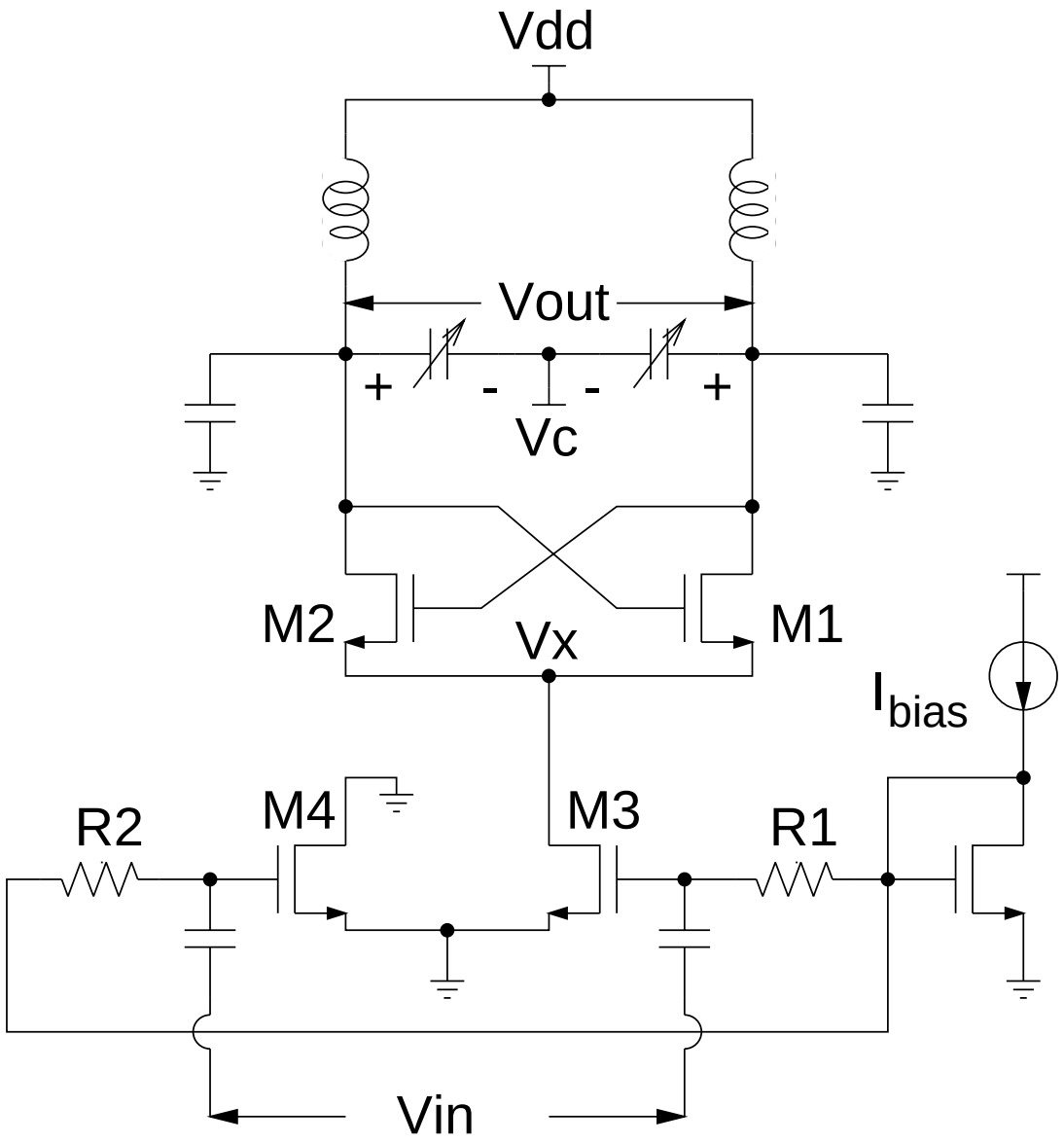
TRACKING ILFD



- Locking range extension

DIFFERENTIAL TRACKING ILFD

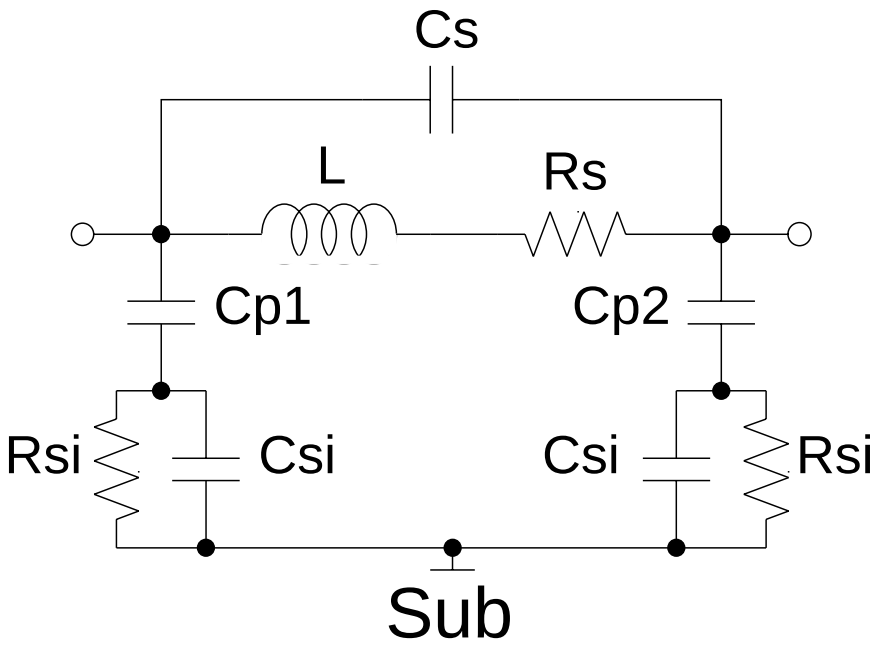
- 0.24 μm CMOS
- Vdd=1.5 V
- $\mathrm{I_{bias}}$=300 μA
- f_o=2.45 GHz
- f_i=4.9 GHz

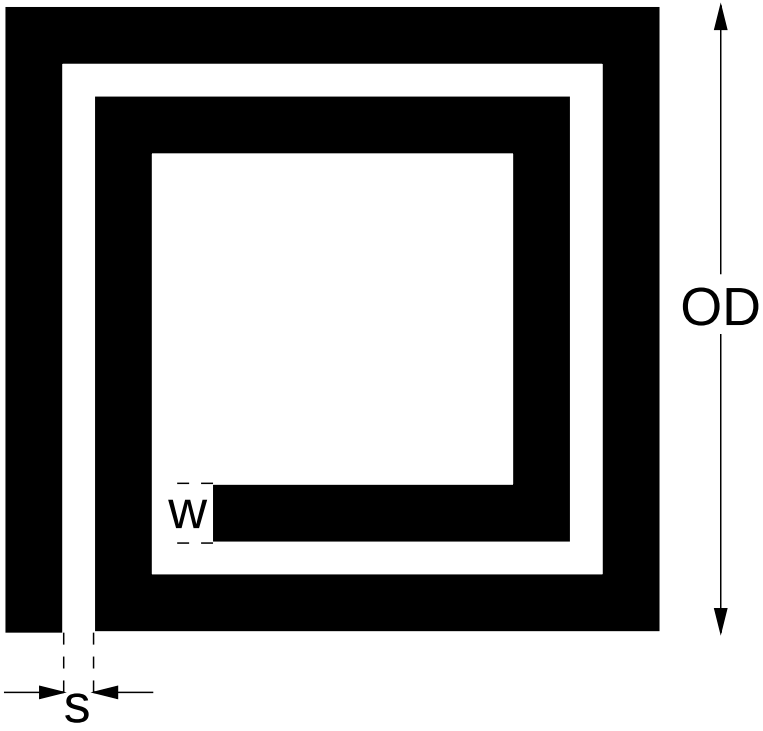


INDUCTOR DESIGN (ILFD)

- Maximum locking range $\Rightarrow$ maximize L
- Minimum power consumption $\Rightarrow$ maximize LQ

INDUCTOR DESIGN





- Design parameters:
  - w: metal width
  - s: metal spacing
  - OD: outer dimension
  - n: number of turns

INDUCTOR DESIGN (ILFD)

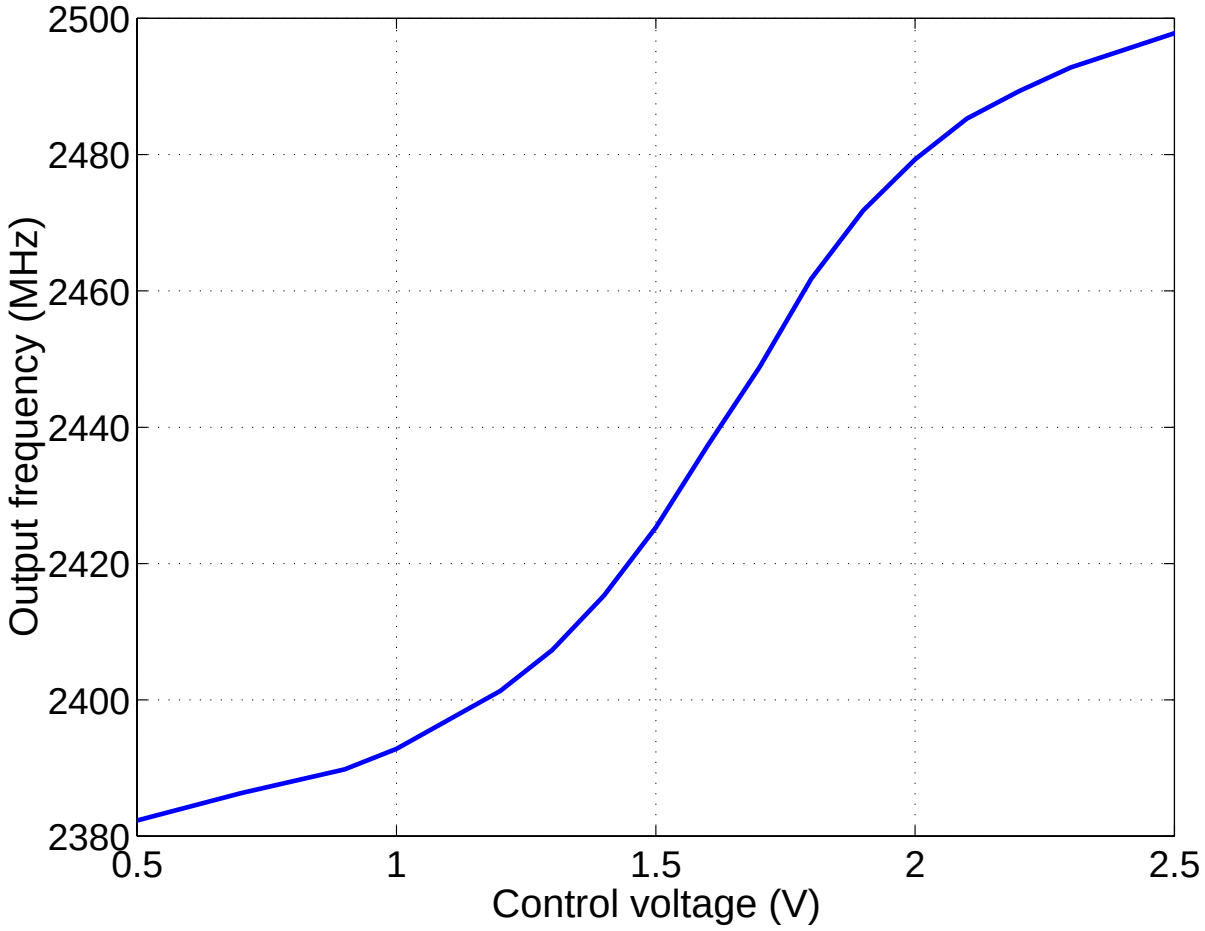
- In planar spiral inductors maximizing L does not maximize LQ

$$\Downarrow$$

maximize L for a given LQ

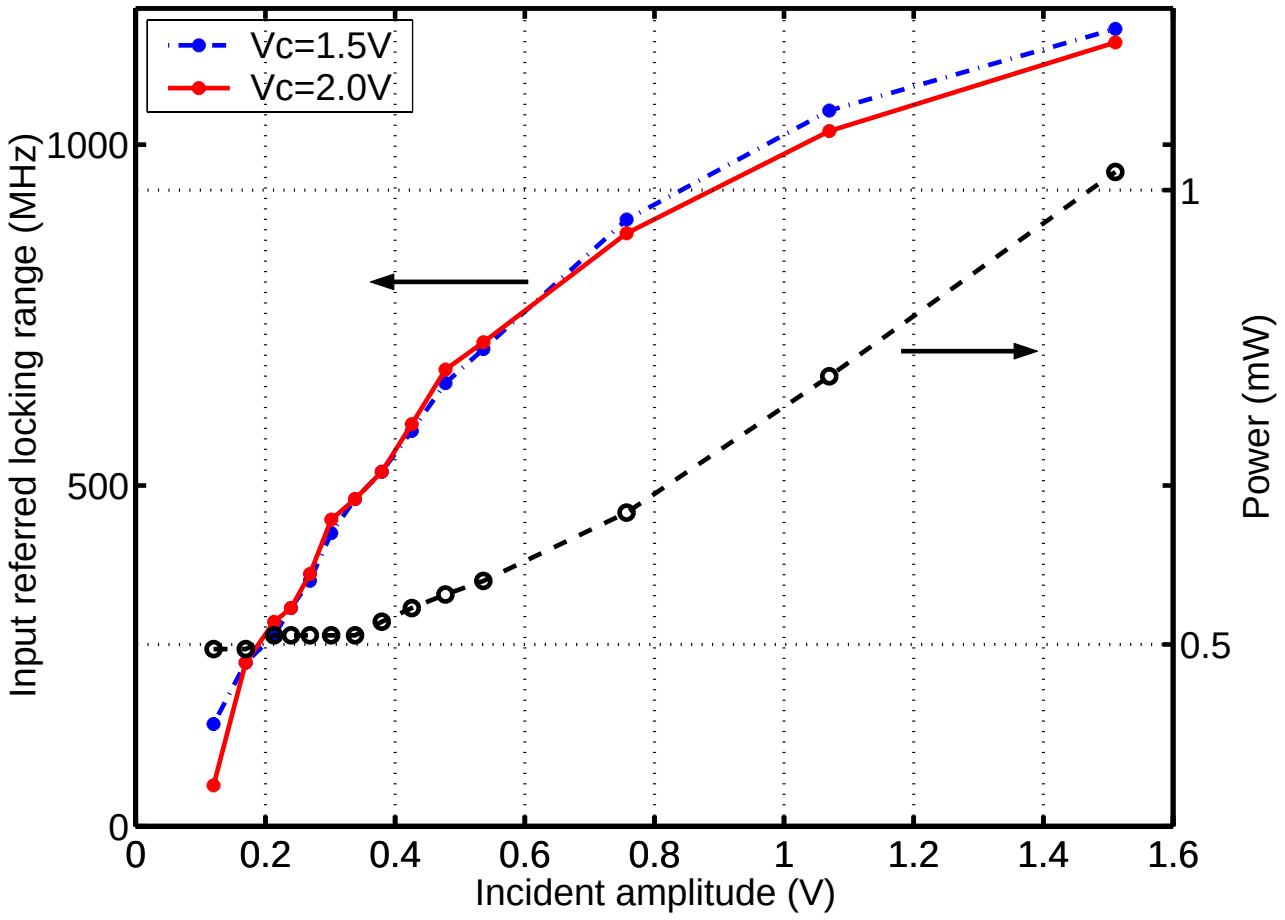
ILFD FREE–RUNNING OSCILLATION

- 0.24 μm CMOS
- Vdd=1.5 V
- $\mathrm{I_{bias}}$=300 μA
- Δf=110 MHz (5%)
- ΔV_c=2 V

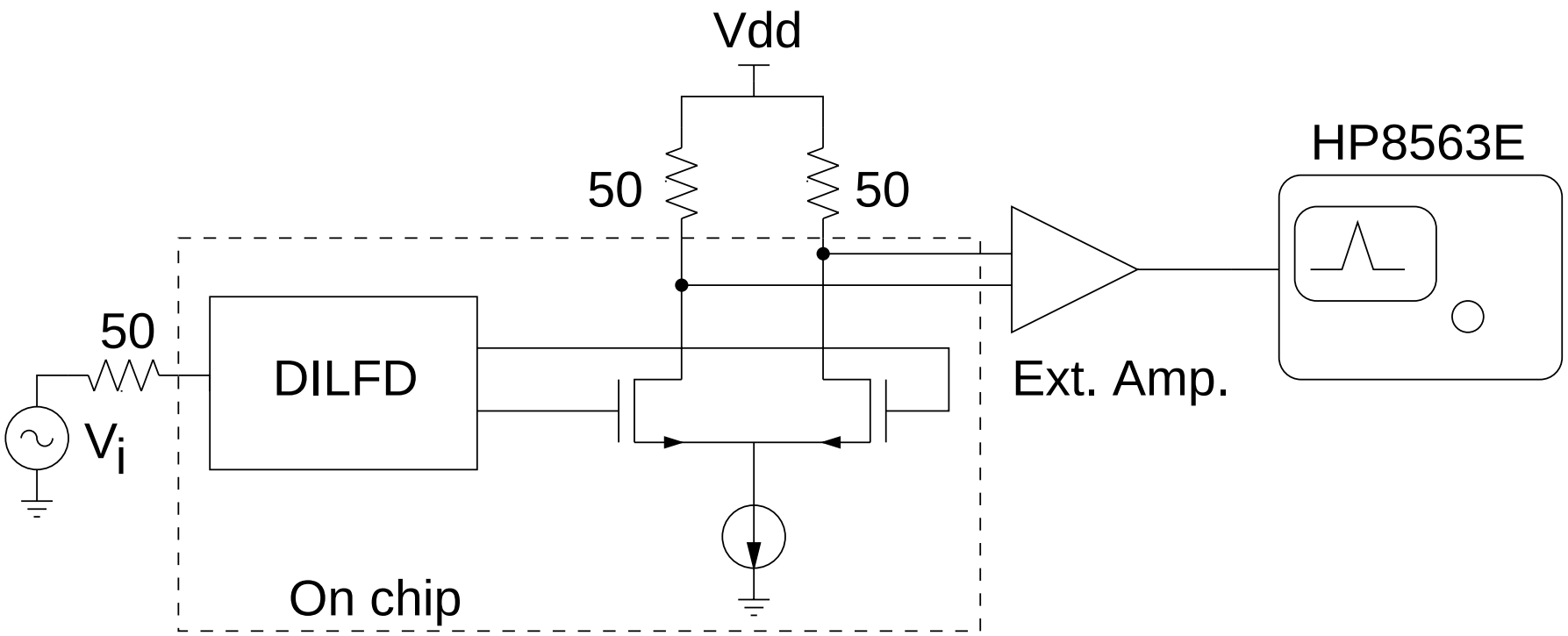


ILFD LOCKING RANGE/POWER CONSUMPTION

- 0.24 μm CMOS
- Vdd=1.5 V
- f_o=2.45 GHz
- f_i=4.9 GHz
- Δf=1 GHz
  @ 1 V ($\approx$ 20%)
- Power=0.75 mW
  @ 1 V



PHASE NOISE MEASUREMENT TEST SETUP



ILFD PHASE NOISE

- 0.24 μm CMOS
- Vdd=1.5 V
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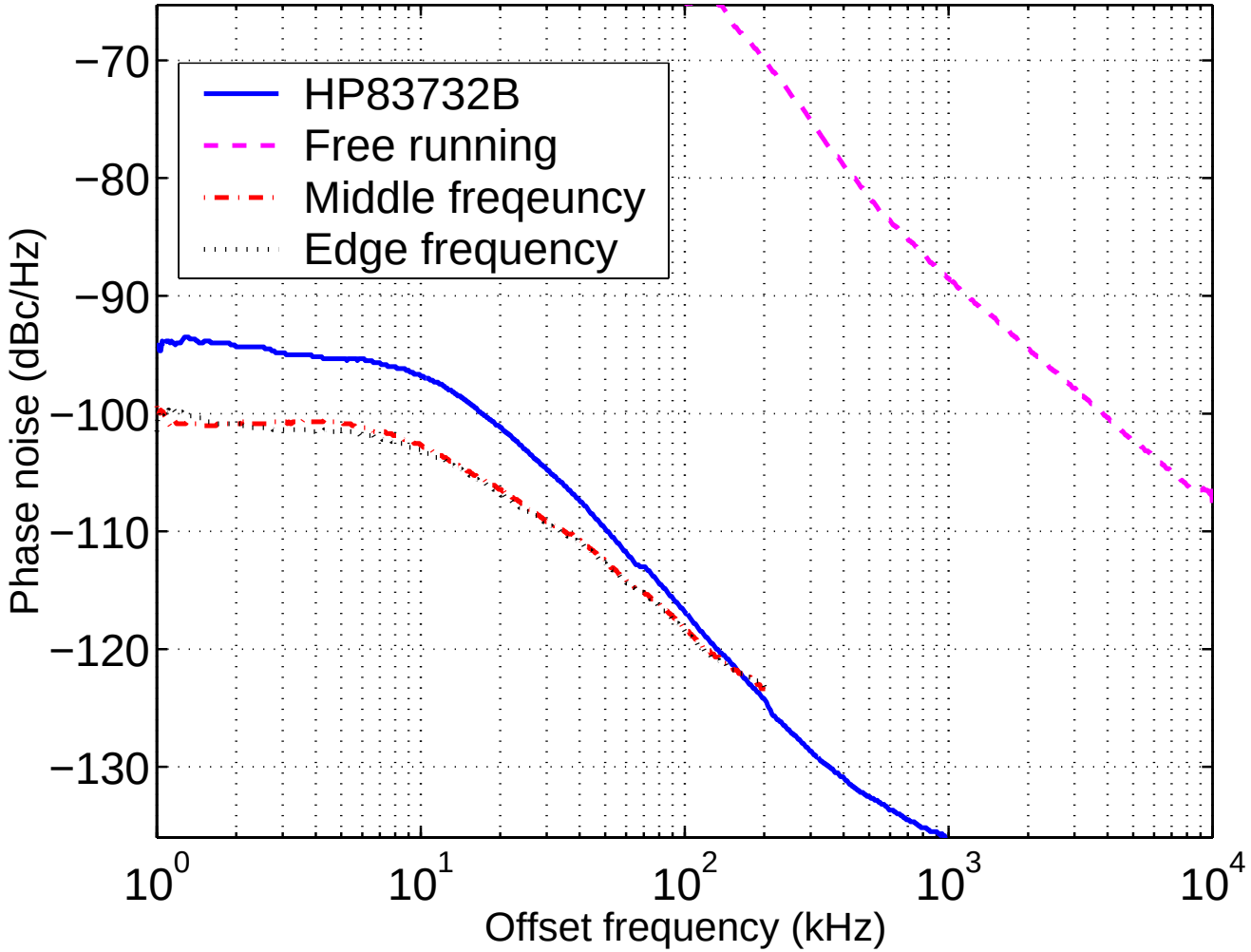


ILFD SUMMARY

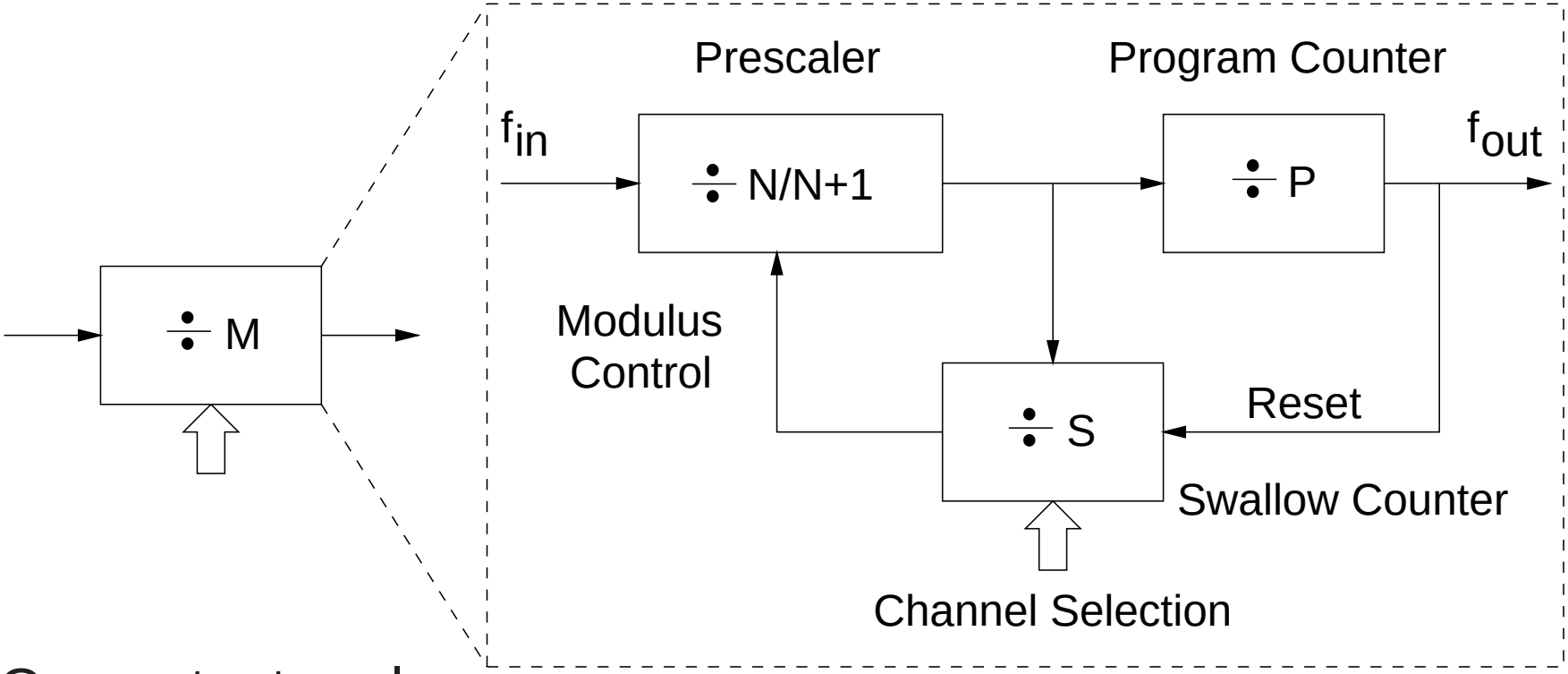
Frequency of operation	5 GHz
Output frequency tuning	110 MHz $\approx$ 5%
Input–referred locking range	600 MHz $\approx$ 12% @ 0.55 mW
	1000 MHz $\approx$ 20% @ 0.8 mW
Technology	0.24 μm CMOS
Die area	0.225 mm^2

Flipflop based divider (for comparison)

0.24 μm CMOS (simulation)	5 mW @ 5 GHz
0.1 μm CMOS [1]	2.6 mW @ 5 GHz

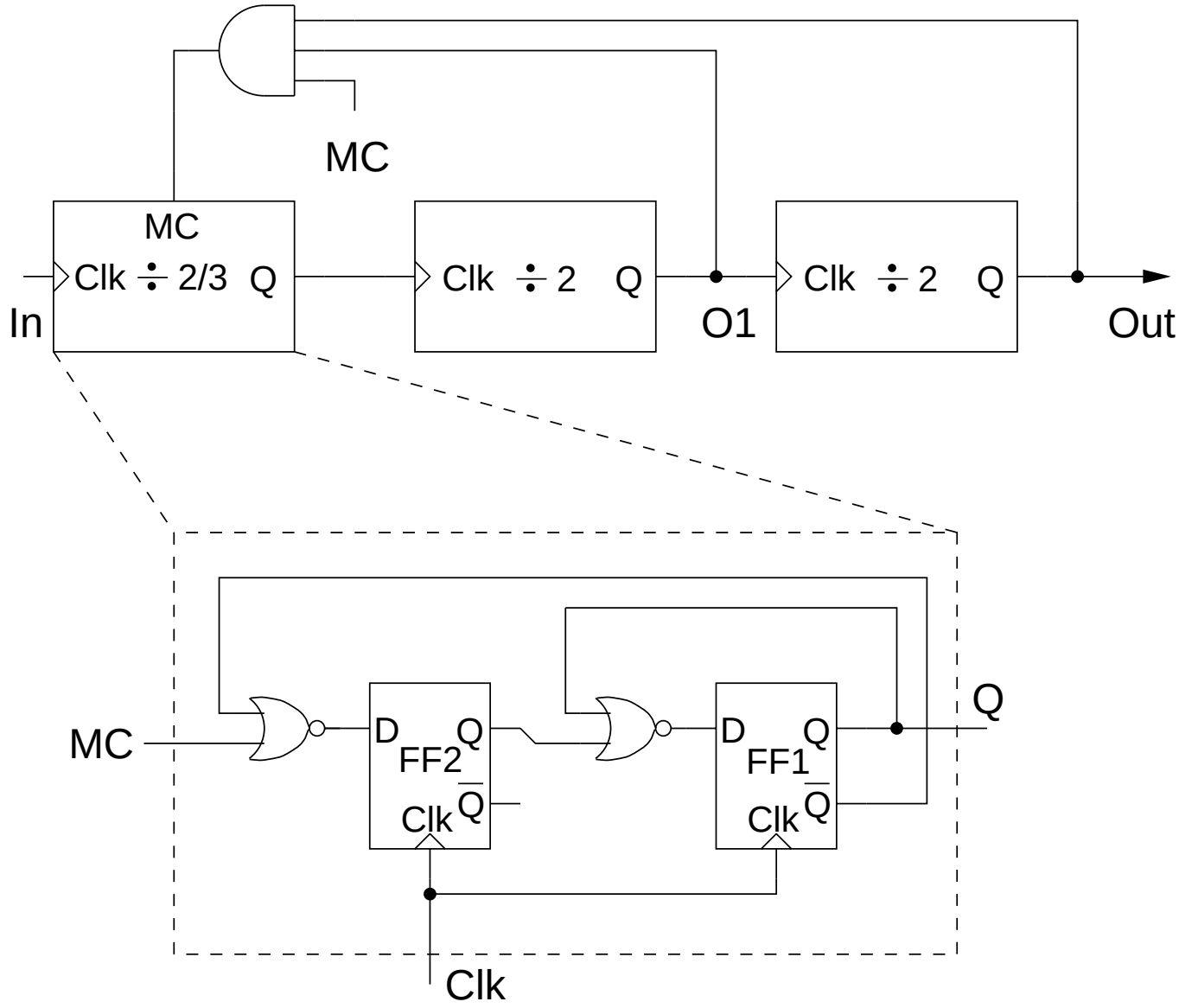
[1] Razavi *et al.*, JSSC Vol. 30, No.2, pp 101–109, Feb. 1995

PROGRAMMABLE FREQUENCY DIVIDER

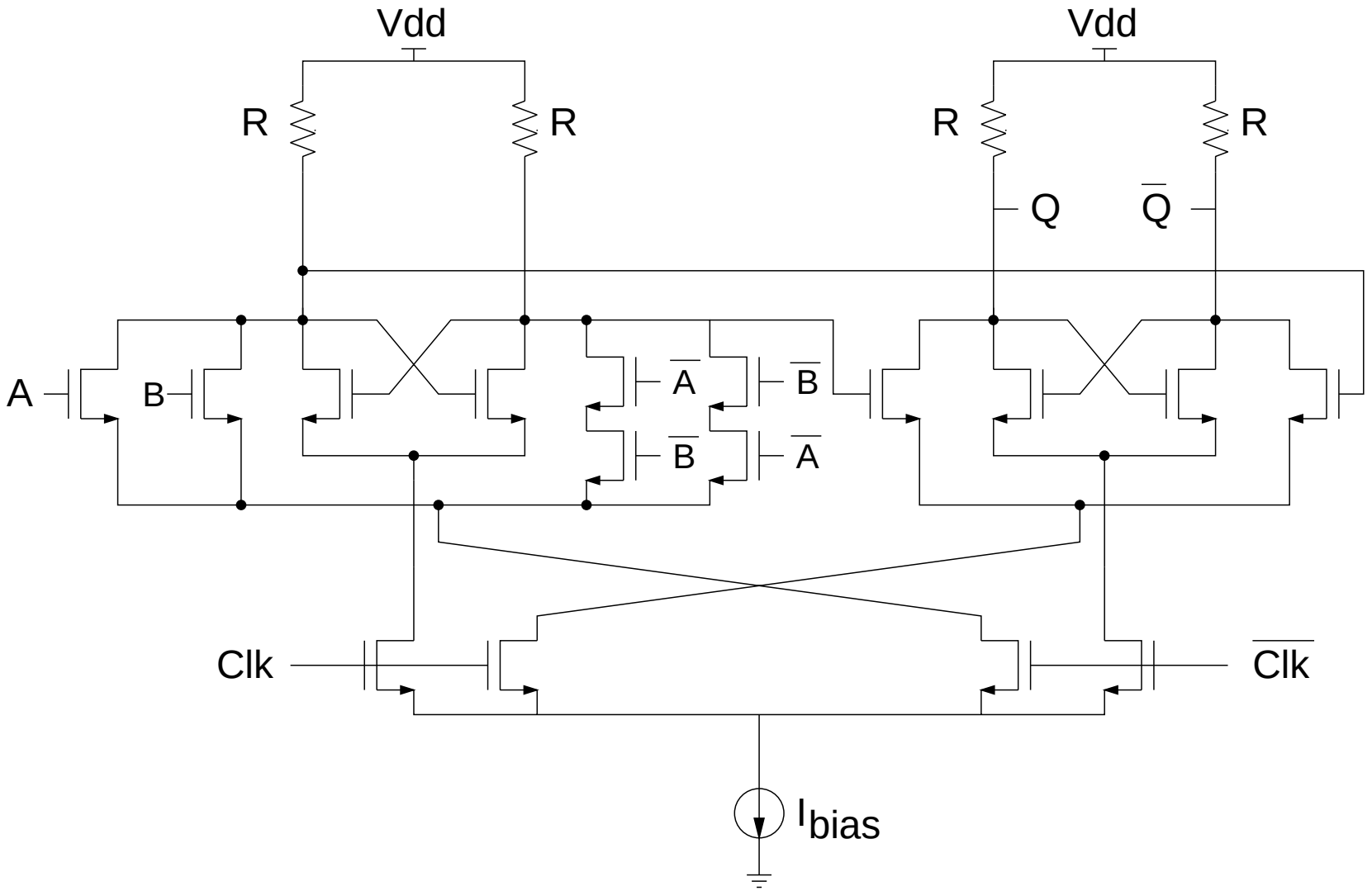


- One output cycle = $(N+1)S + (P-S)N = PN + S$ input cycles.
- $M = PN + S$
- $N = 8, P = 26, S = 12...19, M = 220...227$

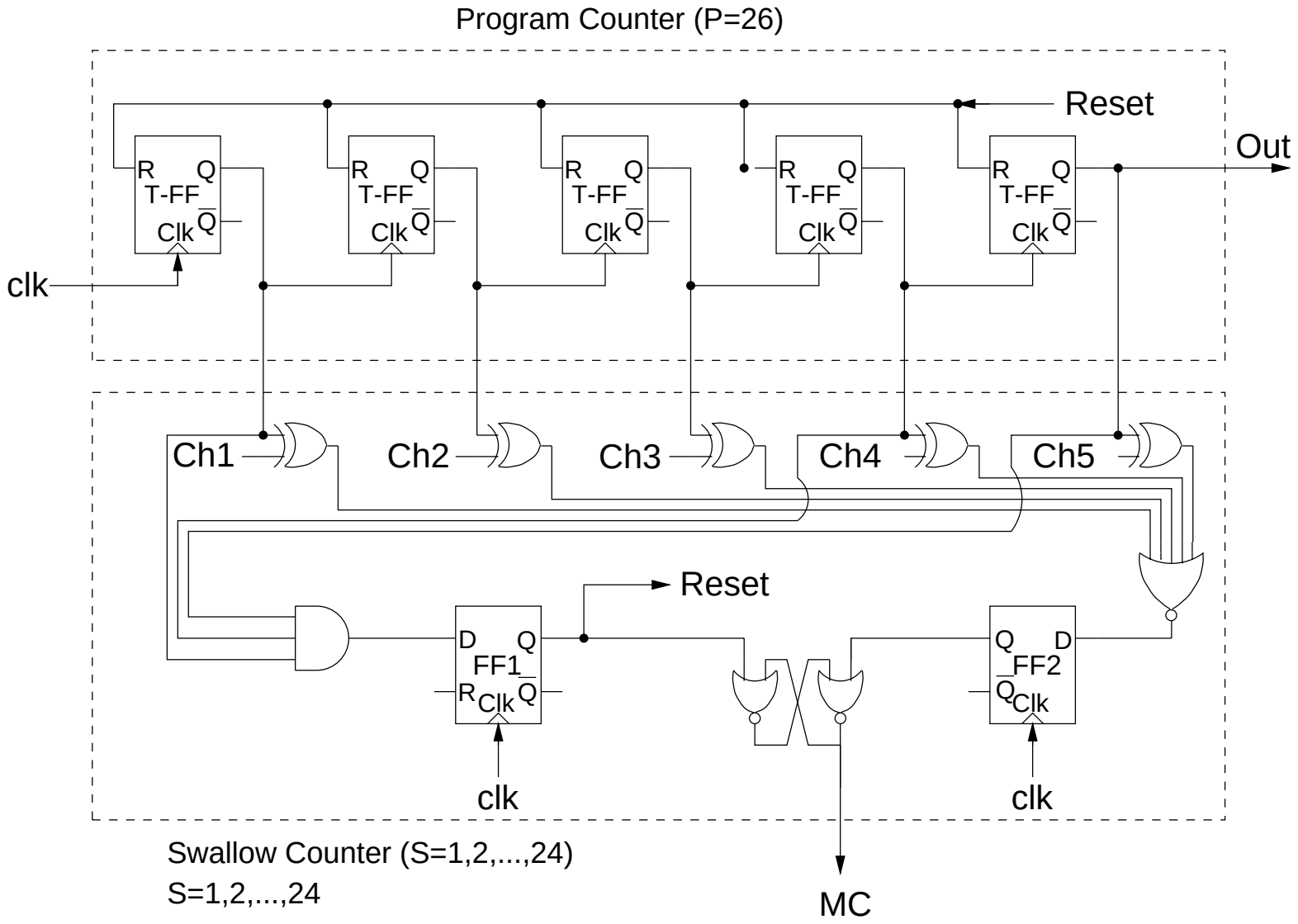
PRESCALER (÷ 8/9)



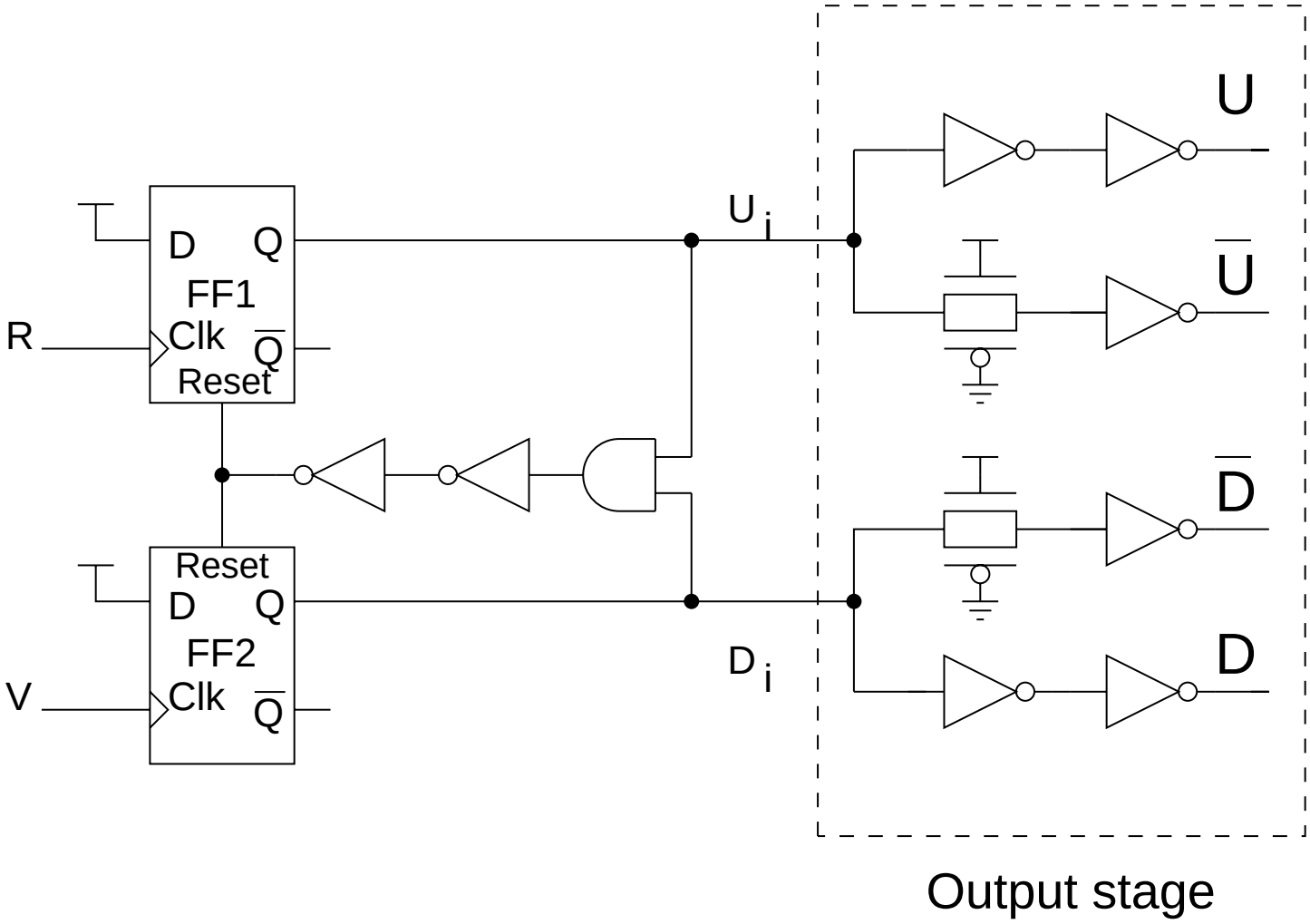
NOR/FLIPFLOP IMPLEMENTATION



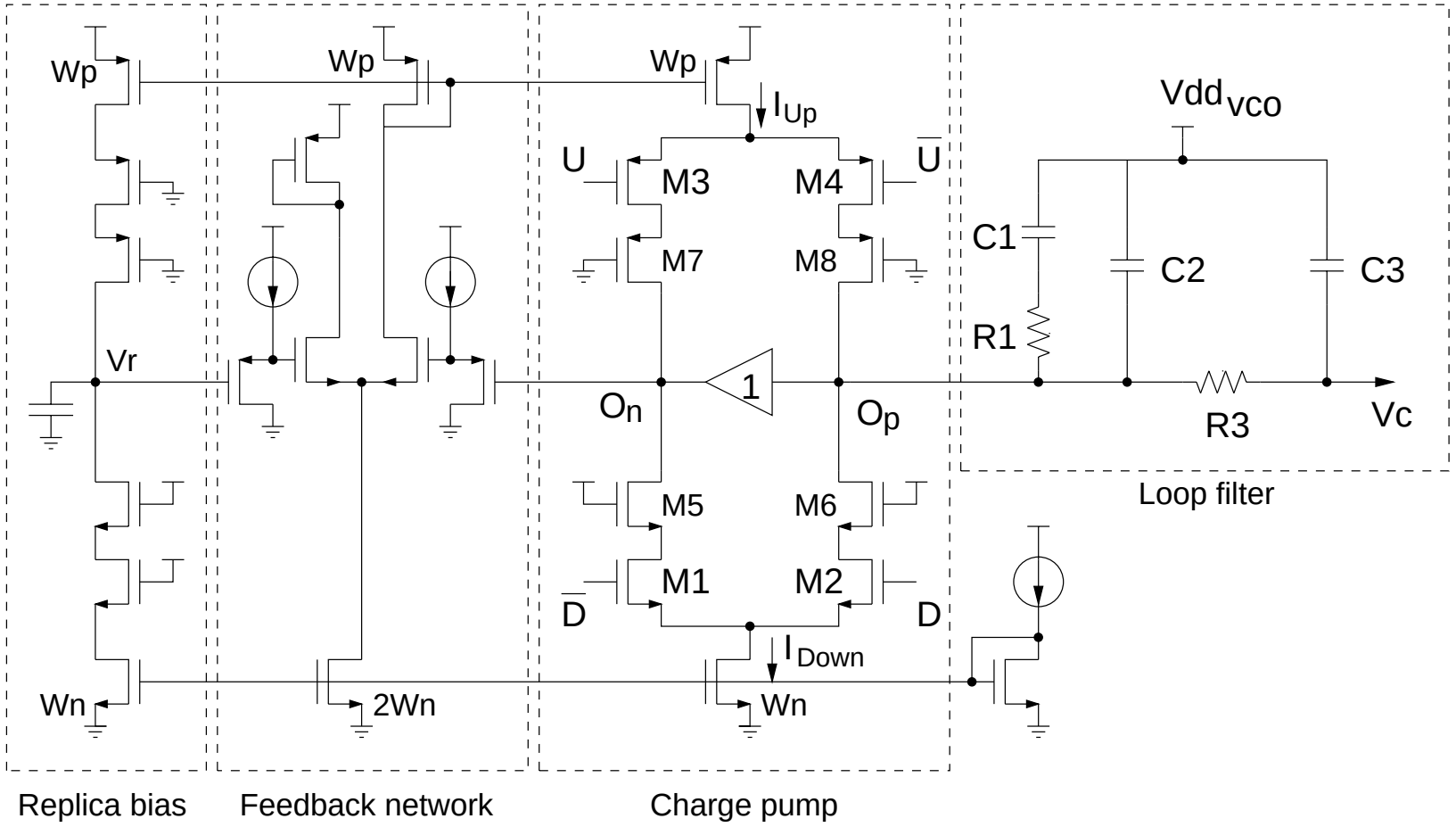
PROGRAM AND PULSE SWALLOW COUNTERS



PHASE/FREQUENCY DETECTOR

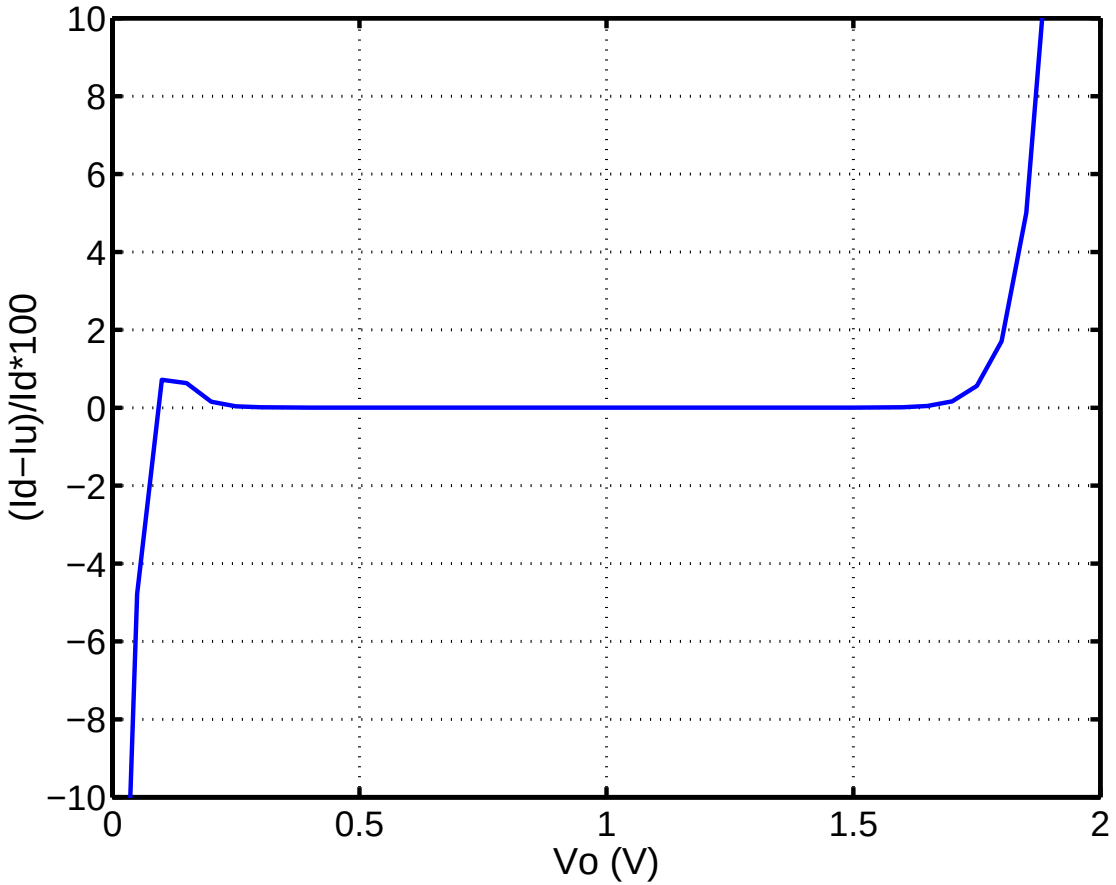


CHARGE PUMP AND LOOP–FILTER



CHARGE PUMP CURRENT MATCHING

- $\frac{\Delta I}{I}$ <0.05%
  0.25 V $\leq V_{\mathrm{O}} \leq$ 1.75 V
- $\frac{\Delta I}{I}$ <2%
  0.1 V $\leq V_{\mathrm{O}} \leq$ 1.8 V

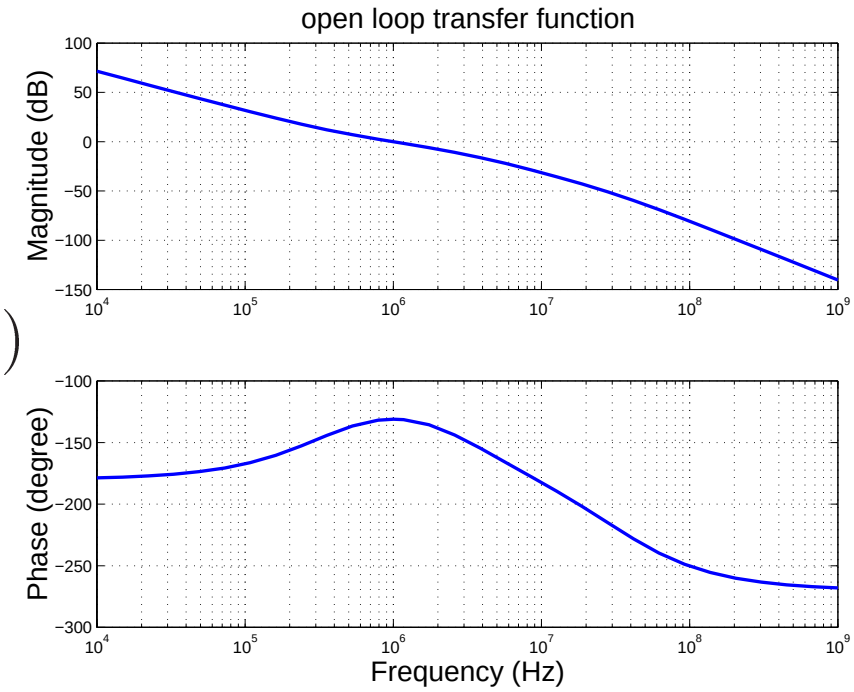


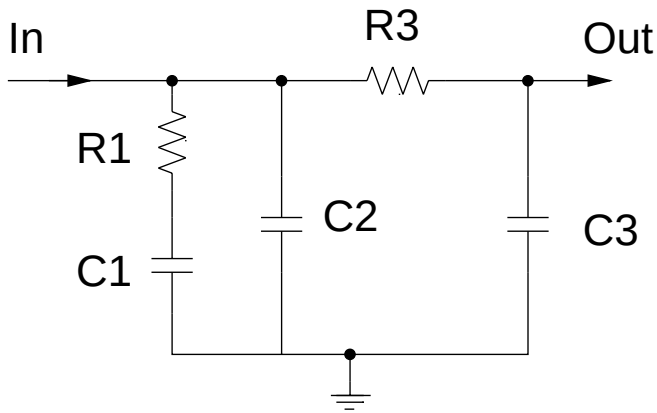
LOOP FILTER

	PLL order		
	2^{nd} order	3^{rd} order	4^{th} order
# Poles	2	3	4
Independent design variables:			
1) Phase margin	$\surd$	$\surd$	$\surd$
2) Loop bandwidth	$\surd$	$\surd$	$\surd$
3) Spur attenuation			$\surd$

Loop filter design (4^{th} order PLL)

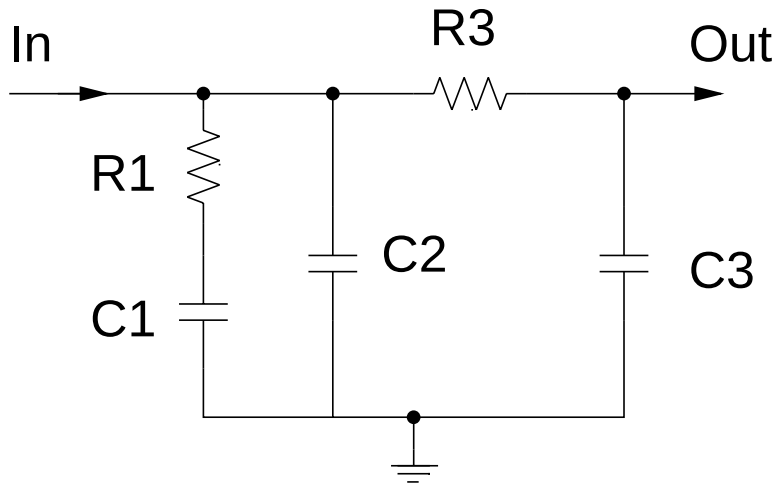
- $R_3C_3 \ll R_1(C_2 + C_3)$
- $b = \frac{C_1}{C_2+C_3}$
- PM $\approx \tan^{-1}(\sqrt{1+b}) - \tan^{-1}(\frac{1}{\sqrt{1+b}})$
- $W_c \approx \frac{\sqrt{1+b}}{R_1C_1}$
- $t_s = \frac{f_2(\text{PM})}{W_c}$
- R_3C_3 sets the spur attenuation.





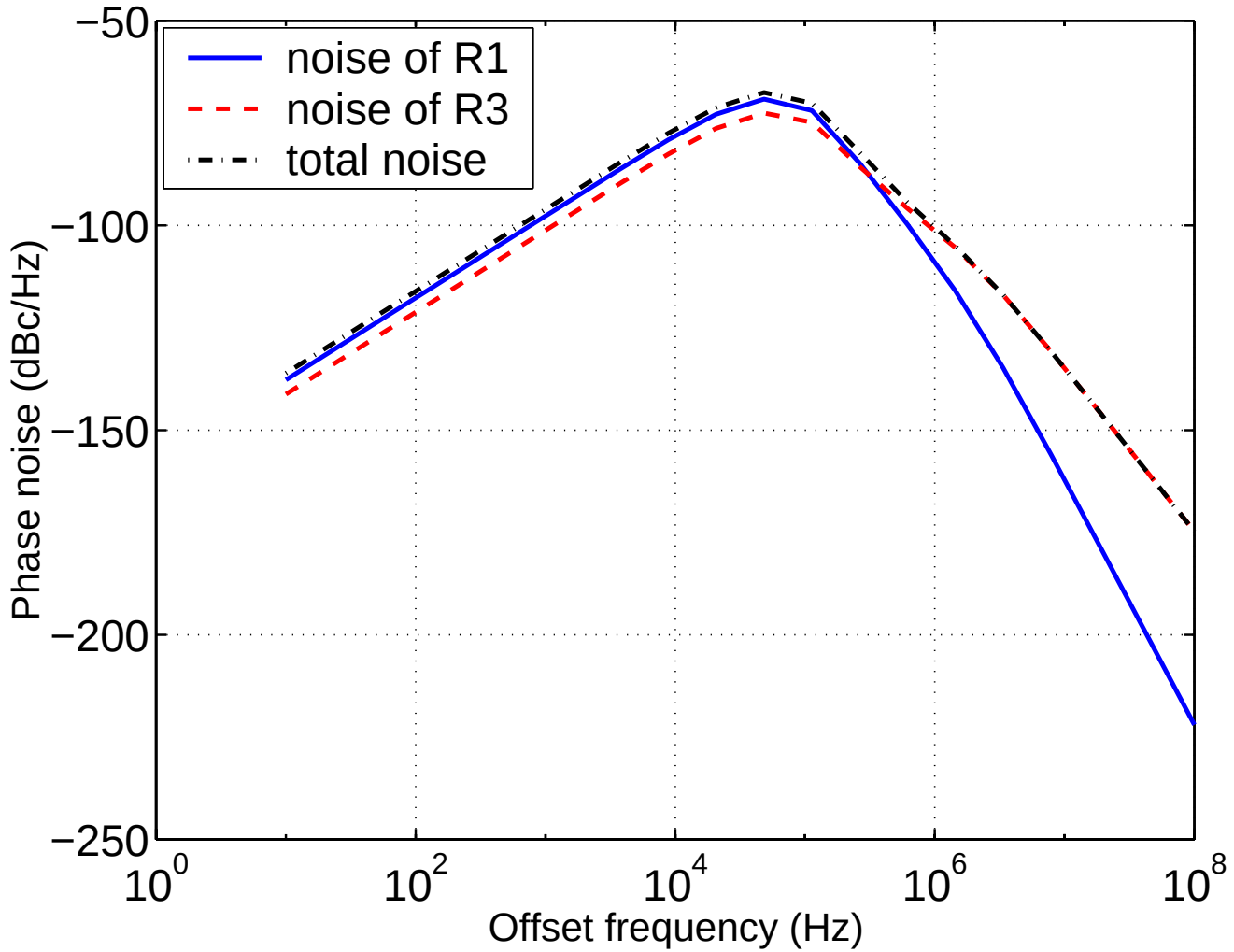
LOOP PARAMETERS

Parameter	Value
K_{vco}	360 MHz/V (Average) 500 MHz/V (Max)
I_p	3 μA
C_1	42 pF
C_2	3.5 pF
C_3	2.2 pF
R_1	170 kΩ
R_3	64.5 kΩ
PM	49°
W_c	60 kHz
$\lvert H(j2\pi f)\rvert$ @ f_{ref}	-45 dB
t_s	$<$ 35 μs



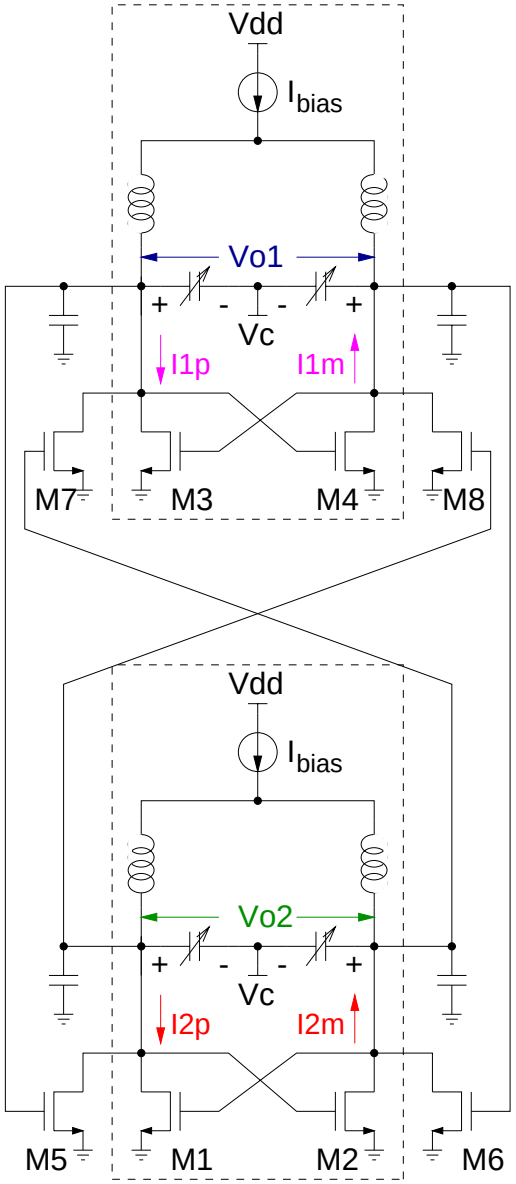
LOOP–FILTER NOISE

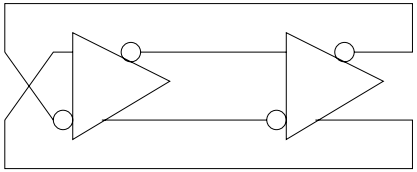
- L=-149 dBc/Hz @ 22 MHz

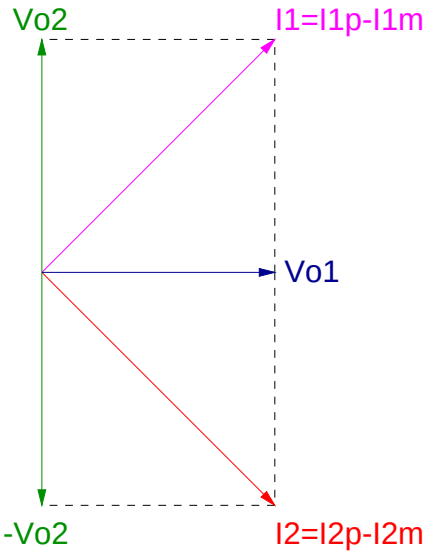


VOLTAGE–CONTROLLED OSCILLATOR

- 0.24 μm CMOS
- Vdd=1.5 V
- I_{bias}=4.0 mA
- f_o=4.9 GHz





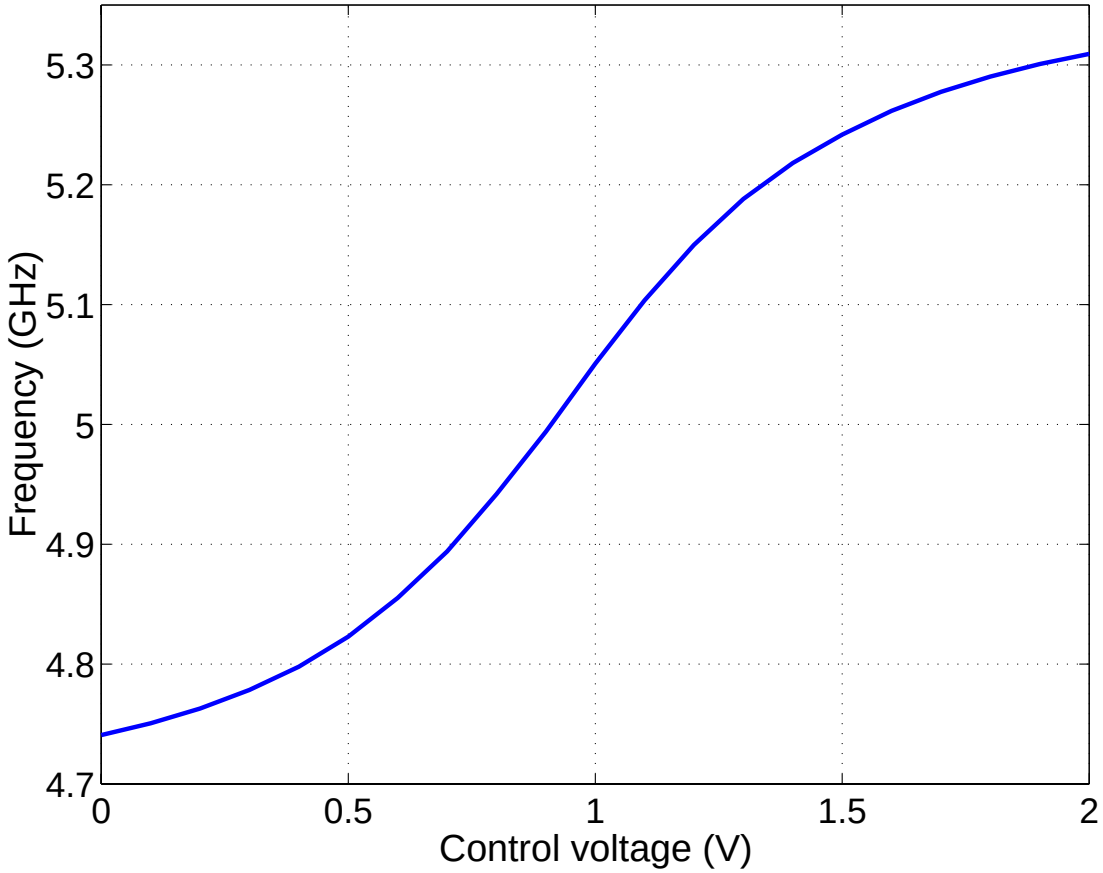


INDUCTOR DESIGN (VCO)

- Maximum $Q \Rightarrow$ minimum inductor noise
- If inductors are not the main source of noise, maximum $LQ \Rightarrow$
  - Maximum oscillation amplitude for a given bias current.
  - Minimum phase noise due to active devices.

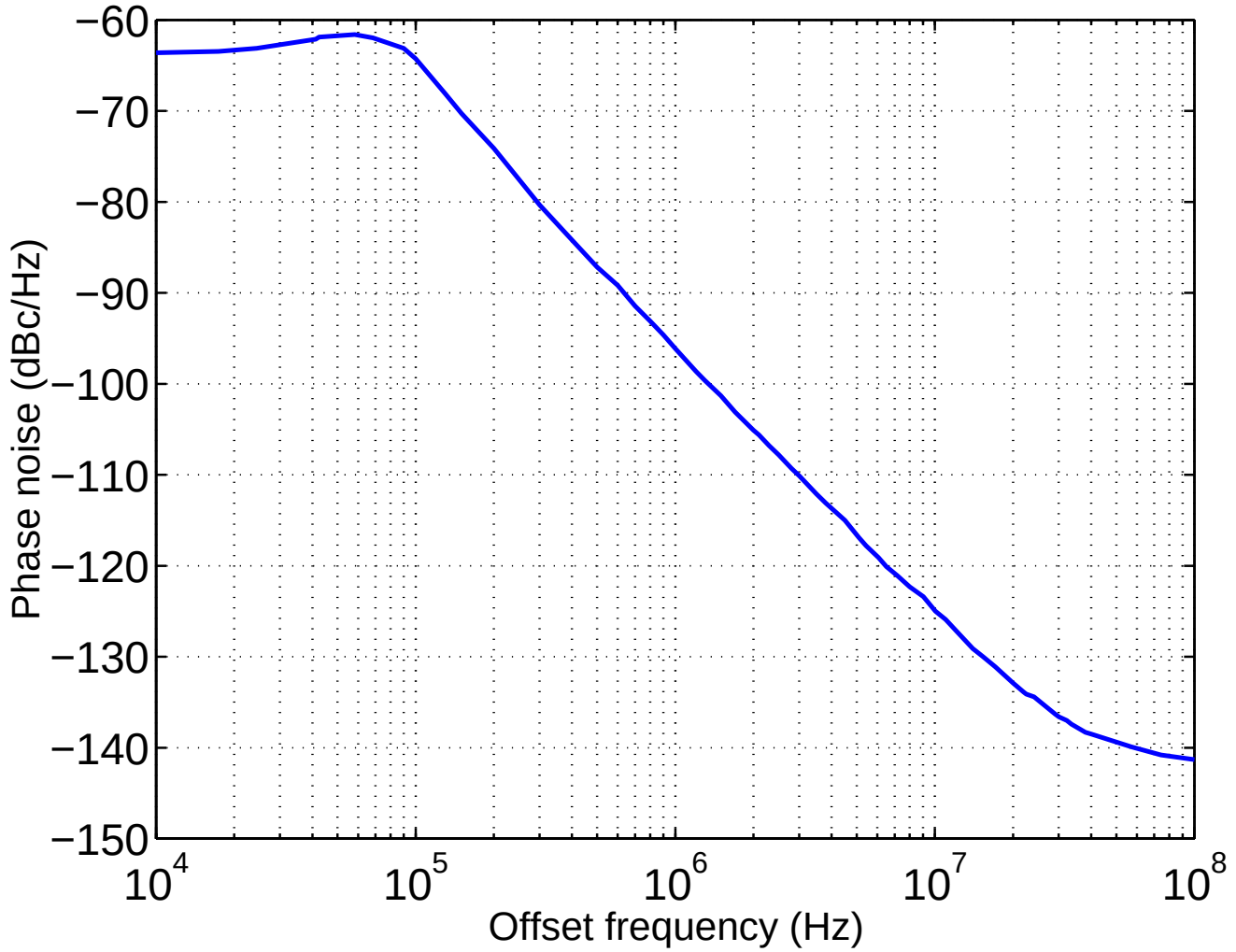
VCO FREQUENCY TUNING

- 0.24 μm CMOS
- Vdd=1.5 V
- $\mathrm{I}_{\mathrm{bias}}$=4.0 mA
- Δf =550 MHz (11%)
- $(\frac{df}{dv})_{\max}$=500 MHz/V

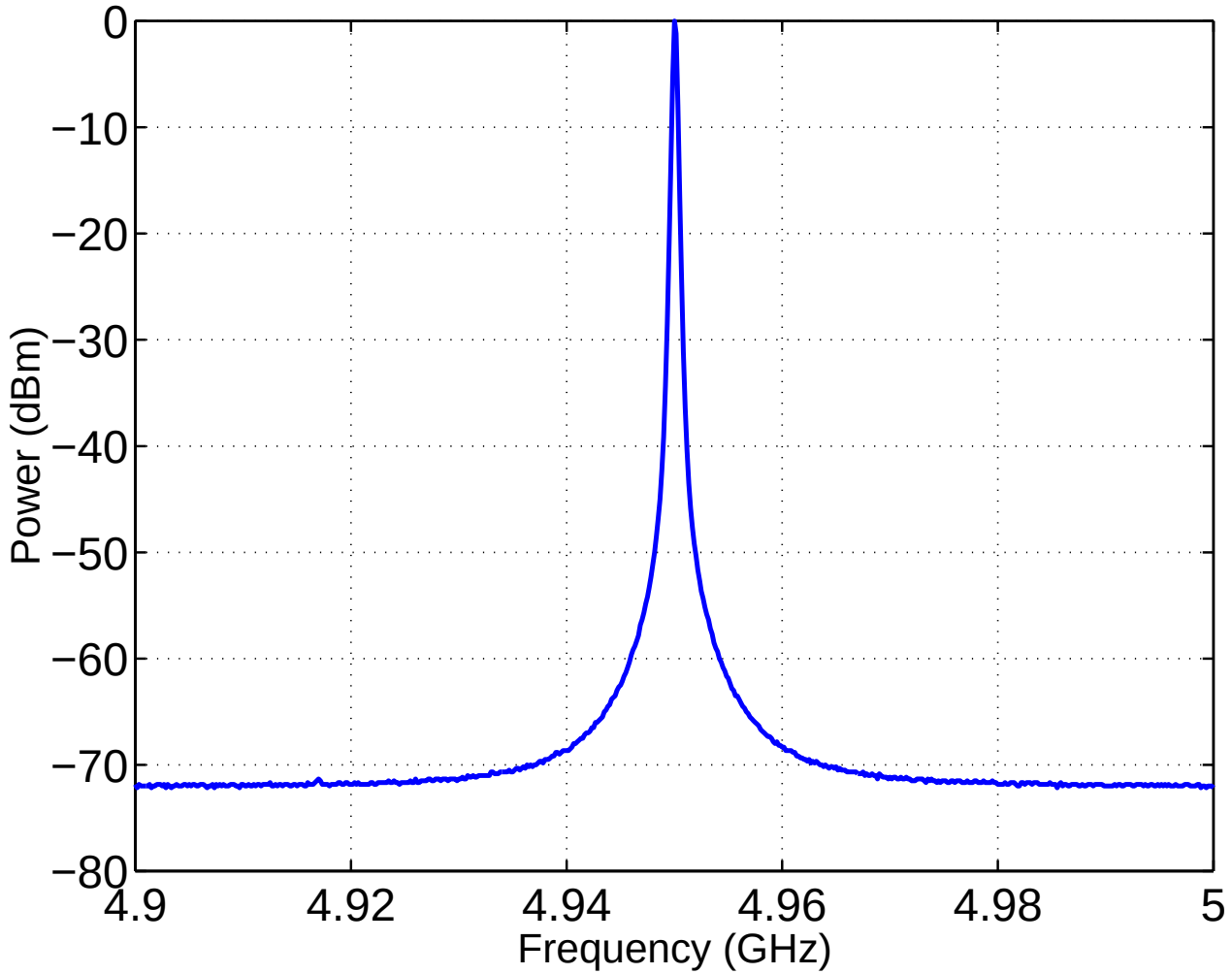


PLL PHASE NOISE

- L=-134 dBc/Hz @ 22 MHz

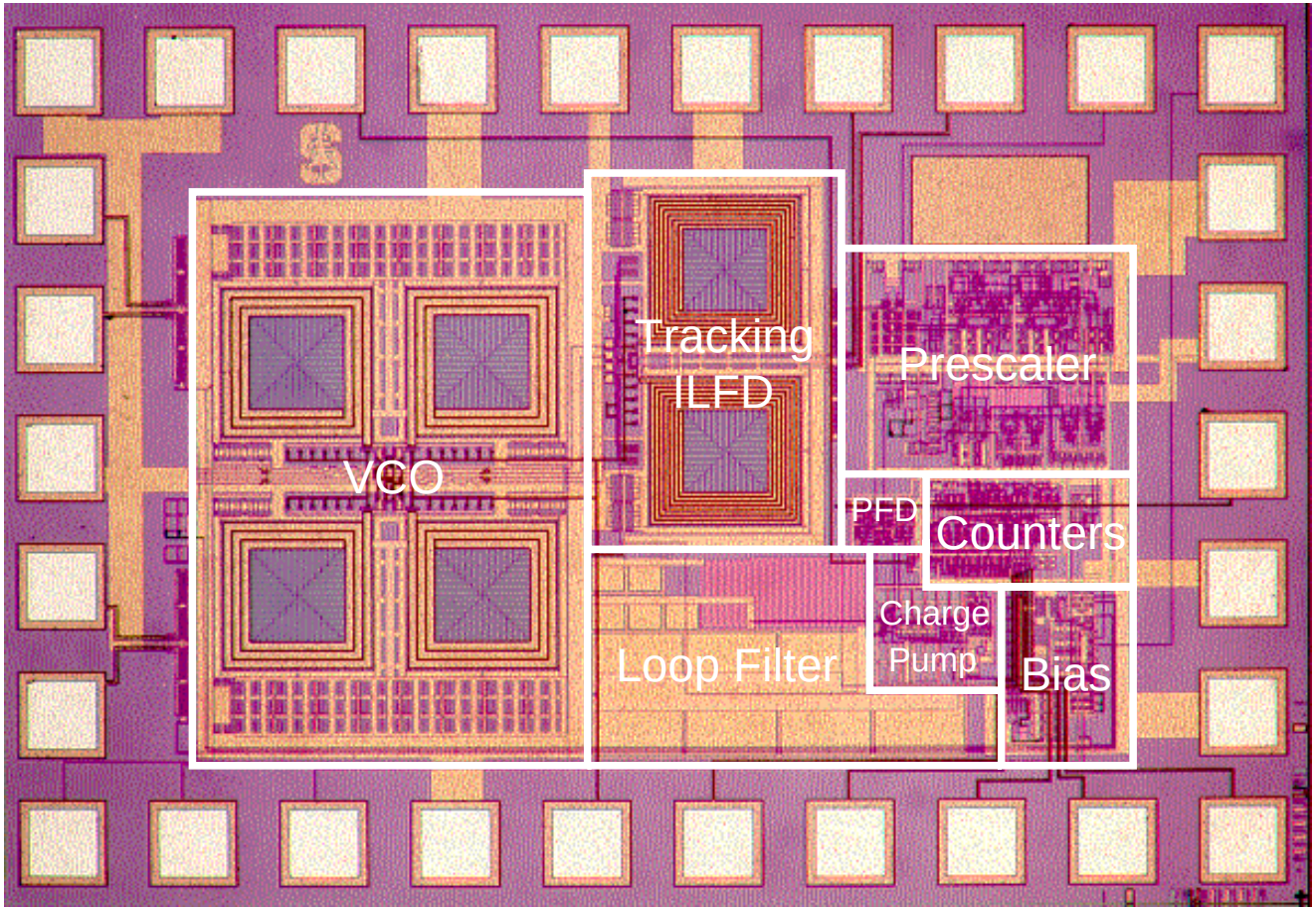


SPECTRUM OF THE SYNTHESIZED OUTPUT



SYNTHESIZER CHIP MICROGRAPH

- 0.24 μm CMOS
- area=1.45 mm^2 (1 $\times$ 1.45 mm^2)



SUMMARY

Synthesized frequencies	4.840–$4.994\ \mathrm{GHz}$
Reference frequency	$11\ \mathrm{MHz}$
Spurs	$< -70\ \mathrm{dBc}$
Phase noise	$-134\ \mathrm{dBc/Hz}$ @ $22\mathrm{MHz}$
Loop bandwidth	$60\ \mathrm{kHz}$
Settling time	$< 35\ \mu\mathrm{s}$
Power dissipation	
VCO	$12\ \mathrm{mW}$
ILFD	$1\ \mathrm{mW}$
Prescaler	$6.6\ \mathrm{mW}$
Digital+Bias Circuits	$2\ \mathrm{mW}$
Total	$21.6\ \mathrm{mW}$
Supply voltage	$1.5\ \mathrm{V}$ (analog)
	$2.0\ \mathrm{V}$ (digital)
Implementation	
Die area	$1.45\ \mathrm{mm}^2$
Technology	$0.24\ \mu\mathrm{m}$ CMOS

COMPARISON

Ref.	f (GHz)	P (mW)	L (μm)	FM	PN (dBc/Hz)	PN_n	Spur
[1]	1.6	90	0.6	10.7	-114 @ 600kHz	-135.4	-80 dBc
[2]	1.8	51	0.4	14.1	-134 @ 3MHz	-142.4	
[3]	1.6	36	0.5	22.2	-140 @ 35MHz	-126	-45 dBc
[4]	5.0	47	0.4	42.5	-100 @ 5.2MHz	-112.5	-50 dBc
This work	5.0	21.6	0.24	55.5	-134 @ 22MHz	-134	-70 dBc

- $\mathrm{FM} = \frac{f \times \mathrm{L}}{\mathrm{P}}$
- $\mathrm{PN_n} = \mathrm{PN} + 20 \log \left(\frac{\Delta f}{f} \frac{5\mathrm{GHz}}{22\mathrm{MHz}} \right)$

[1] J. Parker et al. “A 1.6GHz CMOS PLL with On–chip loop filter” JSSC Vol 33 Mar 98.

[2] J. Craninckx et al. “A Fully Integrated CMOS DCS–1800 Synthesizer” JSSC Vol 33 Dec 98.

[3] A. Shahani et al. “Low Power Dividerless Frequency Synthesis ...” JSSC Vol 33, Dec 98.

[4] C. Lam et al. “A 2.6GHz/5.2GHz Frequency Synthesizer in a 0.4μm CMOS Technology”, VLSI 99.

CONCLUSION

- A 5GHz frequency synthesizer is fully integrated in 0.24μm CMOS.
- Power consumption is reduced significantly by:
  - employing a tracking ILFD.
  - optimizing spiral inductors for the VCO and ILFD.
  - current sharing in the prescaler.
- Loop–filter noise is kept small by using reasonably small resistors.
- A spurious free output is achieved by:
  - using a semi–differential charge pump with well matched currents.
  - minimizing the skew of the PFD complementary outputs.
  - designing a fourth–order loop.

CONTRIBUTIONS

- Developing a general theory for injection–locked oscillators.
- Developing design techniques for very low power ILFD's with a wide locking range.
- Introducing the tracking ILFD.
- Designing a very low power and fully integrated CMOS frequency synthesizer at 5 GHz.
- Developing a very simple loop filter design recipe for third and fourth order PLL's.
- Demonstrating the operation of analog CMOS circuits with a sub 2 V supply.

ACKNOWLEDGMENTS

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Conexant