A CMOS Frequency Synthesizer with an Injection-Locked Frequency Divider for a 5 GHz Wireless LAN Receiver

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OUTLINE

- Motivation
- Introduction to wireless LAN
- Synthesizer architecture
- Synthesizer building blocks
- Summary and conclusion
Motivation

- Large demand for wideband wireless LAN systems
  - 20+ Mb/s data rate
  - Low cost
  - Low power
- New released frequency band
  - Unlicensed national information infrastructure (U–NII) band
GOAL

- Design a 5 GHz frequency synthesizer for a U–NII band wireless–LAN receiver (HIPERLAN compatible).
- Implement in CMOS.
- Minimize power consumption.
FREQUENCY OF OPERATION

HIPERLAN

U-NII

23.5 MHz
## HIPERLAN/1 STANDARD

<table>
<thead>
<tr>
<th></th>
<th>Class A</th>
<th>Class B</th>
<th>Class C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitter power</td>
<td>+10 dBm</td>
<td>+20 dBm</td>
<td>+30 dBm</td>
</tr>
<tr>
<td>Receiver sensitivity</td>
<td>-50 dBm</td>
<td>-60 dBm</td>
<td>-70 dBm</td>
</tr>
<tr>
<td>Maximum signal level</td>
<td></td>
<td>-25 dBm</td>
<td></td>
</tr>
<tr>
<td>Modulation</td>
<td></td>
<td>GMSK (BT=0.3)</td>
<td></td>
</tr>
<tr>
<td>Data rate</td>
<td></td>
<td>20 Mb/s</td>
<td></td>
</tr>
<tr>
<td>Topology</td>
<td></td>
<td>multihop <em>ad hoc</em></td>
<td></td>
</tr>
<tr>
<td>Carrier switching time</td>
<td></td>
<td>≤ 1 ms</td>
<td></td>
</tr>
<tr>
<td>Channel bandwidth</td>
<td></td>
<td>23.5 MHz</td>
<td></td>
</tr>
</tbody>
</table>
HIPERLAN MULTIHOP *ad hoc topology*
● Weaver architecture.

● Requires quadrature LO’s to reject the image signal.
**Typical PLL–Based Frequency Synthesizer**

- Reference is a crystal oscillator.
- \( f_{out} = M \times f_{ref} \)
- Multiple LO frequencies are generated by changing M.
- Frequency dividers are power hungry.
  - Their power consumption increases with frequency.
PROPOSED PLL ARCHITECTURE

- \( f_{ref} = 11 \text{ MHz} \)
- \( f_o = 4.840–4.994 \text{ GHz} \)
- 8 channels
- \( M = 220–227 \)
- \( N = 8 \)
By impressing an oscillator with an external (incident) signal, frequency locking can be achieved.

- First-harmonic injection locked oscillators \( \left( \frac{f_i}{f_o} = 1 \right) \).

- Subharmonic injection locked oscillators \( \left( \frac{f_i}{f_o} = \frac{1}{N} \right) \).

- Superharmonic injection locked oscillators \( \left( \frac{f_i}{f_o} = N \right) \).

Injection–locked frequency dividers (ILFDs).
- Intermodulation of the input and output is the base of frequency division in an ILFD.

- An ILFD is an oscillator with perturbed oscillation.
  - Oscillation conditions should be satisfied in the presence of the incident signal.
SPECIAL CASE (DIVIDE–BY–TWO)

\[ f(e) = a_0 + a_1 e + a_2 e^2 + a_3 e^3 \]

- **Condition 1:**
  \[ \frac{\Delta \omega}{\omega_r} < \left| \frac{H_0 a_2 V_i}{2Q} \right|, \quad \frac{H_0}{Q} = \frac{LQ \omega_r}{Q} = L \omega_r \]

- **Condition 2:**
  \[ H_0 \left( a_1 + \frac{3}{2} a_3 V_i^2 + a_2 V_i \cos(\phi) \right) < 1 \]
TRACKING ILFD

- Locking range extension
Differential tracking ILFD

- 0.24 μm CMOS
- Vdd=1.5 V
- I_{bias}=300 μA
- f_o=2.45 GHz
- f_i=4.9 GHz
INDUCTOR DESIGN (ILFD)

- Maximum locking range $\Rightarrow$ maximize $L$
- Minimum power consumption $\Rightarrow$ maximize $LQ$
INDUCTOR DESIGN

- Design parameters:
  - w: metal width
  - s: metal spacing
  - OD: outer dimension
  - n: number of turns
In planar spiral inductors maximizing $L$ does not maximize $LQ$.

Maximize $L$ for a given $LQ$. 

INDUCTOR DESIGN (ILFD)
ILFD FREE—RUNNING OSCILLATION

- $0.24 \, \mu m$ CMOS
- $V_{dd}=1.5 \, V$
- $I_{bias}=300 \, \mu A$
- $\Delta f=110 \, MHz \ (5\%)$
- $\Delta V_c=2 \, V$
ILFD LOCKING RANGE/POWER CONSUMPTION

- 0.24 μm CMOS
- Vdd=1.5 V
- $f_o=2.45$ GHz
- $f_i=4.9$ GHz
- $\Delta f=1$ GHz
  @ 1 V ($\approx 20\%$)
- Power=0.75 mW
  @ 1 V
PHASE NOISE MEASUREMENT TEST SETUP

![Test Setup Diagram]

- **Input Signal** $V_i$
- **DILFD**
- **Ext. Amp.**
- **HP8563E**
- **Vdd**
- **50 Ohm Resistors**
- **On chip**

Diagram showing the connection of the test setup with the HP8563E instrument.
ILFD PHASE NOISE

- 0.24 μm CMOS
- Vdd=1.5 V
- $f_o=2.45$ GHz
- $f_i=4.9$ GHz
## ILFD SUMMARY

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency of operation</td>
<td>5 GHz</td>
</tr>
<tr>
<td>Output frequency tuning</td>
<td>110 MHz $\approx$ 5%</td>
</tr>
<tr>
<td>Input–referred locking range</td>
<td>600 MHz $\approx$ 12% @ 0.55 mW</td>
</tr>
<tr>
<td>Input–referred locking range</td>
<td>1000 MHz $\approx$ 20% @ 0.8 mW</td>
</tr>
<tr>
<td>Technology</td>
<td>0.24 $\mu$m CMOS</td>
</tr>
<tr>
<td>Die area</td>
<td>0.225 mm$^2$</td>
</tr>
</tbody>
</table>

*Flipflop based divider (for comparison)*

<table>
<thead>
<tr>
<th>Technology</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.24 $\mu$m CMOS (simulation)</td>
<td>5 mW @ 5 GHz</td>
</tr>
<tr>
<td>0.1 $\mu$m CMOS [1]</td>
<td>2.6 mW @ 5 GHz</td>
</tr>
</tbody>
</table>

One output cycle = \((N + 1)S + (P - S)N\) = \(PN + S\) input cycles.

- \(M = PN + S\)
- \(N = 8, P = 26, S = 12...19, M = 220...227\)
PRESCALER ($\div 8/9$)
NOR/FLIPFLOP IMPLEMENTATION
PROGRAM AND PULSE SWALLOW COUNTERS

Program Counter (P=26)

Swallow Counter (S=1,2,...,24)
S=1,2,...,24

MC
PHASE/FREQUENCY DETECTOR
CHARGE PUMP AND LOOP–FILTER

Replica bias  Feedback network  Charge pump
• \( \frac{\Delta I}{I} < 0.05\% \)
  \[ 0.25 \, \text{V} \leq V_O \leq 1.75 \, \text{V} \]

• \( \frac{\Delta I}{I} < 2\% \)
  \[ 0.1 \, \text{V} \leq V_O \leq 1.8 \, \text{V} \]
# Loop Filter

<table>
<thead>
<tr>
<th># Poles</th>
<th>2&lt;sup&gt;nd&lt;/sup&gt; order</th>
<th>3&lt;sup&gt;rd&lt;/sup&gt; order</th>
<th>4&lt;sup&gt;th&lt;/sup&gt; order</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 poles</td>
<td>2</td>
<td>3</td>
<td>4</td>
</tr>
</tbody>
</table>

Independent design variables:

<table>
<thead>
<tr>
<th></th>
<th>2&lt;sup&gt;nd&lt;/sup&gt; order</th>
<th>3&lt;sup&gt;rd&lt;/sup&gt; order</th>
<th>4&lt;sup&gt;th&lt;/sup&gt; order</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) Phase margin</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>2) Loop bandwidth</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>3) Spur attenuation</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>
**Loop Filter Design ($4^{th}$ Order PLL)**

- $R_3C_3 \ll R_1(C_2 + C_3)$
- $b = \frac{C_1}{C_2 + C_3}$
- $PM \approx \tan^{-1}\left(\sqrt{1+b}\right) - \tan^{-1}\left(\frac{1}{\sqrt{1+b}}\right)$
- $W_c \approx \frac{\sqrt{1+b}}{R_1C_1}$
- $t_s = \frac{f_2(\text{PM})}{W_c}$
- $R_3C_3$ sets the spur attenuation.
## Loop Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_{vco}$</td>
<td>360 MHz/V (Average) 500 MHz/V (Max)</td>
</tr>
<tr>
<td>$I_p$</td>
<td>3 μA</td>
</tr>
<tr>
<td>$C_1$</td>
<td>42 pF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>3.5 pF</td>
</tr>
<tr>
<td>$C_3$</td>
<td>2.2 pF</td>
</tr>
<tr>
<td>$R_1$</td>
<td>170 kΩ</td>
</tr>
<tr>
<td>$R_3$</td>
<td>64.5 kΩ</td>
</tr>
<tr>
<td>PM</td>
<td>49°</td>
</tr>
<tr>
<td>$W_c$</td>
<td>60 kHz</td>
</tr>
<tr>
<td>$</td>
<td>H(j2\pi f)</td>
</tr>
<tr>
<td>$t_s$</td>
<td>&lt; 35 μs</td>
</tr>
</tbody>
</table>

![Circuit Diagram]
• $L = -149$ dBc/Hz at 22 MHz
VOLTAGE–CONTROLLED OSCILLATOR

- 0.24 μm CMOS
- Vdd=1.5 V
- $I_{bias}=4.0$ mA
- $f_0=4.9$ GHz
**INDUCTOR DESIGN (VCO)**

- Maximum $Q \Rightarrow$ minimum inductor noise
- If inductors are not the main source of noise, maximum $LQ \Rightarrow$
  - Maximum oscillation amplitude for a given bias current.
  - Minimum phase noise due to active devices.
VCO FREQUENCY TUNING

- 0.24 $\mu$m CMOS
- $V_{dd}=1.5$ V
- $I_{bias}=4.0$ mA
- $\Delta f = 550$ MHz (11%)
- $\left(\frac{df}{dv}\right)_{max}=500$ MHz/V
PLL PHASE NOISE

- L=-134 dBc/Hz @ 22 MHz
SPECTRUM OF THE SYNTHESIZED OUTPUT
SYNTHESIZER CHIP MICROGRAPH

- 0.24 $\mu$m CMOS
- area=1.45 mm$^2$ (1 $\times$ 1.45 mm$^2$)
### SUMMARY

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synthesized frequencies</td>
<td>4.840–4.994 GHz</td>
</tr>
<tr>
<td>Reference frequency</td>
<td>11 MHz</td>
</tr>
<tr>
<td>Spurs</td>
<td>&lt; –70 dBc</td>
</tr>
<tr>
<td>Phase noise</td>
<td>–134 dBc/Hz @ 22MHz</td>
</tr>
<tr>
<td>Loop bandwidth</td>
<td>60 kHz</td>
</tr>
<tr>
<td>Settling time</td>
<td>&lt; 35 μs</td>
</tr>
</tbody>
</table>

#### Power dissipation

<table>
<thead>
<tr>
<th>Component</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO</td>
<td>12</td>
</tr>
<tr>
<td>ILFD</td>
<td>1</td>
</tr>
<tr>
<td>Prescaler</td>
<td>6.6</td>
</tr>
<tr>
<td>Digital+Bias Circuits</td>
<td>2</td>
</tr>
<tr>
<td>Total</td>
<td>21.6</td>
</tr>
<tr>
<td>Supply voltage (analog)</td>
<td>1.5 V</td>
</tr>
<tr>
<td>Supply voltage (digital)</td>
<td>2.0 V</td>
</tr>
</tbody>
</table>

#### Implementation

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die area</td>
<td>1.45 mm²</td>
</tr>
<tr>
<td>Technology</td>
<td>0.24 μm CMOS</td>
</tr>
</tbody>
</table>
## Comparison

<table>
<thead>
<tr>
<th>Ref.</th>
<th>$f$ (GHz)</th>
<th>$P$ (mW)</th>
<th>$L$ ($\mu$m)</th>
<th>FM</th>
<th>PN (dBc/Hz)</th>
<th>$PN_n$</th>
<th>Spur</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>1.6</td>
<td>90</td>
<td>0.6</td>
<td>10.7</td>
<td>-114 @ 600kHz</td>
<td>-135.4</td>
<td>-80 dBC</td>
</tr>
<tr>
<td>[2]</td>
<td>1.8</td>
<td>51</td>
<td>0.4</td>
<td>14.1</td>
<td>-134 @ 3MHz</td>
<td>-142.4</td>
<td></td>
</tr>
<tr>
<td>[3]</td>
<td>1.6</td>
<td>36</td>
<td>0.5</td>
<td>22.2</td>
<td>-140 @ 35MHz</td>
<td>-126</td>
<td>-45 dBC</td>
</tr>
<tr>
<td>[4]</td>
<td>5.0</td>
<td>47</td>
<td>0.4</td>
<td>42.5</td>
<td>-100 @ 5.2MHz</td>
<td>-112.5</td>
<td>-50 dBC</td>
</tr>
<tr>
<td>This work</td>
<td>5.0</td>
<td>21.6</td>
<td>0.24</td>
<td>55.5</td>
<td>-134 @ 22MHz</td>
<td>-134</td>
<td>-70 dBC</td>
</tr>
</tbody>
</table>

- $FM = \frac{f \times L}{P}$
- $PN_n = PN + 20 \log \left( \frac{\Delta f}{f} \cdot \frac{5GHz}{22MHz} \right)$

[4] C. Lam et al. “A 2.6GHz/5.2GHz Frequency Synthesizer in a 0.4$\mu$m CMOS Technology”, VLSI 99.
CONCLUSION

- A 5GHz frequency synthesizer is fully integrated in 0.24\textmu m CMOS.

- Power consumption is reduced significantly by:
  - employing a tracking ILFD.
  - optimizing spiral inductors for the VCO and ILFD.
  - current sharing in the prescaler.

- Loop–filter noise is kept small by using reasonably small resistors.

- A spurious free output is achieved by:
  - using a semi–differential charge pump with well matched currents.
  - minimizing the skew of the PFD complementary outputs.
  - designing a fourth–order loop.
CONTRIBUTIONS

- Developing a general theory for injection–locked oscillators.
- Developing design techniques for very low power ILFD’s with a wide locking range.
- Introducing the tracking ILFD.
- Designing a very low power and fully integrated CMOS frequency synthesizer at 5 GHz.
- Developing a very simple loop filter design recipe for third and fourth order PLL’s.
- Demonstrating the operation of analog CMOS circuits with a sub 2 V supply.
ACKNOWLEDGMENTS

National Semiconductor
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Conexant