Fractal Capacitors

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***Abstract*—A linear capacitor structure using fractal geometries is described. This capacitor exploits both lateral and vertical electric fields to increase the capacitance per unit area. Compared to standard parallel-plate capacitors, the parasitic bottom-plate capacitance is reduced. Unlike conventional metal-to-metal capacitors, the capacitance density increases with technology scaling. A classic fractal structure is implemented with 0.6-μm metal spacing, and a factor of 2.3 increase in the capacitance per unit area is observed. It is shown that capacitance boost factors in excess of ten may be possible as technology continues to scale. A computer-aided-design tool to automatically generate and analyze custom fractal layouts has been developed.**

I. Introduction

CAPACITORS are one of the crucial elements in integrated circuits and are used extensively in many IC applications such as data converters, sample and holds, switched-capacitor circuits, radio-frequency (RF) oscillators, and mixers. Capacitors can occupy considerable area; therefore, an area-efficient capacitor is highly desirable. The problem is more pronounced in modern process technologies where the vertical spacing of the metal layers does not scale much, if at all.

Four types of capacitors have been commonly used in IC design: gate capacitors, junction capacitors, conventional metal-to-metal/poly capacitors, and thin-insulator capacitors. Gate capacitors have high density (high capacitance per unit area) but are nonlinear and require a dc bias voltage to operate. Due to the thin gate oxide, gate capacitors have a low breakdown voltage. They also have a medium quality factor Q. Junction capacitors suffer from some of the above problems as well. They are highly nonlinear, and they also need a dc bias voltage. In addition, their sensitivity to process variations, poor quality factor, and large temperature coefficient limit their use in many applications. Metal-to-metal and metal-to-poly capacitors, on the other hand, are linear and have high Q. They also exhibit very small temperature variations. Unfortunately, the density of a traditional metal-to-metal capacitor is very low due to the relatively thick interlevel oxide layers. The problem becomes more severe with scaled technologies since the vertical spacing of the metal layers stays relatively constant. As a result, standard parallel-plate capacitors consume a larger percentage of the die area as technology scales. There has been a recent growth in the use of thin-insulator capacitors in IC applications. Double-poly capacitors and metal-insulator-metal (MIM) capacitors use a thin oxide to achieve high density [1]. The capacitance density is much higher than the density of a standard metal-to-metal capacitor, but it is lower than the density of a gate capacitor built in the same technology. The need for additional masks and process steps makes these capacitors more expensive compared to other types of capacitors. Double-poly capacitors and MIM capacitors are highly linear and have high quality factors, but due to the cost overhead, they are generally not available in standard digital processes.

This paper introduces a high-density capacitor structure using fractal geometries that can be built in standard digital processes. The linearity of this structure is similar to the conventional parallel-plate metal-to-metal capacitor. The bottom-plate parasitic capacitance of the proposed structure is small, which makes it appealing for many circuit applications such as switched-capacitor systems. Unlike conventional metal-to-metal capacitors, the density of a fractal capacitor increases with scaling.

Section II compares lateral and vertical flux capacitors and investigates the effect of scaling. Section III reviews the concept of fractals. The application of fractal geometries to capacitor structures is presented in Section IV, and some of the advantages of this new approach are discussed. A computer-aided-design (CAD) tool developed to automate the process of generating customized fractal layouts is discussed in Section V. The measurement results of a prototype fractal capacitor are the subject of Section VI.

II. Lateral Flux Capacitors

Fig. 1(a) shows a lateral flux capacitor. In this capacitor, the two terminals of the device are built using a single layer of metal, unlike a vertical flux capacitor, where two different metal layers must be used. As process technologies continue to scale, lateral fringing becomes more important. The lateral spacing of the metal layers s shrinks with scaling, yet the thickness of the metal layers t and the vertical spacing of the metal layers t_{ox} stay relatively constant. This means that structures utilizing lateral flux enjoy a significant improvement with process scaling, unlike conventional structures that depend on vertical flux. Fig. 1(b) shows a scaled lateral flux capacitor. It is obvious that the capacitor in Fig. 1(b) is larger than the one in Fig. 1(a).

Lateral flux can be used to increase the total capacitance obtained in a given area. Fig. 2(a) is a standard parallel-plate capacitor. In Fig. 2(b), the plates are broken into cross-connected sections [2]. As can be seen, a higher capacitance

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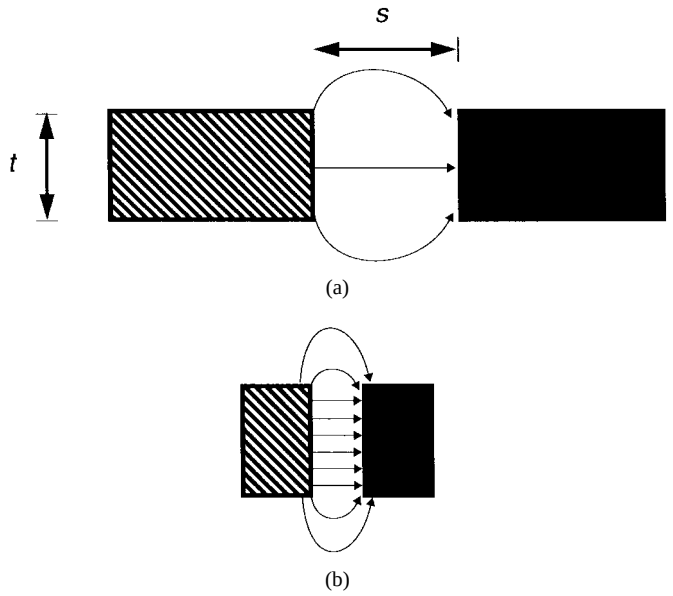

Fig. 1. Effect of scaling on lateral flux capacitors (a) before scaling and (b) after scaling.

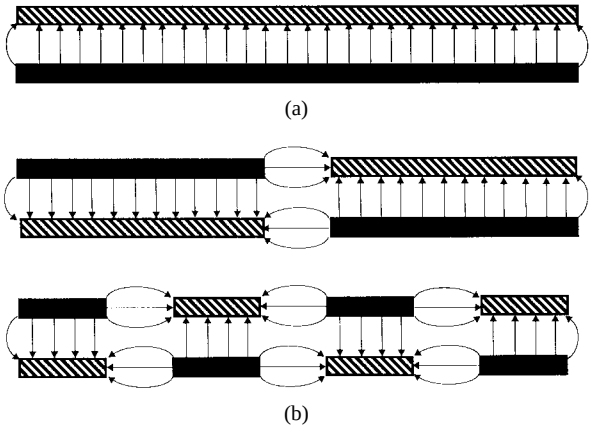

Fig. 2. Vertical flux versus lateral flux. (a) A standard parallel-plate structure and (b) cross-connected metal layers.

density can be achieved by using lateral flux as well as vertical flux. To emphasize that the metal layers are cross connected, the two terminals of the capacitors in Fig. 2(b) are identified with two different shades. The idea can be extended to multiple metal layers as well.

Fig. 3 shows the ratio of metal thickness to minimum lateral spacing t/s versus channel length for various technologies [3]–[5]. The trend suggests that lateral flux will have a crucial role in the design of capacitors in future technologies.

The increase in capacitance due to fringing is proportional to the periphery of the structure. Therefore, structures with large periphery per unit area are desirable. Methods for increasing this periphery are the subject of the following sections.

III. Fractals

A fractal is a mathematical abstract [6]. Some fractals are visualizations of mathematical formulas while others are the result of the repeated application of an algorithm, or a *rule*, to a *seed*. Many natural phenomena can best be described with

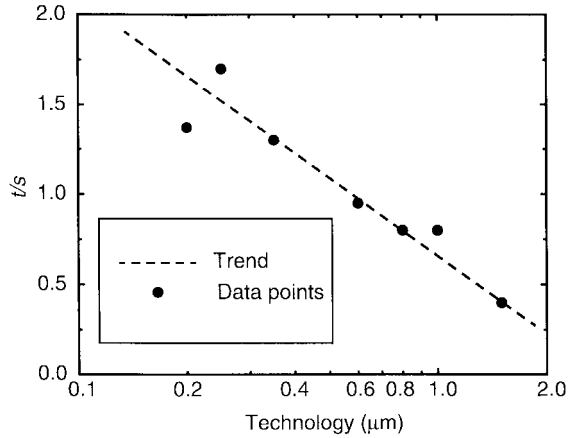

Fig. 3. Ratio of metal thickness to horizontal metal spacing versus technology (channel length).

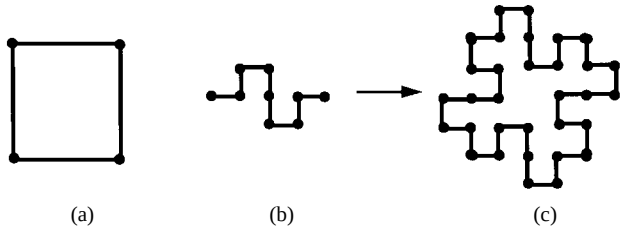

Fig. 4. Construction of a Koch curve. (a) An initiator, (b) a generator, and (c) the first step of the process.

the help of fractals. Examples include the shape of mountain ranges, clouds, coastlines, etc.

Some ideal fractals have a finite area but an infinite perimeter. The concept can be better understood with the help of an example. *Koch islands* are family of fractals first introduced as a crude model for the shape of a coastline. The construction of a Koch curve begins with an *initiator*, as shown in the example of Fig. 4(a). A square is a simple initiator with $M = 4$ sides. The construction continues by replacing each segment of the initiator with a curve called a *generator*, an example of which is shown in Fig. 4(b) that has $N = 8$ segments. The size of each segment of the generator is $r = 1/4$ of the initiator. By recursively replacing each segment of the resulting curve with the generator, a fractal border is formed. The first step of this process is depicted in Fig. 4(c). The total area occupied remains constant throughout the succession of stages because of the particular shape of the generator. A more complicated Koch island can be seen in Fig. 5. The associated initiator of this fractal has four sides, and its generator has 32 segments. It can be noted that the curve is self-similar, i.e., each section of it looks like the entire fractal. As we zoom in in Fig. 5, more detail becomes visible, and this is the essence of a fractal.

Fractal dimension D is a mathematical concept that is a measure of the complexity of a fractal. The dimension of a flat curve is a number between one and two, which is given by

$$D = \frac{\log(N)}{\log\left(\frac{1}{r}\right)} \tag{1}$$

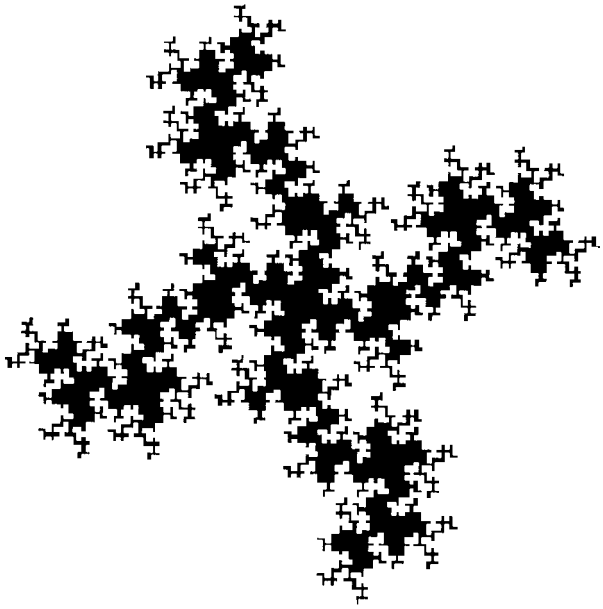

Fig. 5. A Koch island with $M = 4, N = 32$, and $r = 1/8$.

where N is the number of segments of the generator and r is the ratio of the generator segment size to the initiator segment size. The dimension of a fractal curve is a fraction. In particular, it exceeds one, which is the intuitive dimension of curves. A curve that has a high degree of complexity, or D, fills out a two-dimensional flat surface more efficiently. The fractal in Fig. 4(c) has a dimension of 1.5, whereas for the border line of Fig. 5, $D = 1.667$.

For the general case where the initiator has M sides, the periphery of the initiator is proportional to the square root of the area

$$P_0 = k \cdot \sqrt{A} \tag{2}$$

where k is a proportionality constant that depends on the geometry of the initiator. For example, for a square initiator, k equals four, and for an equilateral triangle, $k = 2 \cdot \sqrt[4]{27}$. After n successive applications of the generation rule, the total periphery is

$$P = k\sqrt{A} \cdot (Nr)^n \tag{3}$$

and the minimum feature size (the resolution) is

$$l = \frac{k\sqrt{A}}{M} \cdot r^n. \tag{4}$$

Eliminating n from (3) and (4) and combining the result with (1), we have

$$P = \frac{k^D}{M^{D-1}} \cdot \frac{\left(\sqrt{A}\right)^D}{l^{D-1}}. \tag{5}$$

Equation (5) demonstrates the dependence of the periphery on parameters such as the area and the resolution of the fractal border. It can be seen from (5) that as l tends toward zero, the periphery goes to infinity; therefore, it is possible to generate fractal structures with very large perimeters in any given area. However, the total periphery of a fractal curve is limited by the attainable resolution in practical realizations.

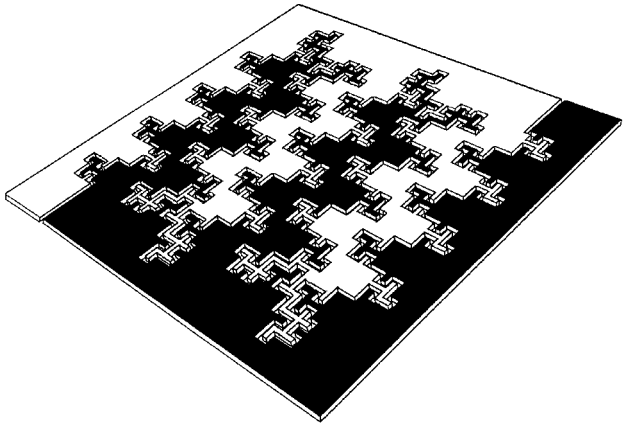

Fig. 6. Three-dimensional representation of a fractal capacitor using a single metal layer.

IV. Fractal Capacitor Structures

In Section II, we suggested that it is possible to increase the capacitance density of parallel-plate capacitors by exploiting lateral fringing fields in cross-connected metal layers. In Section III, we introduced fractals as geometrical structures with large perimeters. These suggest that fractals are good candidates for use in lateral flux capacitors. Although lithography limitations prevent fabrication of a real fractal, one can use quasi-fractal geometries with feature sizes limited by lithography.

The final shape of a fractal can be tailored to almost any form. The flexibility arises from the fact that there are a wide variety of geometries that can be used as the initiator and as the generator. It is also possible to use different generators during each step. This is an advantage for integrated circuits, where flexibility in the shape of the layout is desired.

Fig. 6 is a three-dimensional representation of a fractal capacitor. This capacitor uses only one metal layer with a fractal border. For a better visualization of the overall picture, the terminals of this square-shaped capacitor have been identified using two different colors. As was discussed before, multiple cross-connected metal layers may be used to improve capacitance density further.

One advantage of using lateral flux capacitors in general, and fractal capacitors in particular, is the reduction of the bottom-plate capacitance. This reduction is due to two reasons. First, the higher density of the fractal capacitor (compared to a standard parallel-plate structure) results in a smaller area. Second, some of the field lines originating from one of the bottom plates terminate on the adjacent plate instead of the substrate, which further reduces the bottom-plate capacitance, as shown in Fig. 7. Because of this property, some portion of the parasitic bottom-plate capacitor is converted into the more useful plate-to-plate capacitance.

The capacitance per unit area of a fractal structure depends on the dimension of the fractal. To improve the density of the layout, fractals with large dimensions should be used. The concept of fractal dimension is demonstrated in Fig. 8. The structure in Fig. 8(a) has a lower dimension compared to the one in Fig. 8(b), so the density (capacitance per unit area) of the latter is higher.

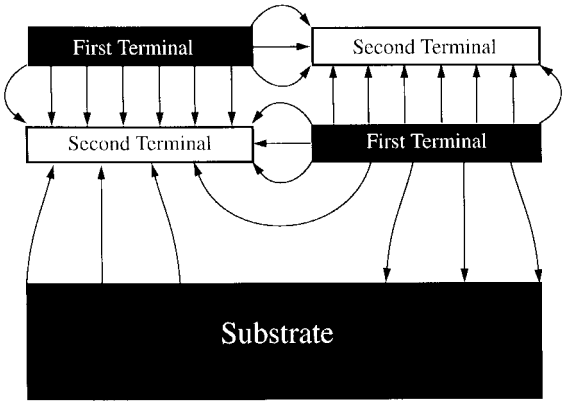

Fig. 7. Reduction of the bottom-plate parasitic capacitance.

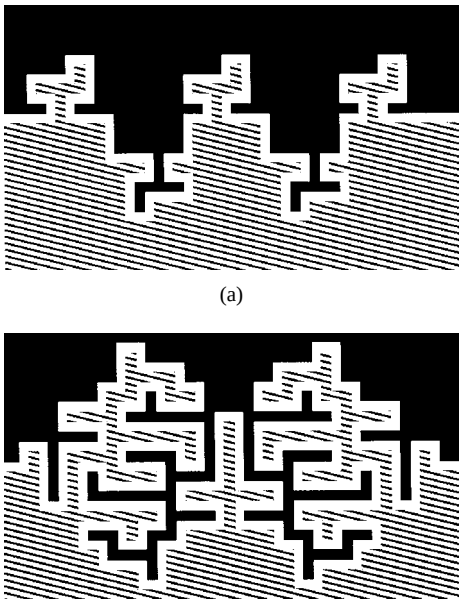

Fig. 8. Fractal dimension of (a) is smaller than that of (b).

To demonstrate the dependence of capacitance density on dimension and lateral spacing of the metal layers, a first-order electromagnetic simulation was performed on two families of fractal structures. In Fig. 9, the boost factor is plotted versus horizontal spacing of the metal layers. The boost factor is defined as the ratio of the total capacitance of the fractal structure to the capacitance of a standard parallel-plate structure with the same area. The solid line corresponds to a family of fractals with a moderate fractal dimension of 1.63, while the dashed line represents another family of fractals with $D = 1.80$, which is a relatively large value for the dimension. In this first-order simulation, it is assumed that the vertical spacing and the thickness of the metal layers are kept constant at a 0.8-μm level. As can be seen in Fig. 9, the amount of boost is a strong function of the fractal dimension as well as scaling.

The degradation of the quality factor, Q is modest because the fractal structure automatically limits the length of the thin metal sections to a few micrometers, keeping the series resistance reasonably small. For applications that require low series

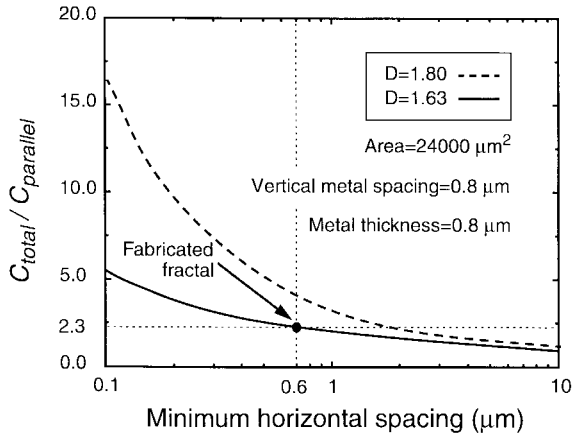

Fig. 9. Boost factor versus lateral spacing.

resistance, lower dimension fractals may be used. Fractals add one more degree of freedom to the design of capacitors, allowing the capacitance density to be traded for a lower series resistance.

In current IC technologies, there is usually tighter control over the lateral spacing of metal layers compared to the vertical thickness of the oxide layers, from wafer to wafer and across the same wafer. Lateral flux capacitors shift the burden of matching away from oxide thickness to lithography. In other words, by using lateral flux, matching characteristics can improve. Furthermore, the pseudorandom nature of the structure can also compensate, to some extent, for the effects of nonuniformity of the etching process. To achieve accurate ratio matching, multiple copies of a unit cell should be used.

Another simple way of increasing capacitance density is to use an interdigitated capacitor depicted in Fig. 10 [2], [7]. One disadvantage of such a structure compared to fractals is its inherent parasitic inductance. Most of the fractal geometries randomize the direction of the current flow and thus reduce the effective series inductance, whereas for interdigitated capacitors, the current flow is in the same direction for all the parallel stubs. In addition, fractals usually have lots of rough edges that accumulate electrostatic energy more efficiently compared to interdigitated capacitors. To demonstrate this, an interdigitated capacitor as well as a fractal structure were simulated. The fractal under consideration had a moderate dimension of 1.63. The interdigitated capacitor and the fractal structure had the exact same area and perimeter, yet the capacitance of the interdigitated capacitor was 15% smaller. Furthermore, interdigitated structures are more vulnerable to nonuniformity of the etching process. However, the relative simplicity of the interdigitated capacitor does make it useful in some applications.

The woven structure shown in Fig. 11 may also be used to achieve high capacitance density. The vertical lines are in metal-2 and horizontal lines are in metal-1. The two terminals of the capacitor are identified using different shades. Compared to an interdigitated capacitor, a woven structure has much less inherent series inductance. The current flowing in different directions results in a higher self-resonant frequency. In addition, the series resistance contributed by vias is smaller than

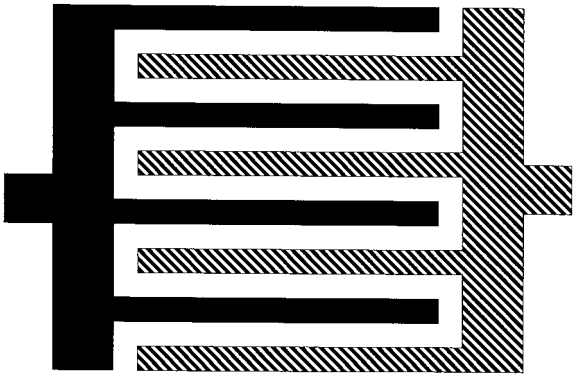

Fig. 10. An interdigitated capacitor.

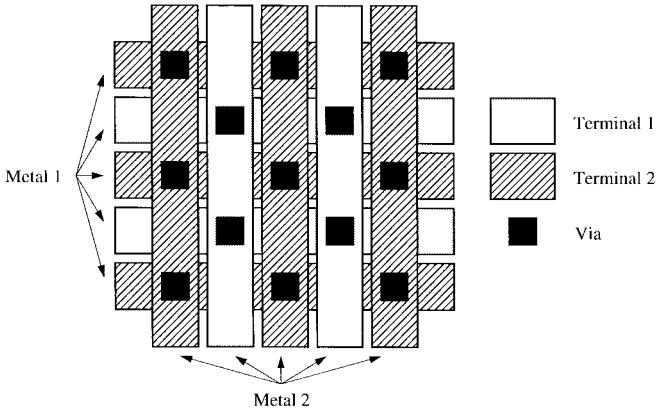

Fig. 11. A woven structure.

that of an interdigitated capacitor because cross connecting the metal layers can be done with greater ease. However, the capacitance density of a woven structure is smaller compared to an interdigitated capacitor with the same metal pitch because the capacitance contributed by the vertical fields is smaller.

V. CAD Tool

One problem in the use of fractal structures is their generation and predictability. A CAD tool has been developed that automatically generates customized fractal layouts. *Layout generator for fractal capacitors* (LGFC) is an interactive program that accepts a technology file as well as a fractal library as inputs. The fractal library contains information about different families of fractals. The library file has a simple format, and the user can easily modify the existing fractals or add new ones. The technology file contains information on the characteristics of the process being used, more specifically, the design rules.

The user has to provide some information such as the desired area and the final shape of the layout. The program creates the layout, produces a report, and also generates a three-dimensional description of the fractal structure in various field-solver formats (e.g., Maxwell [8]). The electromagnetic simulator uses this information to simulate fields and calculate the value of the capacitor as well as the parasitic resistance and inductance. The operation of the CAD tool is summarized in Fig. 12.

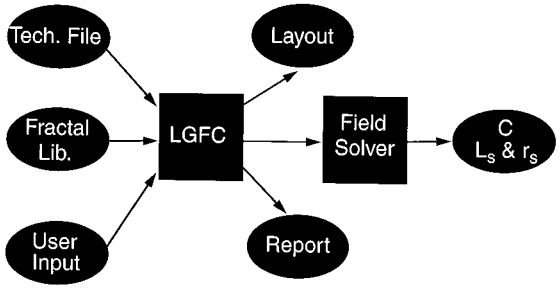

Fig. 12. Overview of LGFC, the layout generator for fractal capacitors.

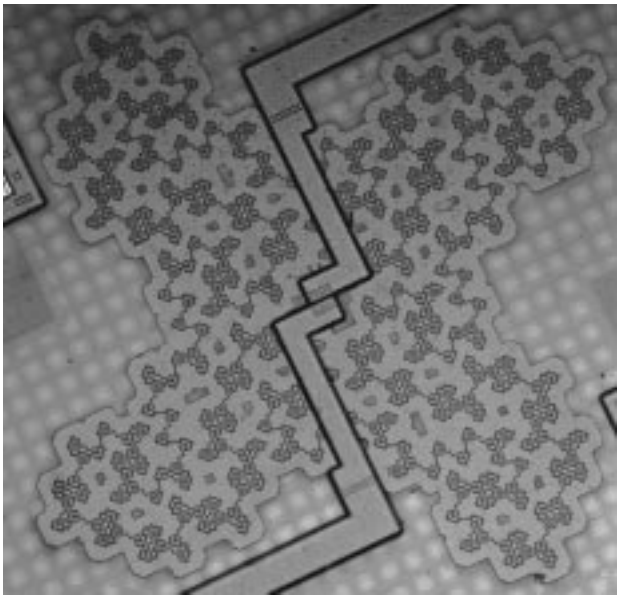

Fig. 13. Die micrograph of a prototype fractal capacitor.

VI. Measurements

To demonstrate the feasibility of fractal capacitors, a prototype structure has been implemented in a five-metal-layer process. The die micrograph of the capacitor is shown in Fig. 13. The lateral metal spacing is 0.6 μm, while the vertical spacing and metal layer thickness are both 0.8 μm. The total area of the capacitor is 24 000 μm^2. This Koch-island fractal structure is not necessarily the most efficient choice, especially because of the wasted areas on the sides, but was chosen on the basis of aesthetic considerations. Four cross-coupled metal layers are used as the body of the structure, and the fifth metal layer is solely used to make connections to the capacitor terminals. The need for an additional metal layer to make contacts to the capacitor terminals is only a property of this particular fractal and is not an inherent characteristic of fractal structures in general. Fig. 6 is an example of a square-shaped structure that does not have this limitation. In each metal layer, there is an inner and outer conductor and a fractal border.

The results of high-frequency two-port network measurements are shown in Fig. 14. The measurement is performed using Cascade probes. The two ports are the two terminals of the capacitor relative to ground, so the admittance of the capacitor under test would appear as Y_{12}. The plot depicts the

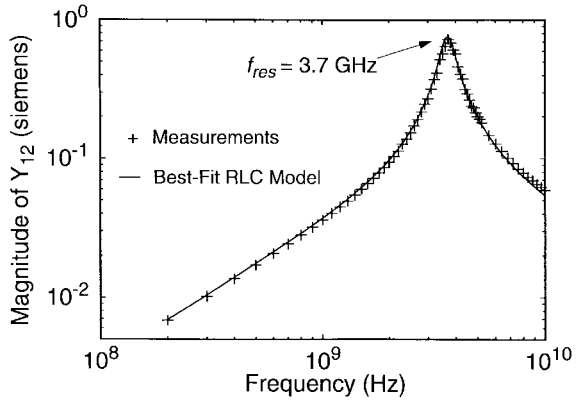

Fig. 14. Two-port network measurements.

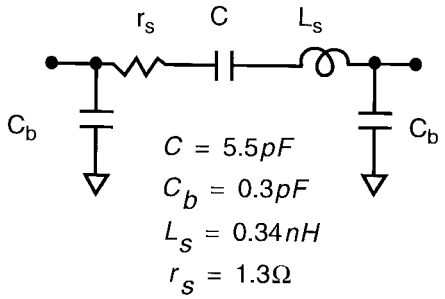

Fig. 15. Best fit parameters.

magnitude of Y_{12} as a function of frequency. The structure exhibits a self-resonant frequency of 3.7 GHz. The solid curve in the plot is the magnitude of Y_{12} of the best fit RLC model, which is shown in Fig. 15. Field-solver simulations predict a capacitance of 5.4 pF compared to the mean measured value of 5.5 pF. The series inductance of the lines connecting the pads to the capacitor terminals is simulated to be 0.3 nH, which accounts for 90% of the measured series inductance. This means that the self-resonance frequency of the fractal capacitor without the connecting stubs is much higher than the measured value. The series resistance is 1.3 Ω, resulting in a Q of about 23 at 1 GHz. About 80% of the series resistance can be attributed to vias and connecting stubs, so with careful placement of the vias, the Q can be significantly increased. The parasitic bottom-plate capacitance is measured to be 0.3 pF. This value is calculated by subtracting Y_{12} from Y_{11}. Although this particular fractal has a moderate dimension, the overall capacitance density is 2.3 times larger than a standard parallel-plate capacitor.

To investigate the matching properties, the capacitance value is measured for various sites across an 8-in wafer, as shown in Fig. 16. The solid rectangles represent the approximate location of the measured sites. Note that the test sites are far apart from each other, and the minimum spacing between two adjacent test sites is 22 mm. Fig. 17 depicts the distribution of the measured capacitance values. The distribution has a mean value of 5.5 pF and a standard deviation of 83 fF. It is noteworthy that the five points with the value of 5.4 pF in the histogram correspond to the central sites, which show a much smaller standard deviation of 9.4 fF. These five sites are

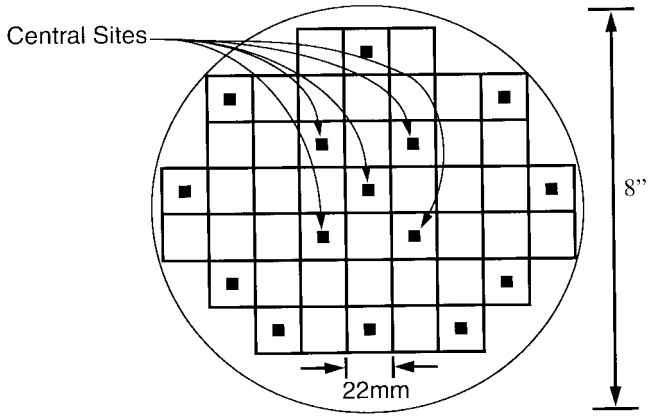

Fig. 16. Measurement sites across the wafer.

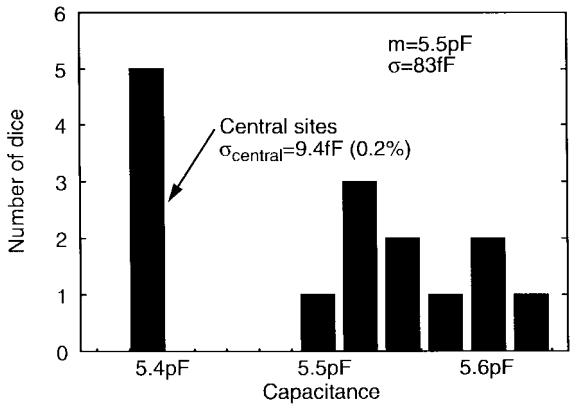

Fig. 17. Capacitance distribution across the wafer.

spread over an area of 60 $\times$ 60 mm^2, as shown in Fig. 16, yet the standard deviation is less than 0.2%. The capacitance increases with distance from the center of the wafer, and the small mismatch is mostly due to systematic variation in oxide thickness across the wafer.

VII. Conclusion

In this paper, a linear capacitor structure has been introduced that uses lateral flux as well as vertical flux to achieve high capacitance per unit area. The structure exploits cross-connected metal layers with a fractal border. Aside from the higher density, one advantage of the proposed structure is the reduction of bottom-plate capacitance due to the smaller area. In addition, since some of the field lines terminate on the adjacent plate instead of the substrate, the bottom-plate capacitance is further reduced. The capacitance density of fractal structures increases with scaling of the process technologies, which makes them more attractive compared to standard parallel-plate capacitors. A CAD tool has been developed to generate customized fractal layouts, in which the final shape of a fractal can be tailored to the user's requirements. A prototype fractal capacitor is implemented with 0.6-μm metal spacing. The overall capacitance density of this structure is measured to be 2.3 times better than a parallel-plate capacitor, with much larger boost factors possible as technology scales.

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