# Lateral IMPATT Diodes in Standard CMOS Technology

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## Abstract

We investigate the use of a lateral IMPATT diode built in 0.25μm CMOS technology as a high frequency power source. These diodes are monolithically integrated in coplanar waveguides and characterized by S-parameter measurements from 40 MHz to 110 GHz. These measurements show excellent agreement with predictions of theoretical models. To our knowledge, this is the first such structure built in a standard CMOS technology.

## Introduction

There is presently significant interest in developing low cost millimeter-wave systems for applications ranging from communications to automobile anti-collision radar systems. CMOS technologies are particularly appealing from a cost reduction and systems integration standpoint. However, these systems typically operate at frequencies beyond currently achievable CMOS transistor $f_T$, rendering conventional CMOS circuit techniques useless. As such, in this work we have investigated the use of a lateral IMPATT (IMPact Avalanche Transit Time) diode as a high frequency (e.g. 77GHz) power source, built in a conventional 0.25μm CMOS technology.

IMPATT diodes offer some of the highest available output powers for semiconductor devices operating at microwave and millimeter wave frequencies. Originally developed in 1958 [1], various IMPATT diode structures have been reported over the years. These include mesa, planar, distributed, and lateral structures [2]. However, all of these structures, whether vertical or horizontal, require special fabrication techniques and process modifications to achieve the desired performance. The basic theory was well described by Read [1] in his original paper. In addition, Sze [3] and DeLoach [4] have reviewed the theory in the light of experimental results. Briefly, an IMPATT diode consists of three regions, an avalanche breakdown region, drift region and inactive region as shown in Fig. 1.

An IMPATT is biased into reverse breakdown, and a frequency-dependent negative resistance arises from phase delay between the current and voltage waveforms in the device.

Maximum output power is facilitated by arranging for V and I to be out of phase with one another by an angle of 180°. The first 90° of phase shift is achieved within the avalanche region. The remaining 90° is obtained by adjusting the drift region length.

## Device Structure and Properties

For our design, the $p^+$, n, and $n^+$ regions of the IMPATT diode (Fig. 1) are implemented using standard source/drain, n-well, and ohmic contact diffusion regions, respectively. The dimensions of the diode tested (0.5μm x 100μm) are based on two considerations: (1) reducing the resistance of the inactive region by increasing the diode width while also keeping it below a quarter wavelength to minimize any resonance or phasing problems, and (2) increasing the power efficiency by reducing the junction area and hence the junction capacitance.

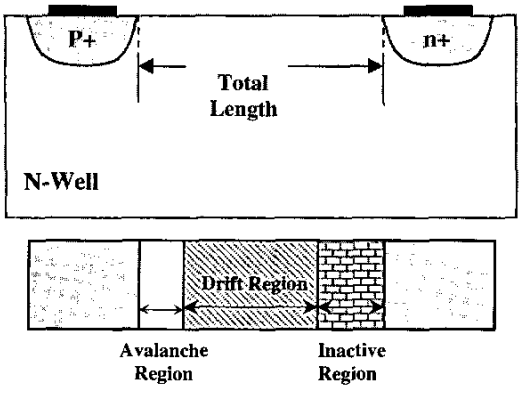


Fig. 1. Lateral IMPATT diode structure, showing the avalanche region, drift region and the inactive region.



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Designing IMPATT diodes in standard CMOS technology reveals the importance of the n-well impurity concentration as a key factor in controlling all of the critical design parameters: breakdown voltage (Fig. 2); avalanche frequency; and avalanche, drift, and inactive region lengths. Accounting for the vertical impurity concentration gradient of the n-well (lowest at the surface) and spherical junction effects, and based on the measured breakdown voltage (9V for 1mA reverse current) we may extract the doping profile of the n-well [3].

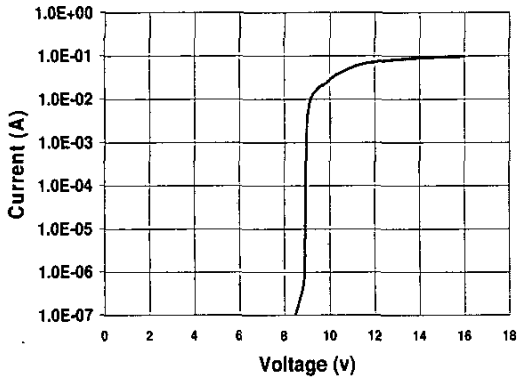



Fig. 2. I-V characteristic of IMPATT diode showing the transition to avalanche breakdown at 9V.

Additionally, the retrograde diffusion profile affects the area of the junction capacitance before and after breakdown. With the reverse bias voltage less than the breakdown value, the junction capacitance decreases as the voltage increases (Fig. 3). This figure is obtained by averaging five measurements at each bias voltage.

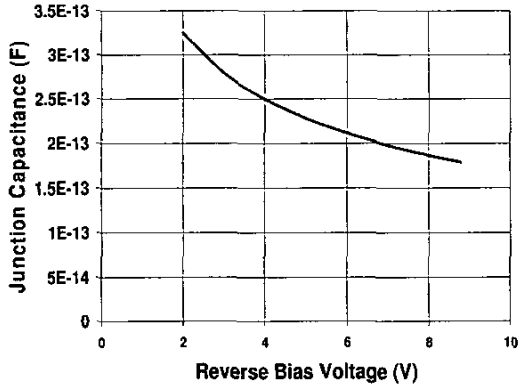



Fig. 3. Junction capacitance as a function of reverse bias voltage (before breakdown).

## RF Measurements

These diodes have been monolithically integrated in coplanar waveguides (Fig. 4) and characterized by S-parameter measurements from 40 MHz to 110 GHz. By carefully designing the Ground-Signal-Ground (GSG) pad we are able to mitigate the undesired oscillations that typically disturb S-parameter measurements of IMPATT diodes.

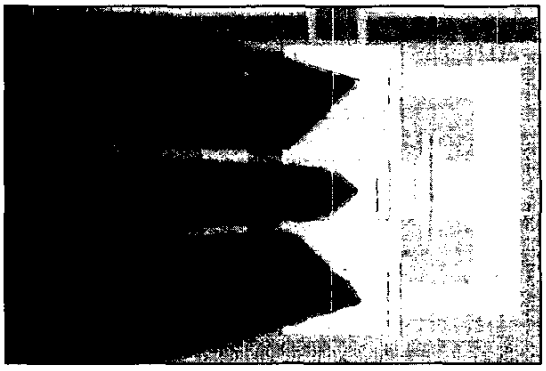
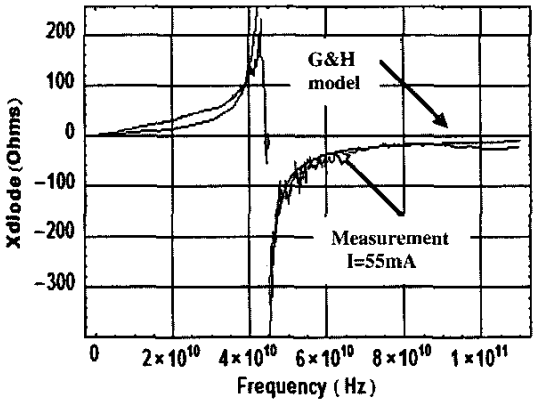


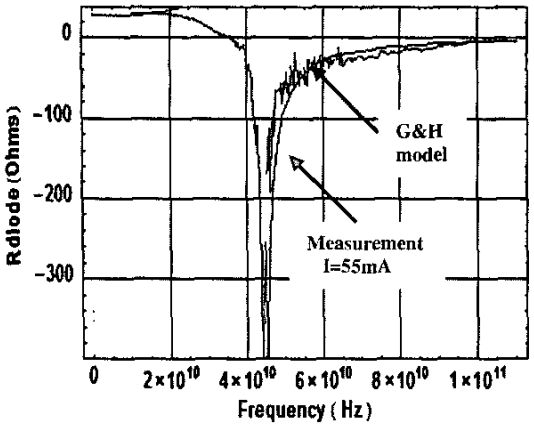
Fig. 4. Die photo of the integrated IMPATT diode and the RF probe.

Based on four measured data points—breakdown voltage, $R_{dc}$ after breakdown, $C_{diode}$ before breakdown, and avalanche frequency—the model proposed in [5] (G&H Model) was constructed. As seen, the model's impedance profile matches the measured data closely (Fig. 5).




(a)

Fig. 5a. Comparison between measured impedance at I=55mA and the model introduced in [4] based on the four measured data points. (a) Imaginary part.




(b)

Fig. 5b. Comparison between measured impedance at I=55mA and the model introduced in [4] based on the four measured data points. (b)Real part.

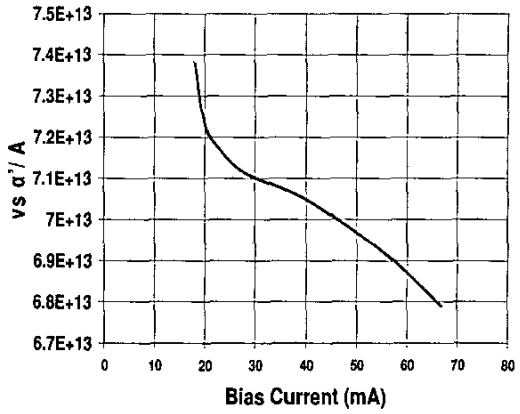



Fig. 6. Illustration of how increasing the bias current affects the saturation velocity and the ionization constant.

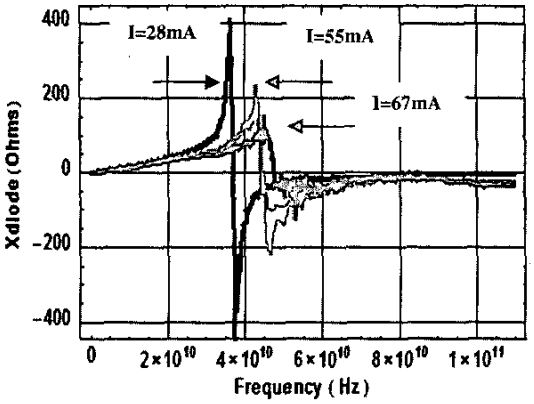
## Results and Discussion

As shown in Table 1, the ratio of the avalanche frequency to the square root of the bias current decreases slightly instead of remaining constant. This is caused by the temperature increase due to increasing bias current. This increase in temperature causes the saturation drift velocity and the ionization constant to decrease (Fig. 6). Additionally, Table 1 shows that the avalanche frequency increases with increasing bias current (Fig. 7). This is as expected and furthermore provides a convenient means for tuning the IMPATT diode.

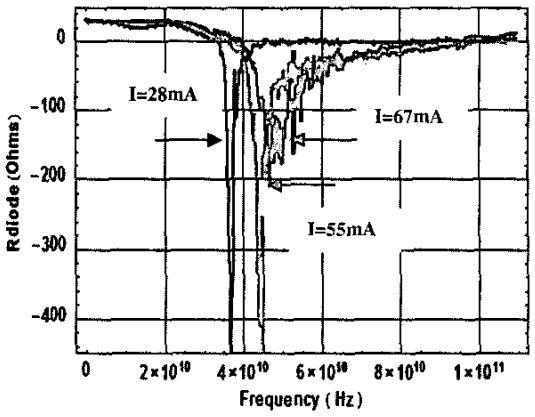
Table 1 Ratio of avalanche frequency to the square root of the bias current.

| Bias Voltage [V] | Bias Current [mA] | Avalanche Frequency $f_a$ [GHz] | $f_a / \sqrt{[I_{bias}]}$ |
|---|---|---|---|
| 9.8 | 23 | 28.3 | 187 |
| 10 | 28 | 31.1 | 186 |
| 10.5 | 40 | 37 | 185 |
| 11 | 55 | 43 | 183 |
| 11.5 | 67 | 47 | 182 |

For very high frequencies the real part of the IMPATT diode impedance becomes positive because of the increasing dominance by the series resistance introduced by the inactive region.




(a)




(b)

Fig. 7. IMPATT impedance data extracted from the $S_{11}$ parameter measurements. As expected, the increase in avalanche frequency is proportional to the square root of the bias current. (a) Imaginary part. (b) Real part.

## Conclusion

Once the methodology is understood (Fig. 8) these devices can be designed in any standard CMOS technology that has an n-well with impurity concentration less than about $5x10^{17}cm^{-3}$. Above this approximate upper limit on impurity concentration, tunneling effects begin to dominate the breakdown process, preventing avalanching. Within that limit, the selection of process technology should be based on the desired operating frequency as it is directly proportional to the n-well impurity concentration. These devices appear well suited for use in millimeter-wave integrated circuits where minimum cost and high integration are valued.

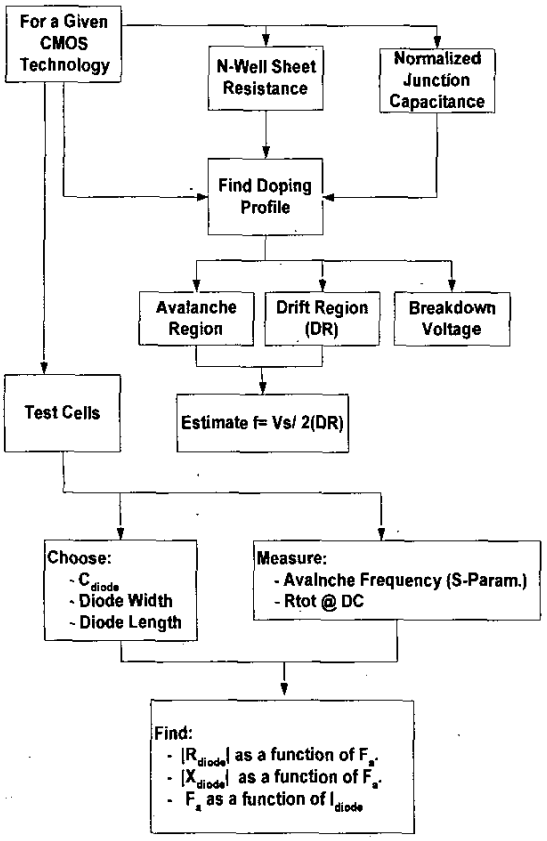



Fig. 8. For a given CMOS technology, certain key parameters can be extracted to determine the IMPATT design specifications.


## Acknowledgement

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