

# A 5GHz, 1mW CMOS Voltage-Controlled Differential Injection-Locked Frequency Divider

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# OUTLINE

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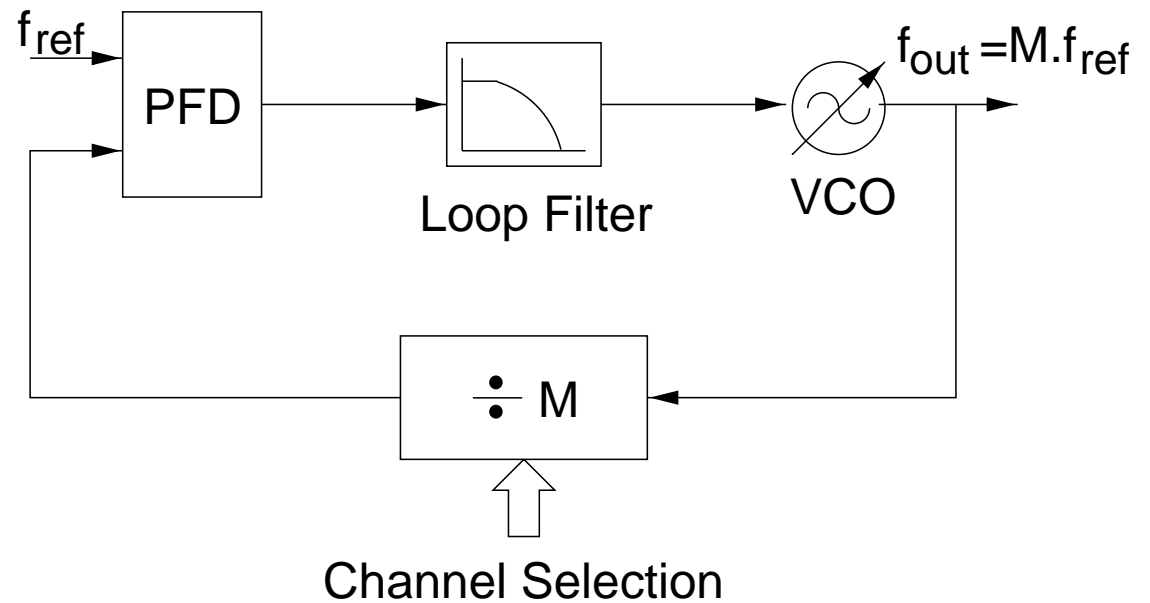
- motivation
- injection–locked frequency dividers (ILFDs)
  - mathematical model
  - circuit implementation
  - design issues
    - \* optimal inductor design
- measurement results
- summary
- conclusion

# MOTIVATION

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- wireless systems:
  - are narrowband
  - require frequency synthesizers
  - require low power operation
- PLL-based frequency synthesizer require frequency dividers

- conventional dividers:
  - wideband
  - power hungry



# IDEA

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- design a low–power and narrowband frequency divider

use resonators to trade off bandwidth for power

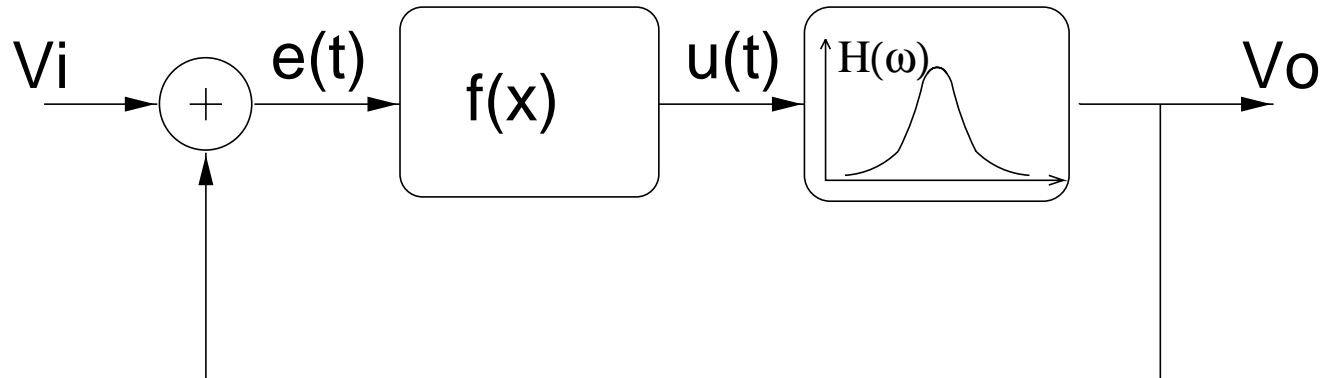
# INJECTION-LOCKED OSCILLATORS

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- by impressing an oscillator with an external (incident) signal, frequency locking can be achieved
    - first-harmonic injection locked oscillators ( $f_i = f_o$ )
    - subharmonic injection locked oscillators ( $f_i = \frac{1}{N} f_o$ )
    - superharmonic injection locked oscillators ( $f_i = N \times f_o$ )
- injection-locked frequency dividers (ILFDs)

# ILFD MODEL

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$$v_o(t) = V_o \cos(\omega_o t)$$

$$v_i(t) = V_i \cos(\omega_i t + \phi)$$

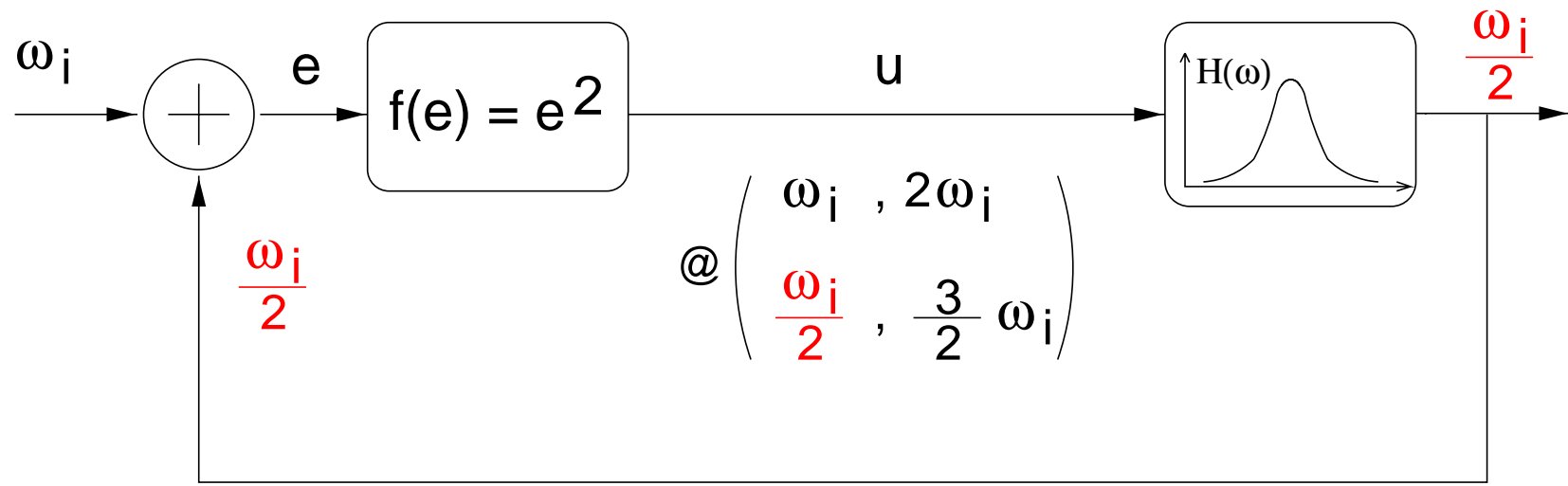
$$u(t) = f[e(t)] = f[v_o(t) + v_i(t)]$$

$$H(\omega) = \frac{H_0}{1 + j2Q \frac{\omega - \omega_r}{\omega_r}}$$

- oscillation condition should be satisfied in the presence of the incident signal.

# SIMPLIFIED PICTURE

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$$e = \cos(\omega_i t) + \cos\left(\frac{\omega_i}{2} t\right)$$

$$u = \left[ \cos(\omega_i t) + \cos\left(\frac{\omega_i}{2} t\right) \right]^2$$

$$u = 1 + \frac{1}{2} \cos(2\omega_i t) + \frac{1}{2} \cos(\omega_i t) + \cos\left(\frac{3\omega_i}{2} t\right) + \cos\left(\frac{\omega_i}{2} t\right)$$

## SPECIAL CASE (DIVIDE-BY-TWO)

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$$f(e) = a_0 + a_1 e + a_2 e^2 + a_3 e^3$$

- phase condition:

$$\left| \frac{\Delta\omega}{\omega_r} \right| < \left| \frac{H_0 a_2 V_i}{2Q} \right|, \quad \frac{H_0}{Q} = \frac{LQ\omega_r}{Q} = L\omega_r$$

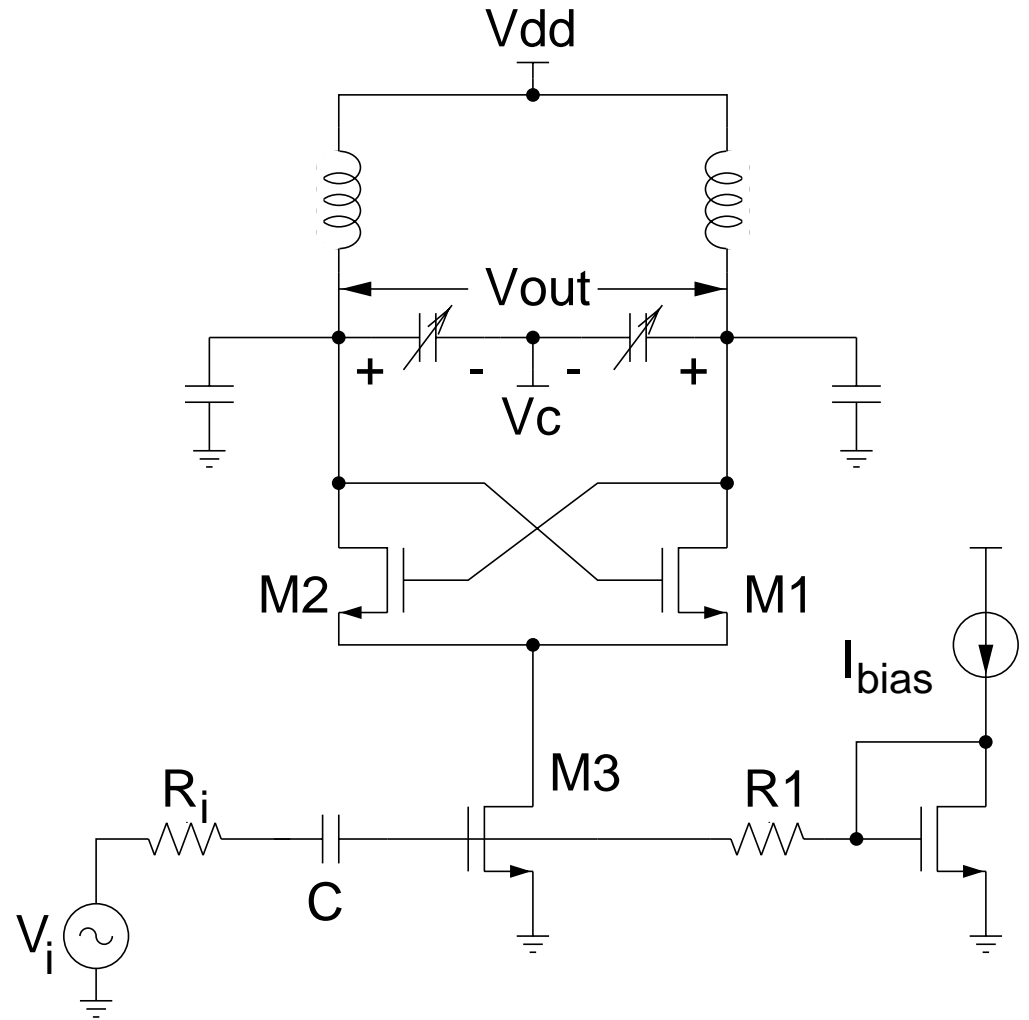
- gain condition:

$$H_0 \left( a_1 + \frac{3}{2} a_3 V_i^2 + a_2 V_i \cos(\phi) \right) < 1$$



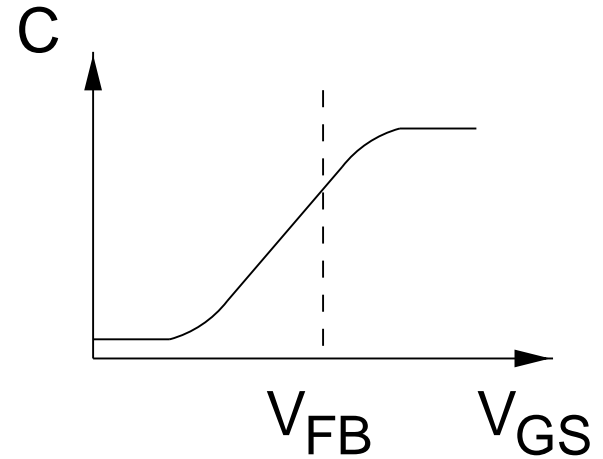
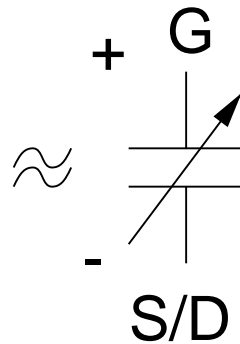
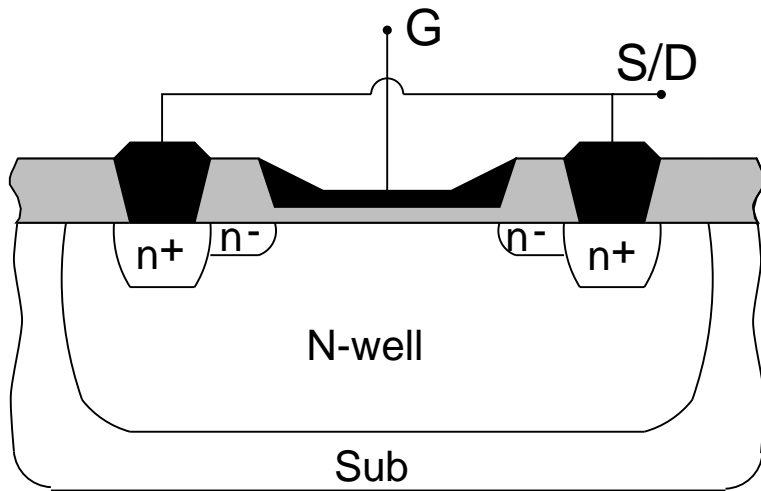
# VOLTAGE-CONTROLLED DIFFERENTIAL ILFD

- $0.24\mu\text{m}$  CMOS
- $V_{\text{dd}}=1.5\text{V}$
- $I_{\text{bias}}=300\mu\text{A}$
- $f_o=2.25\text{GHz}$
- $f_i=4.5\text{GHz}$



# VARACTOR

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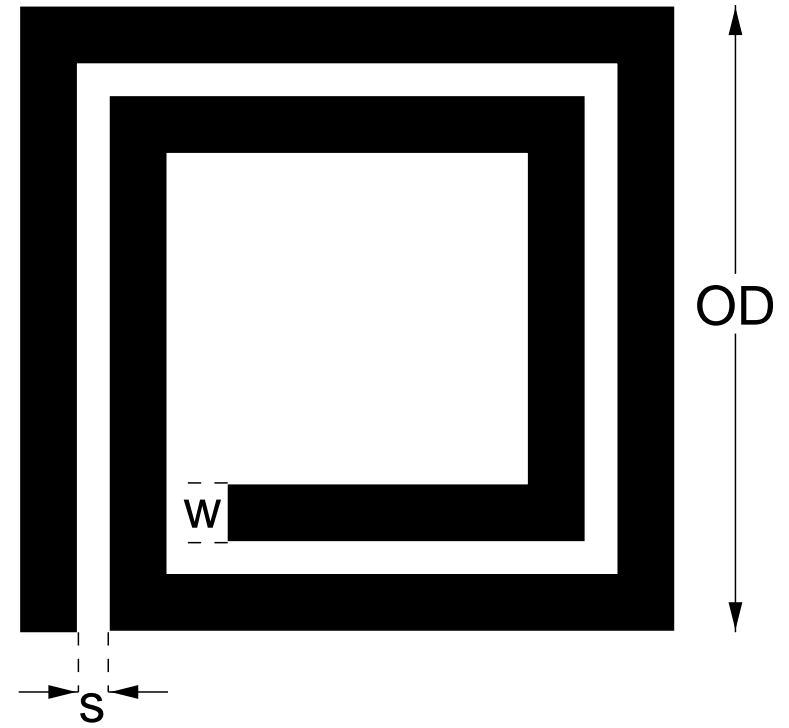
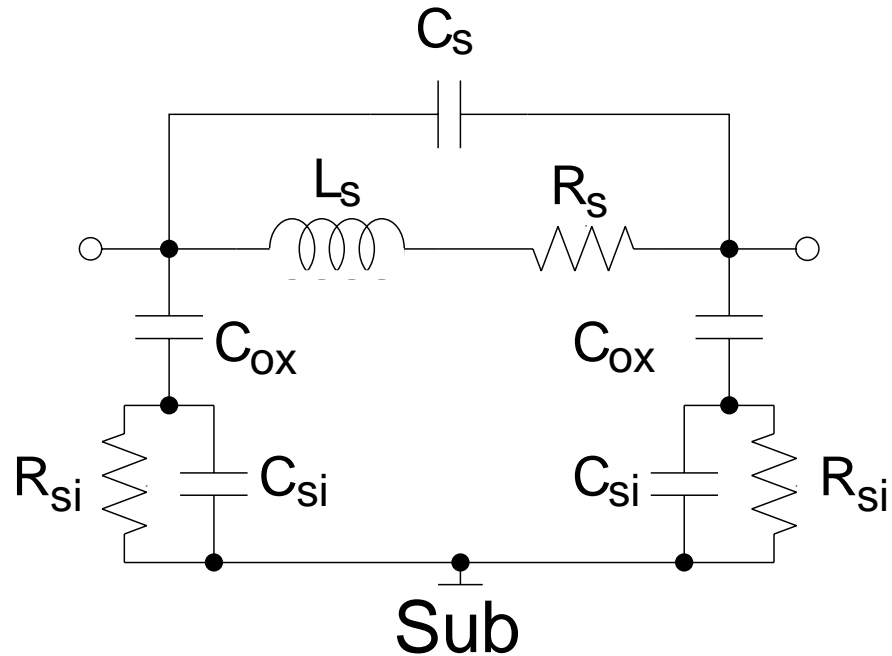
- accumulation mode MOS capacitor
  - large quality factor ( $> 60$  @ 2.5GHz)
  - flat-band voltage  $\approx$  zero volt

# INDUCTOR DESIGN

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- maximum locking range  $\Rightarrow$  maximize  $L$
- minimum power consumption  $\Rightarrow$  maximize  $LQ$

# INDUCTOR DESIGN



- design parameters:
  - w: metal width
  - s: metal spacing
  - OD: outer dimension
  - n: number of turns

# INDUCTOR DESIGN

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- in planar spiral inductors maximizing  $L$  does not maximize  $LQ$

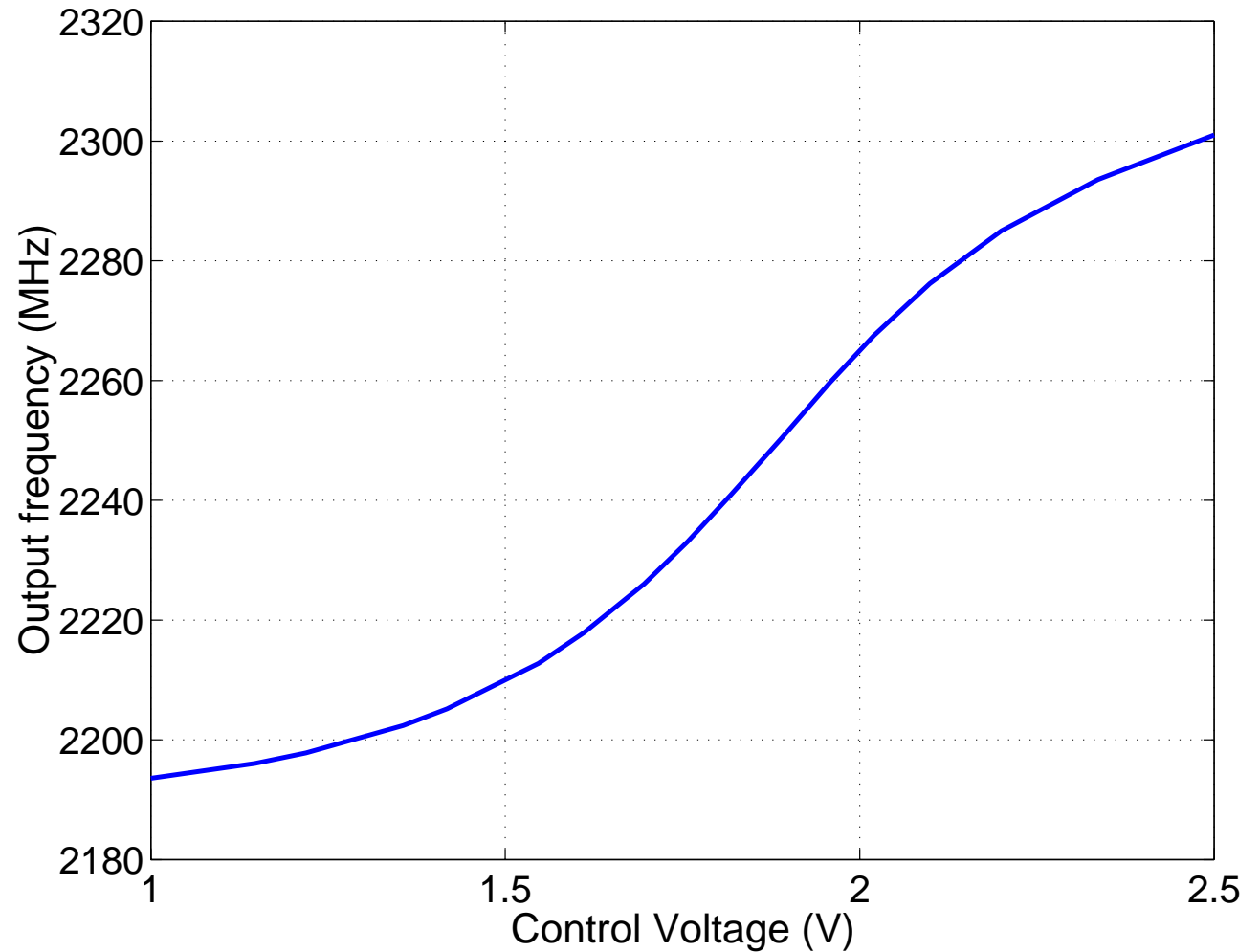


maximize  $L$  for a given  $LQ$

# MEASUREMENT (FREE-RUNNING OSCILLATION)

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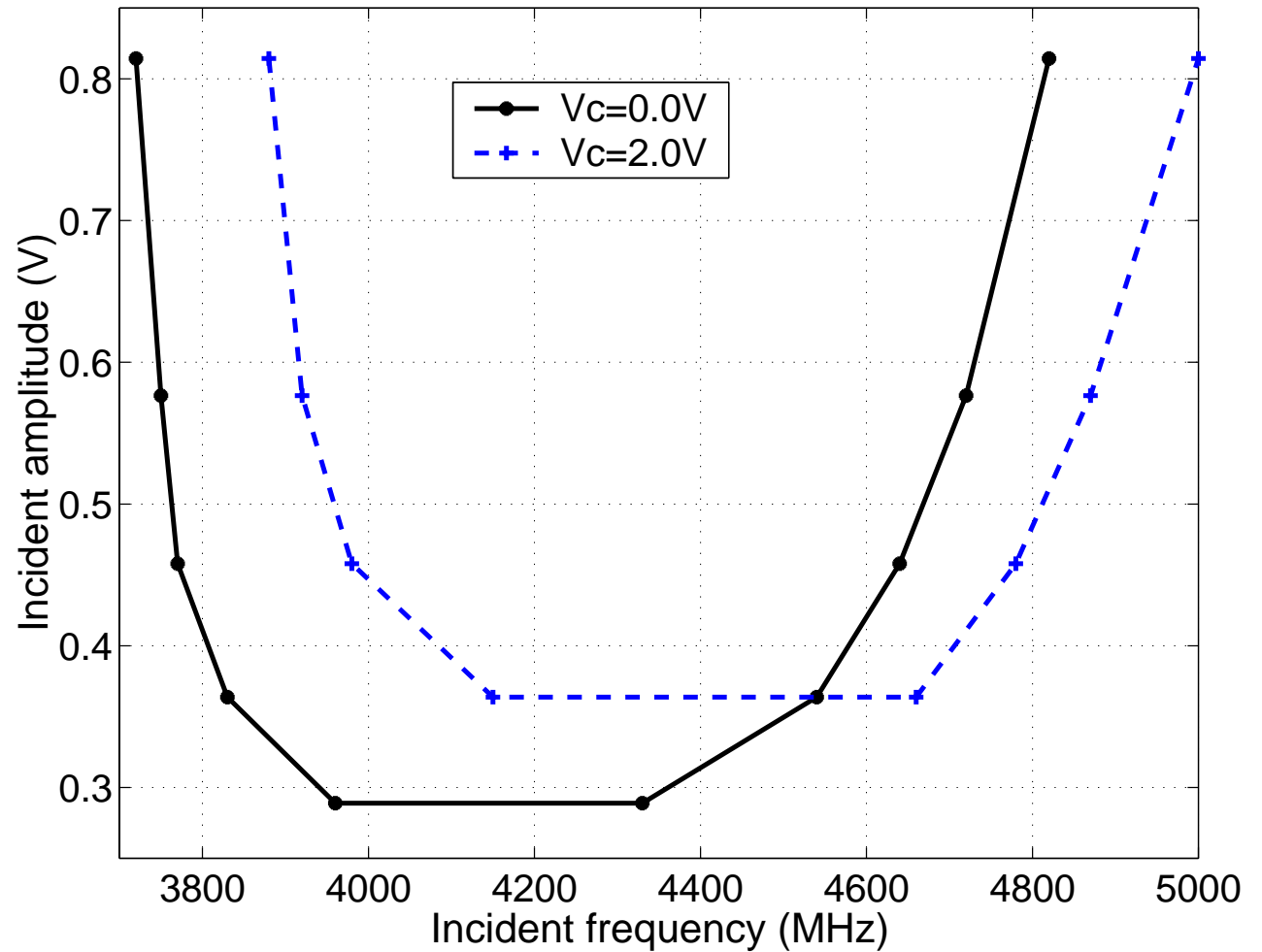
- $0.24\mu\text{m}$  CMOS
- $V_{\text{dd}}=2.0\text{V}$
- $I_{\text{bias}}=600\mu\text{A}$
- $\Delta f=110\text{MHz}$
- $\frac{\Delta f}{f_o}=5\%$
- $\Delta V_c=1.5\text{V}$



# MEASUREMENTS (FREQUENCY RANGE)

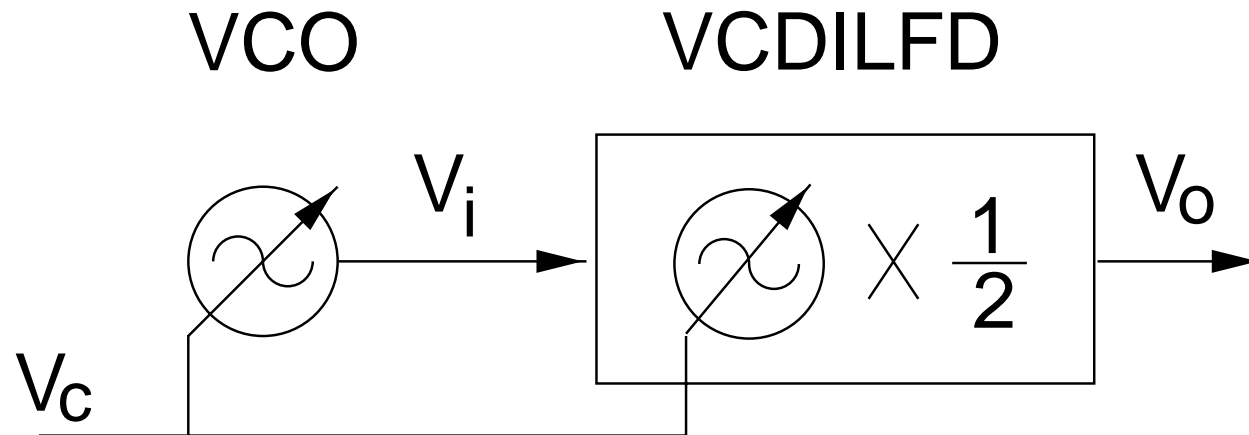
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- $0.24\mu\text{m}$  CMOS
- $V_{\text{dd}}=1.5\text{V}$
- $I_{\text{bias}}=300\mu\text{A}$



# TRACKING ILFD

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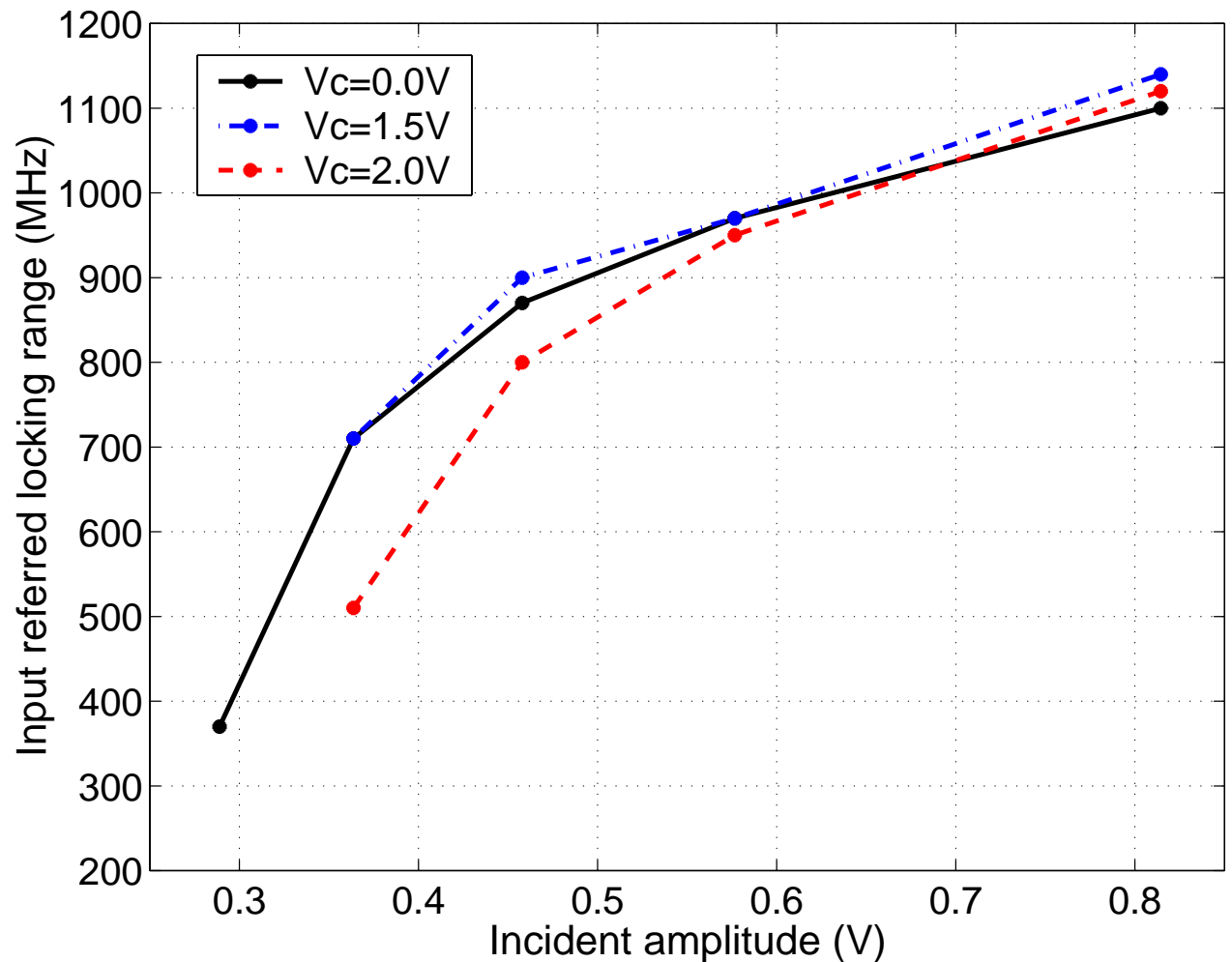
- locking range extension

Rategh *et al.*, symposium on VLSI circuits, June 1999, session 12.1



# MEASUREMENTS (LOCKING RANGE)

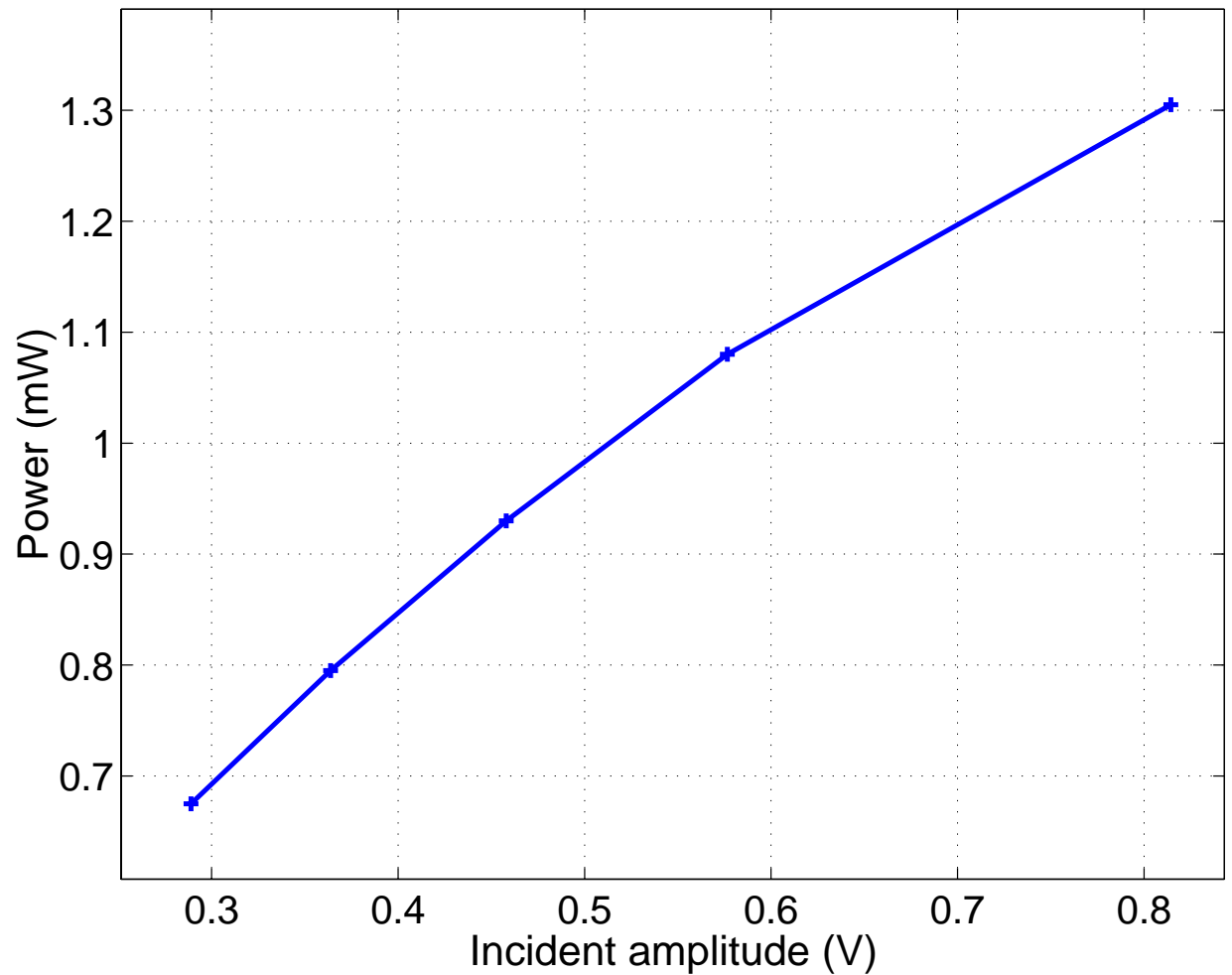
- 0.24 $\mu\text{m}$  CMOS
- $V_{\text{dd}}=1.5\text{V}$
- $f_o=2.2\text{GHz}$
- $f_i=4.4\text{GHz}$
- $\Delta f=900\text{MHz}$   
 $\approx 20\% @ 0.5\text{V}$



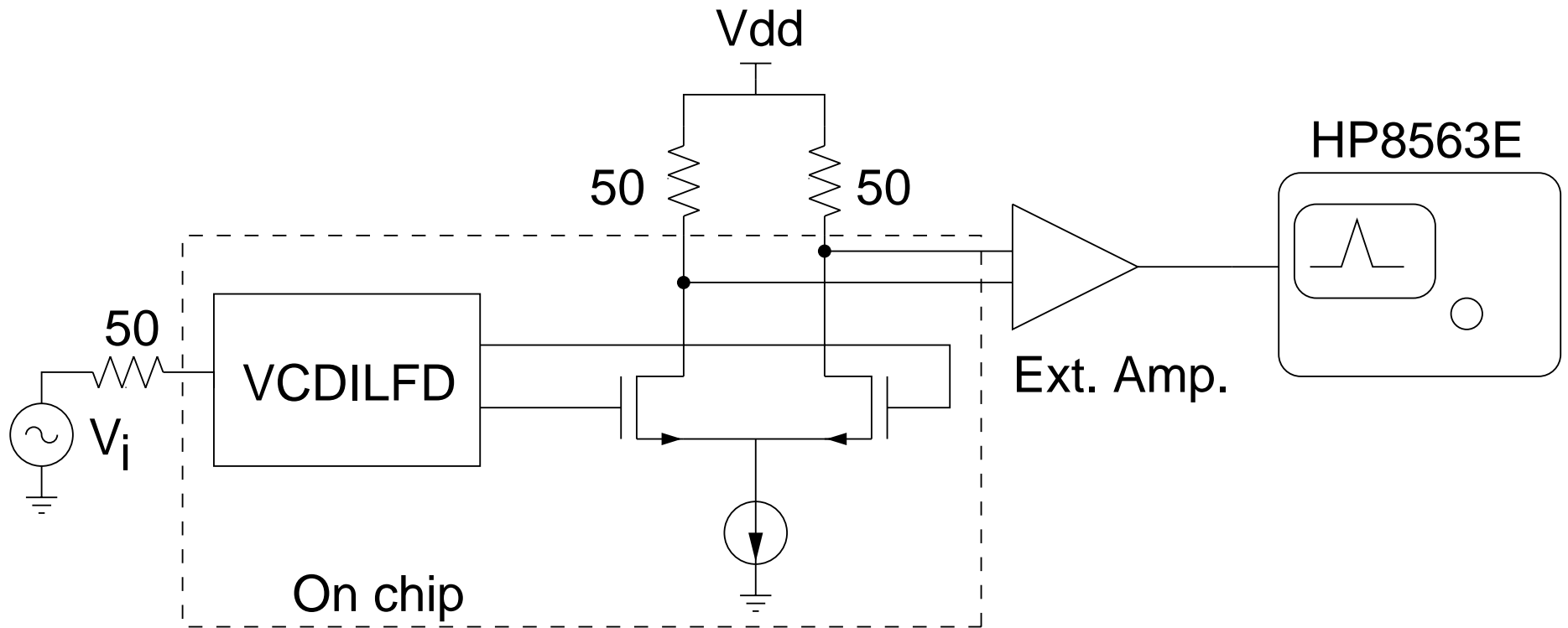
# MEASUREMENTS (POWER CONSUMPTION)

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- $0.24\mu\text{m}$  CMOS
- $V_{\text{dd}}=1.5\text{V}$
- $f_o=2.2\text{GHz}$
- $f_i=4.4\text{GHz}$
- $P=1.0\text{mW}$  @  $0.5\text{V}$

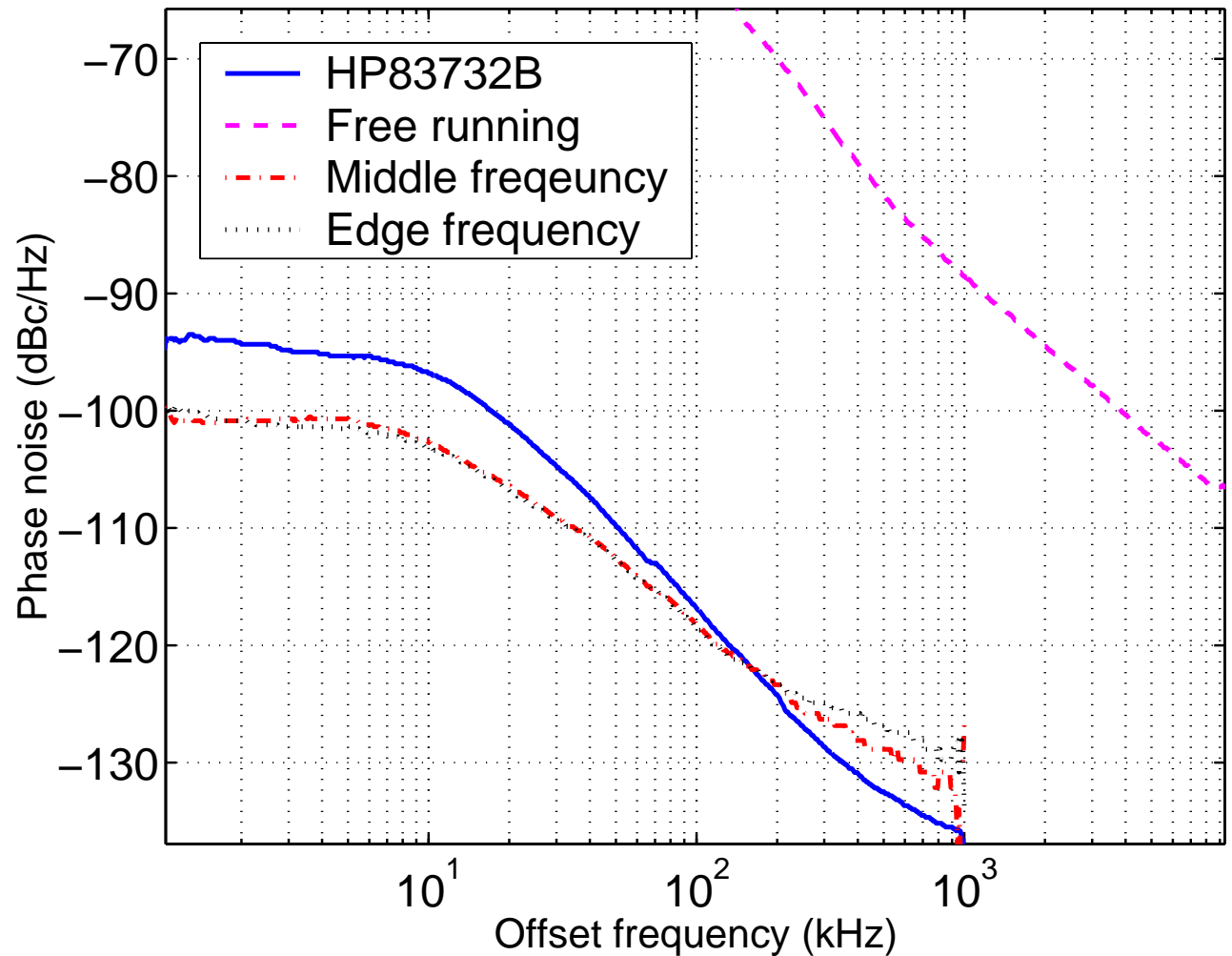


# PHASE NOISE MEASUREMENT TEST SETUP



# MEASUREMENTS (PHASE NOISE)

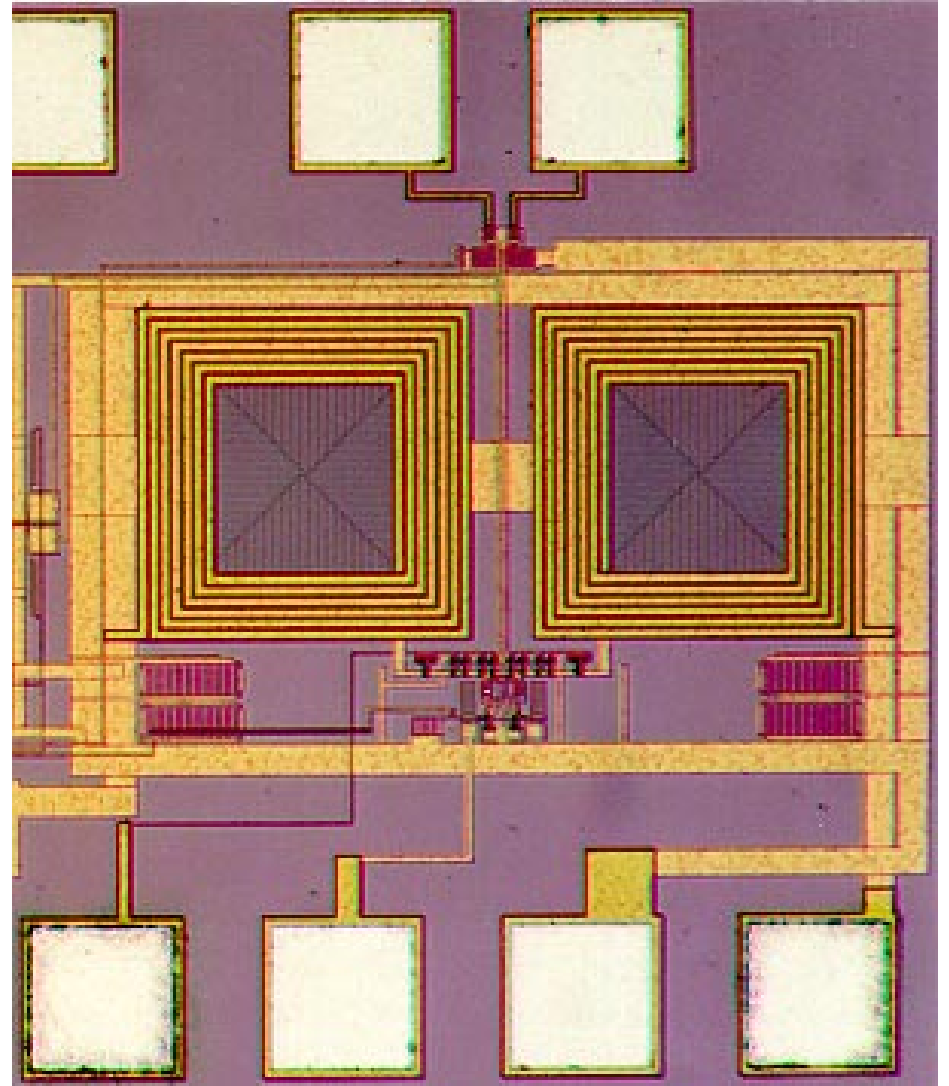
- 0.24 $\mu\text{m}$  CMOS
- Vdd=1.5V
- $f_o=2.2\text{GHz}$
- $f_i=4.4\text{GHz}$



# CHIP MICROGRAPH

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- $0.24\mu\text{m}$  CMOS
- $\text{area}=0.186\text{mm}^2$   
( $345\mu\text{m} \times 540\mu\text{m}$ )



# SUMMARY

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maximum frequency of operation	5GHz
output frequency tuning	110MHz $\approx$ 5%
input-referred locking range	450MHz $\approx$ 10% @ 0.7mW
	900MHz $\approx$ 20% @ 1.0mW
technology	0.24 $\mu$ m CMOS
die area	0.186mm <sup>2</sup>

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## *flip-flop-based divider*

0.24 $\mu$ m CMOS (simulation)	7mW @ 5GHz
0.1 $\mu$ m CMOS	2.6mW @ 5GHz

(Razavi *et al.*, JSSC Vol. 30, No.2, pp 101–109, Feb. 1995)

# CONCLUSION

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- injection–locked frequency dividers can be designed with:
  - very large locking range
  - very low power consumption
- spiral inductor design can be optimized to increase the ILFD locking range
- varactors can be used to extend the ILFD locking range (tracking ILFD)
- voltage–controlled ILFDs are suitable for low–power and high–frequency wireless systems

# ACKNOWLEDGMENTS

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