A 5GHz, 1mW CMOS Voltage Controlled Differential Injection Locked Frequency Divider

Hamid R. Rategh, Hirad Samavati, and Thomas H. Lee

Abstract— **A voltage controlled differential injection locked frequency divider (VCDILFD) with a large locking range is designed in a 0.24μm CMOS technology. A 29% locking range is achieved by an optimal inductor design and also by employing high Q accumulation mode MOS varactors to change the free–running oscillation frequency of the divider. The measurement results show frequency division at 5GHz with more than 1GHz locking range and power consumption of less than 1mW.**

I. Introduction

Most wireless receivers include at least one frequency synthesizer to generate an LO signal from a low frequency crystal oscillator. In contemporary CMOS radios, frequency synthesizers are one of the most power consuming blocks [4]. Frequency dividers used in the feedback path of phase locked loop (PLL) based synthesizers consume a large percentage of the total power [1]. Due to the frequency limitations of CMOS technologies, or to reduce power consumption, off–chip frequency dividers are often used [1]. Since most wireless systems operate in a narrow frequency band, injection locked frequency dividers (ILFDs) [3], which are narrowband in nature, can be used to trade off bandwidth for power and maximum frequency of operation. Thus higher integration and lower power operation can be achieved. In this paper we demonstrate the design of high frequency ILFDs with very large bandwidth and small power consumption.

II. Injection Locked Frequency Dividers

Injection locking can be used to frequency lock an oscillator to an external (incident) signal. When the incident frequency is a harmonic of the oscillation frequency (superharmonic injection locking), frequency division is performed [3]. The oscillation conditions of unity loop gain and zero excess phase should be satisfied in an injection locked frequency divider. The frequency of operation (locking range) of an ILFD can be limited by failure of either the phase or gain condition [3]. Fig. 1 shows a model for an ILFD. The function $f(x)$ models all the nonlinearities in an ILFD and $H(\omega)$ represents the frequency selective block. In the special case of a third order $f(x)$ and divide–by–two operation, the phase–limited locking range of an LC ILFD can be expressed as:

The authors are with the Center for Integrated Systems, Stanford University, Stanford, CA 94305.

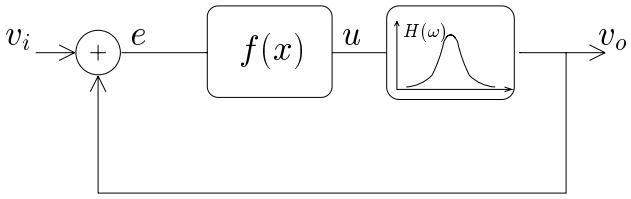

Fig. 1. Model for an injection locked frequency divider

$$|\frac{\Delta\omega}{\omega_r}| < |\frac{H_0 a_2 V_i}{2Q}| \quad (1)$$

where ω_r is the free–running oscillation frequency, $\Delta\omega$ is the frequency offset from ω_r, V_i is the incident amplitude, H_0 is the impedance of the LC tank at resonance, Q is the quality factor of the LC tank, and a_2 is the second–order coefficient of the nonlinearity in $f(x)$ [3]. As (1) suggests, a larger $\frac{H_0}{Q}$ results in a larger locking range for a given incident amplitude. In an LC oscillator $\frac{H_0}{Q} = \omega L$, so the largest practical inductance should be used to maximize the locking range.

III. Circuit implementation

Fig. 2 shows the schematic of a voltage controlled differential ILFD (VCDILFD). The incident signal is injected into the gate of M3 which delivers the incident signal to the common source connection of M1 and M2. The output signal is fed back to the gates of M1 and M2. The output and incident signals are thus summed across the gates and sources of M1 and M2.

A. Inductors

On–chip spiral inductors with patterned ground shields [7] are used in this design. As mentioned in section II, an inductor with the biggest value should be used to achieve the largest possible locking range. However, the minimum power consumption is achieved when $H_0 = LQ\omega$ is maximized. Due to the parasitics associated with spiral inductors, maximizing L does not necessarily maximize the LQ product. So the power and locking range criteria may not be satisfied simultaneously and one generally must be traded off for the other. To design the spiral inductor we use the same inductor model reported in [6]. The inductance is first approximated with a monomial expression as in [2]. Convex optimization is used

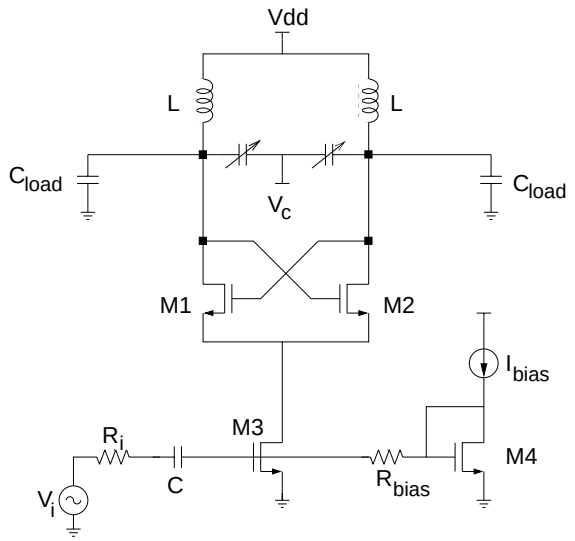

Fig. 2. Schematic of the voltage controlled differential ILFD (VCDILFD)

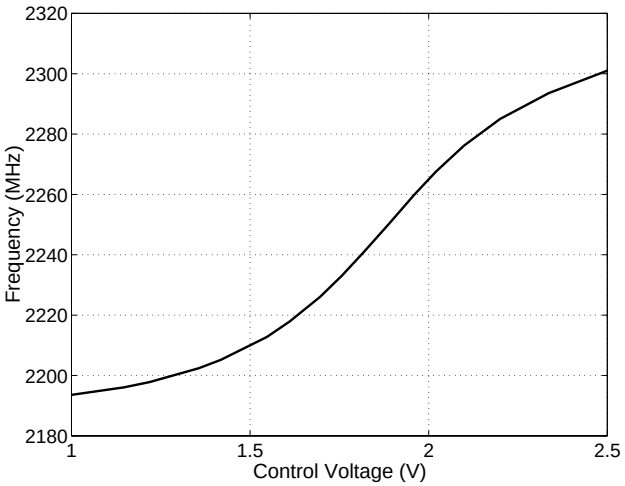

Fig. 3. Tuning range of the free running VCDILFD

next to find the inductor with the maximum inductance such that H_0 is large enough to satisfy the power budget. The inductors in this design are 12nH each with a quality factor of 5.8 at the output frequency (2.5GHz).

B. Varactors

To increase further the locking range of the ILFD we design the LC tank with a variable resonant frequency. Accumulation mode MOS varactors [5] are used for this purpose. Each varactor is laid out with 12 fingers which are 2μm wide and 0.5μm long. The quality factor of this varactor at 2.5GHz is estimated to exceed 60. The quality factor of the LC tank is thus determined mainly by the losses of the inductors.

IV. Measurement Results

A VCDILFD of the type shown in Fig. 2 is designed in a 0.24μm CMOS technology. The chip shown in Fig. 4 has an area of 0.186mm^2 ($345\mu\text{m} \times 540\mu\text{m}$) excluding the pads. In the free–running mode, the oscillator is biased such that $Vdd = 2.0$V and the tail current is 600μA. The free–running oscillation frequency as a function of the control voltage (V_c) is shown in Fig. 3. The tuning range is about 110MHz ($\approx 5\%$ of the center frequency) for a 1.5V control voltage variation.

For divide–by–two operation the supply voltage is set to 1.5V and the tail current is reduced to 300μA. However, in the presence of a large incident signal the average tail current increases beyond 300μA. Fig. 5 shows the operation frequencies of the divider as a function of the incident amplitude for two different control voltages. For a given incident amplitude the operation region lies between the two ends of each curve in Fig. 5. By increasing the control voltage the resonant frequency of the LC tank increases and the operation region moves up in frequency. For a given control voltage more than 1100MHz locking range is achieved when $V_i = 810$mV. Addition of the voltage tuning capability increases the total achievable locking range to greater than 1280MHz ($\approx 29\%$ of the center frequency) at this incident amplitude. Higher incident amplitudes are not tested due to instrument limitations.

Fig. 6 shows the locking range as a function of the incident amplitude for three different control voltages. As expected, changing the control voltage only changes the operation frequencies and not the locking range. It is important to observe that, unlike the single–ended ILFD reported in [3], the locking range in a DILFD is phase limited and monotonically increases with incident amplitudes even as large as 810mV. This difference can be attributed to the fact that the voltage gain of M3 in Fig. 2 is less than unity and the amplitude of the incident signal at the summing node (the common source connection of M1 and M2) is less than that on the gate of M3. The gain–limited region of the locking range which is observed only at large incident amplitudes [3] therefore appears at larger input levels. Compounding this effect is that the increased average tail current (in a DILFD) in the presence of a large incident signal can change $f(x)$ and effectively move the gain–limited region of the locking range to larger incident amplitudes. The average power in the VCDILFD as a function of the incident amplitude is shown in Fig. 7. The average power at 450mV incident amplitude is less than 1mW while the locking range exceeds 1GHz.

Fig. 8 shows the setup for the phase noise measurement. The phase noise measurement results are shown in Fig. 9. The solid line shows the phase noise of the HP83732B signal generator used as the incident signal. The dashed line is the phase noise of the free–running VCDILFD. The two other curves are the phase noise of the VCDILFD when locked to two

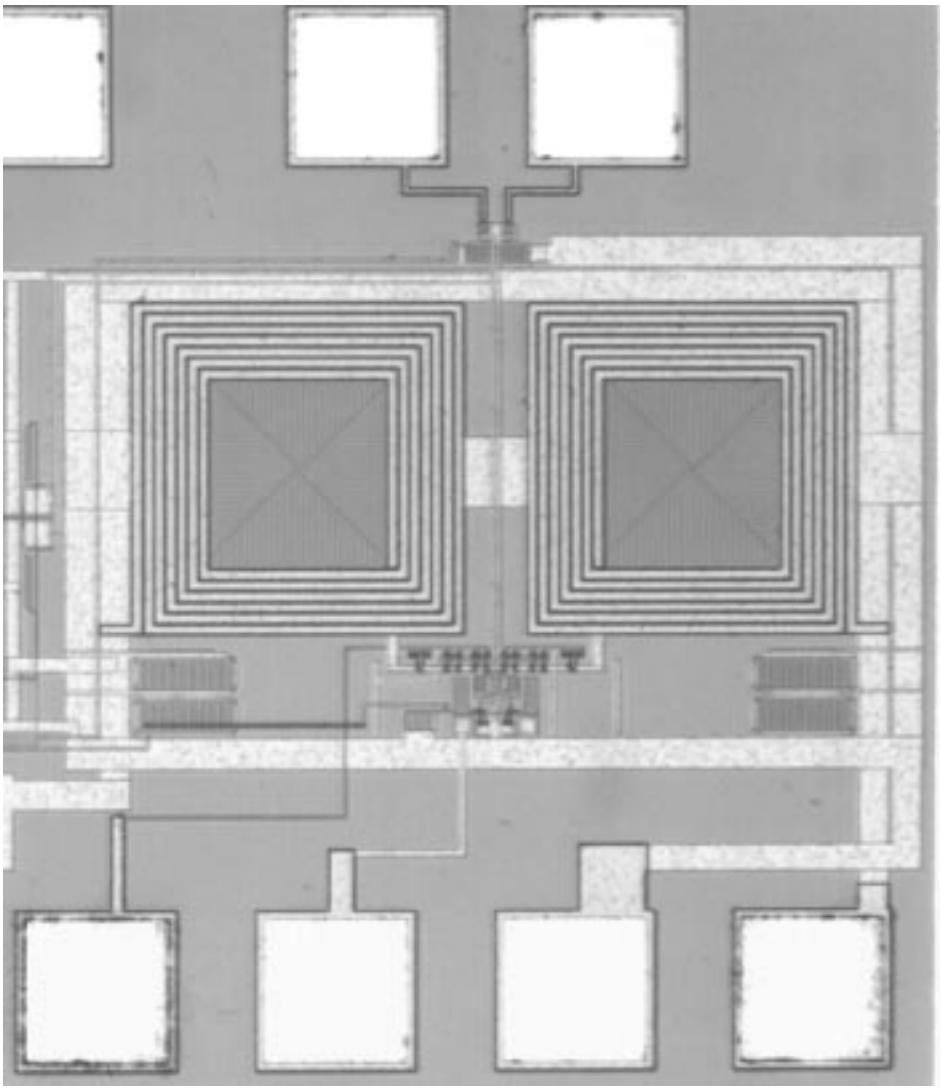

Fig. 4. Chip micrograph of the VCDILFD

different incident frequencies. The curve marked as *middle frequency* is measured when the incident frequency is in the middle of the locking range and the *edge frequency* curve is measured at the lower edge of the locking range. At low offset frequencies the output of the frequency divider follows the phase noise of the incident signal and is $6dB$ lower due to the divide–by–two operation. However, at larger offset frequencies the added noise from the output buffer, the external amplifier (Fig. 8), and from the divider itself reduces the $6dB$ difference between the incident and output phase noise. The phase noise measurements for offset frequencies higher than 300kHz are not accurate due to the dominance of noise from the output buffer and the external amplifier.

V. Conclusion

In this work we show how an injection locked frequency divider which is narrowband in nature can be designed with a very large locking range and still consume very little power. The measurement results on a 5GHz injection locked divider show a locking range greater than 1GHz for less than 1mW of power consumption. The locking range is more than 1.28GHz when the power consumption is increased to 1.3mW. This locking range is much larger than the bandwidth of any standard wireless system. Even considering uncertainties of on–chip passive element values, 29% locking range is more than enough. We believe that voltage controlled ILFDs are excellent alternatives to conventional frequency dividers, especially at multi–GHz frequencies.

VI. Acknowledgments

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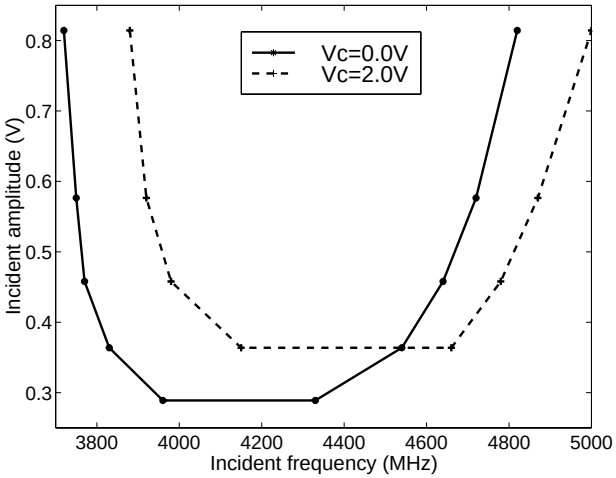

Fig. 5. Operation frequencies of the VCDILFD for different incident amplitudes

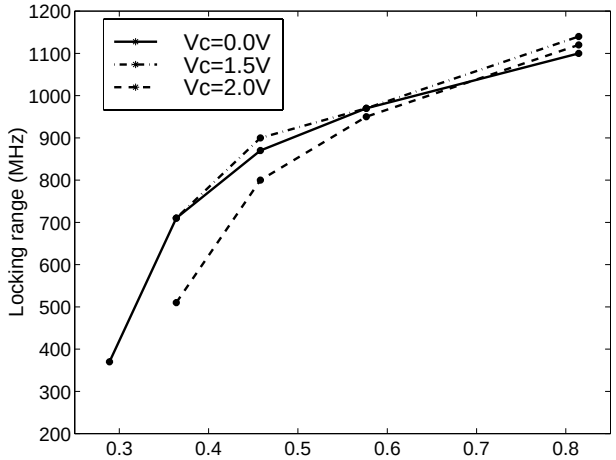

Fig. 6. Locking range as a function of incident amplitude

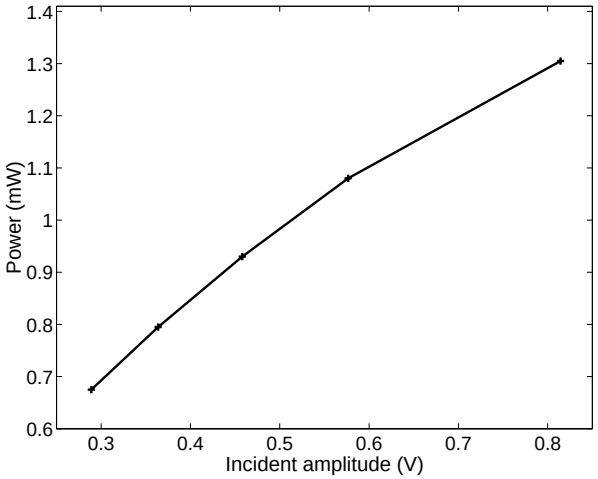

Fig. 7. Average power as a function of incident amplitude

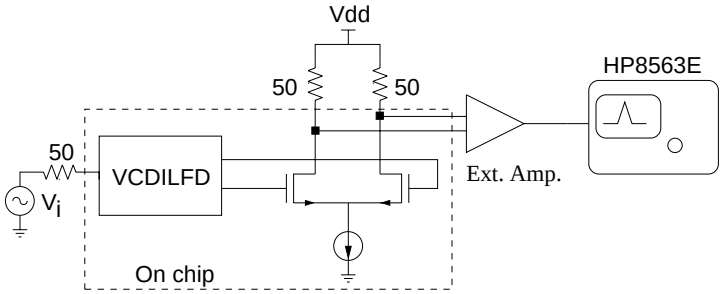

Fig. 8. Phase noise measurement setup

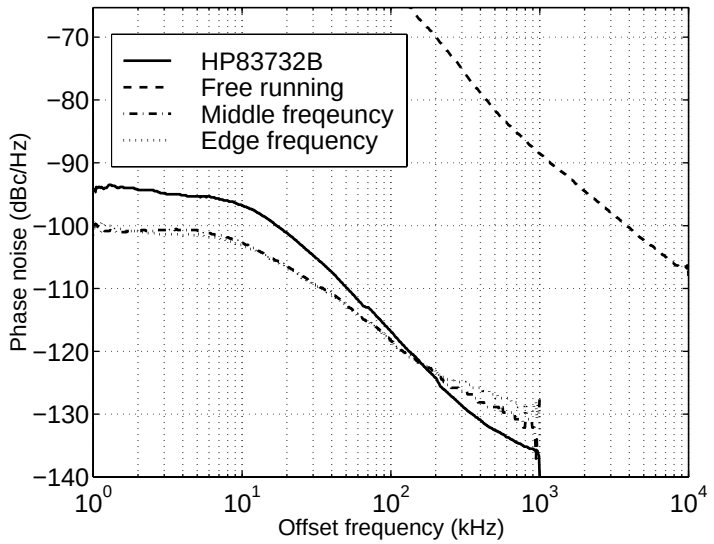

Fig. 9. Phase noise measurements

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